4D SYSTEMS
TURNING TECHNOLOGY INTO ART

4DOLED - 282815

1.5" 128x128 262K Colour PMOLED

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DATASHEET

DOCUMENT DATE: 20TH SEPTEMBER 2018
DOCUMENT REVISION: 1.0

Revision History

REVISION	DATE	COMMENT	REMARKS
1.0	20/09/2018	Initial Version	Initial Draft Version

4DOLED-282815

Table of Contents

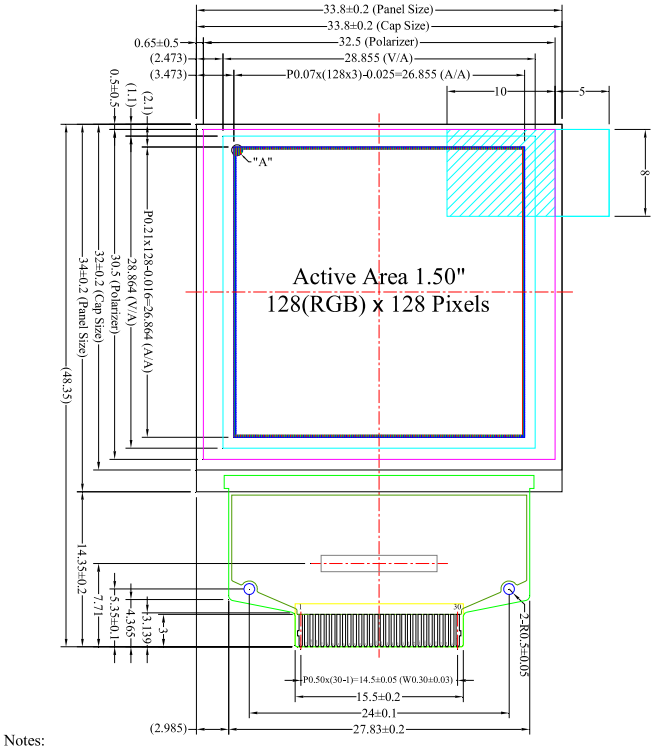
1 General Specification

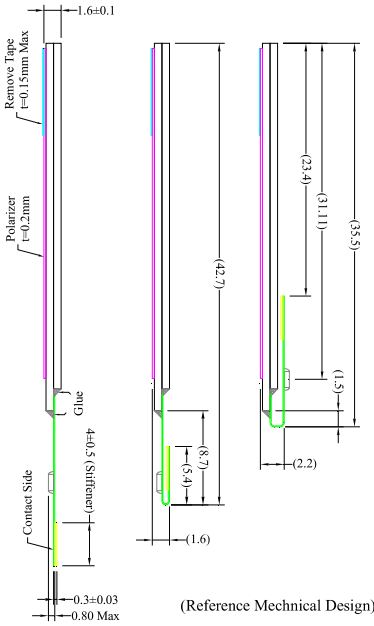
The 4DOLED-282815 is a 1.5" 128x128 pixel resolution 262K colour Passive Matrix OLED display. This OLED is the same display used in the micro-OLED range of modules. It allows a very cost-effective means of adding a full colour small display to any product or your next microcontroller project.

ITEM	CONTENTS	UNIT
Display Mode	Passive Matrix	
Size	1.5	Inch
Color Depth	262K	
Drive Duty	1/128	Duty
Display Size	33.80 x 34.00 x 1.60	mm
Active Area (W × H)	26.855 x 26.864	mm
Dot Pitch (W × H)	0.07 x 0.21	mm
Number of Dots (Pixels)	128 (RGB) × 128	
Pixel Size	0.045 x 0.194	mm
Weight	3.75	g

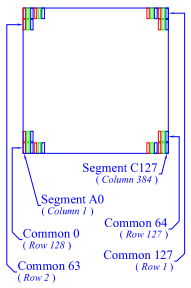
2 Mechanical Details

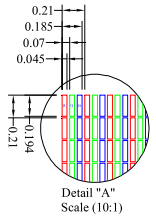
Item	Date	Remark
A	20080815	Original Drawing
B	20120426	Remove Single-side Tape





(Reference Mechnical Design)





Detail "A"
Scale (10:1)

Pin	Symbol
1	N.C. (GND)
2	VCC
3	VCOMH
4	VDDIO
5	VSL
6	N.C.
7	D7
8	D6
9	D5
10	D4
11	D3
12	D2
13	D1
14	D0
15	E/RD#
16	R/W#
17	BS0
18	BS1
19	CS#
20	D/C#
21	RES#
22	IREF
23	GPIO1
24	GPIO0
25	N.C.
26	VDD
27	VCI
28	VSS
29	N.C.
30	N.C. (GND)

Notes:

1. Driver IC: SSD1351
2. Die Size: 10700um x 1500um
3. COF Number: SSD1351U3
4. Interface:
   8-bits 68XX/80XX Parallel, 3-/4-wire SPI
5. General Tolerance: ±0.30
6. The total thickness (1.70 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 1.95 Max.

Customer Approval Signature	4D Systems Pty LTD.					Drawing Number	Rev.
						DFE2828CNCF38	B
	Unless Otherwise Specified		Title	4DOLED-282815		Material	
	Unit	mm				Soda Lime / Polyimide	
	General Roughness						
	Tolerance			Drawn	E.E.	Panel / E.	P.M.
	Dimension	±0.3	By	Dora Yang	Albert Lin	Ivy Lo	Cherry Lin
	Angle	±1	Date	20120426	20120426	20120426	20120426

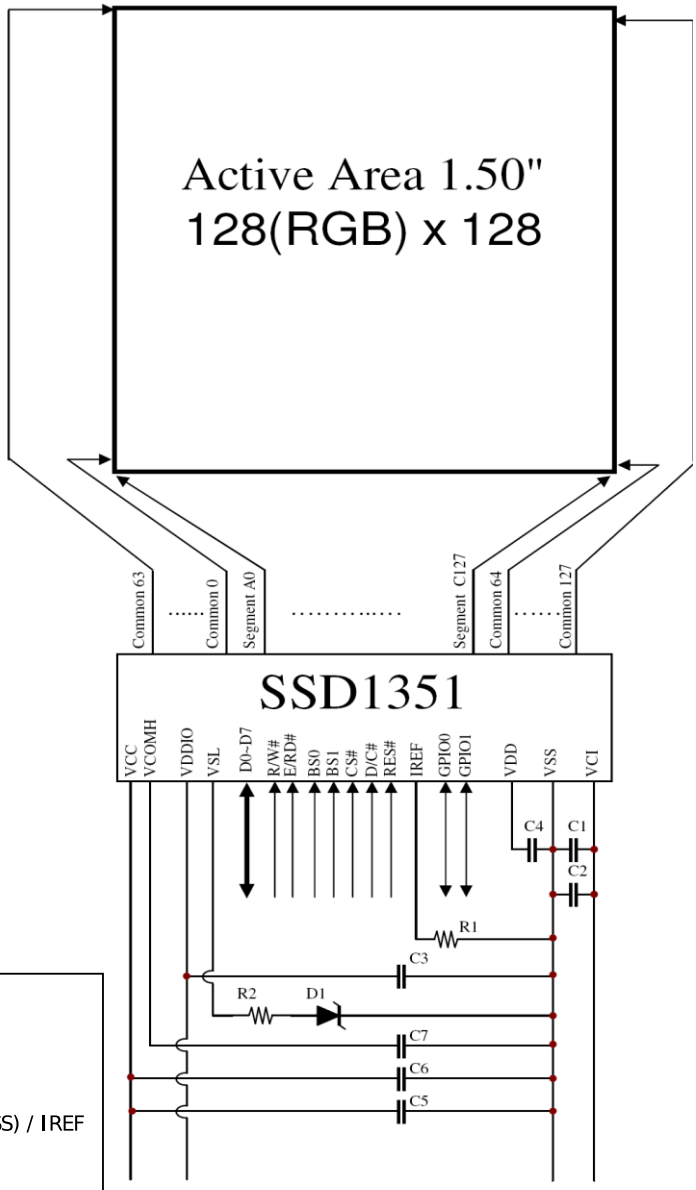
Scale	Sheet	Size
1:1	1 of 1	A3

3 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
27	VCI	P	**Power Supply for Operation** This is a voltage supply pin. It must be connected to external source & always be equal to or higher than V_{DDIO}.
26	VDD	P	**Power Supply for Core Logic Circuit** This is a voltage supply pin which is regulated internally from V_{CI}. A capacitor should be connected between this pin & V_{SS} under all circumstances.
4	VDDIO	P	**Power Supply for I/O Pin** This pin is a power supply pin of I/O buffer. It should be connected to V_{CI} or external source. All I/O signal should have VI_H reference to V_{DDIO}. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to V_{DDIO}.
28	VSS	P	**Ground of Logic Circuit** This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
2	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. It must be connected to external source.
Driver			
22	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5µA maximum.
3	VCOMH	P	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and V_{SS}
5	VSL	P	**Voltage Output Low Level for SEG Signal** This is segment voltage reference pin. External VSL is set as default. This pin has to connect with resistor and diode to ground.
External IC Control			
24 23	GPIO0 GPIO1	I/O	**General Purpose Input/Output** This pin could be left open individually or has signal inputted/outputted. It is able to use as the external DC/DC converter circuit enabled/disabled control or other applications.
Interface			
17 18	BS0 BS1	O	**Communicating Protocol Select** These pins are MCU interface selection input. See the following table: BS0 / BS1 3-wire SPI: 1 / 0 4-wire SPI: 0 / 0 8-bit 68XX Parallel: 1 / 1 8-bit 80XX Parallel: 0 / 1
21	RES#	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
19	CS#	I	**Chip Select** This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

Pin Number	Symbol	I/O	Function
Interface (continued)			
20	D/C#	I	**Data/Command Control** This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. When 3-wire serial mode is selected, this pin must be connected to VSS. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
15	E/RD#	I	**Read/Write Enable or Read** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to V_{SS}.
16	R/W#	I	**Read/Write Select or Write** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to V_{SS}.
7~14	D7~D0	I/O	**Host Data Input/Output Bus** These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.
Reserve			
1,35	N.C. (GND)	-	**Reserved Pin (Supporting Pin)** The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.
6, 25, 29	N.C.	-	**Reserved Pin** The N.C. pins between function pins are reserved for compatible and flexibledesign.

4 Block Diagram



C1, C5: 0.1∝F
C2 : 4.7∝F
C6 : 10∝F
C3, C4: 1∝F
C7 : 4.7uF / 25V Tantalum Capacitor
R1 : 560kΩ, R1 = (Voltage at IREF – VSS) / IREF
R2 : 50Ω, 1/4W
D1 : ≈1.4V, 0.5W

MCU Interface Selection : Based on BS0 and BS1 connection, showed as below table.
Pins connected to MCU interface : D7~D0, E/RD#, R/W#, CS#, D/C#, and RES#

EIM=1(default)

BS0	BS1	Interface mode	Data Bus								Control Bus				
			D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	E/RD#	RES#
0	0	4-wire SPI	**0**	**0**	**0**	**0**	**0**	**NC**	SDIN	SCLK	CS#	D/C#	**0**	**0**	RES#
0	1	3-wire SPI	**0**	**0**	**0**	**0**	**0**	**NC**	SDIN	SCLK	CS#	**0**	**0**	**0**	RES#
1	0	8bit 8080	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	WR#	RD#	RES#
1	1	8bit 6800	D7	D6	D5	D4	D3	D2	D1	D0	CS#	D/C#	R/W#	R	RES#

Note:

a. “0” is connected to VSS.

b. “1” is connected to VDD.

c. “NC” is not-connected.

5 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1,2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1,2
Supply Voltage for I/O Pins	V_{DDIO}	-0.5	V_{CI}	V	1,2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1,2
Operating Temperature	T_{OP}	-40	70	°C	3
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (90 cd/m^2)		10,000	-	Hour	4
Life Time (70 cd/m^2)		15,000	-	Hour	4
Life Time (50 cd/m^2)		20,000	-	Hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 13.0V, Ta = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

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6 Optics & Electrical Characteristics

6.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	70	90	-	cd/m^2
C.I.E (White)	(x) (y)	C.I.E 1931	0.26 0.29	0.30 0.33	0.34 0.37	
C.I.E (Red)	(x) (y)	C.I.E 1931	0.60 0.30	0.64 0.34	0.68 0.38	
C.I.E (Green)	(x) (y)	C.I.E 1931	0.27 0.58	0.31 0.62	0.35 0.66	
C.I.E (Blue)	(x) (y)	C.I.E 1931	0.10 0.12	0.14 0.16	0.18 0.20	
Dark Room Contrast	CR		-	>10,000 :1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 13.0V.
Software configuration follows Section 4.4 Initialization.

6.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note 5	12.5	13.0	13.5	V
High Level Input	V_{IH}		0.8 X V_{DDIO}	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	0.2 X V_{DDIO}	V
High Level Output	V_{OH}	I_{out} =100µA, 3.3MHz	0.9 X V_{DDIO}	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{out} =100µA, 3.3MHz	0	-	0.1 X V_{DDIO}	V
Operating Current for V_{CI}	I_{CI}		-	240	300	µA
Operating Current for V_{CC}	I_{CC}	Note 6	-	13.3	17.0	mA
		Note 7		23.2	29.0	mA
		Note 8		33.4	42.0	mA
Sleep Mode Current for V_{CI}	$I_{CI, Sleep}$		-	2	10	µA
Sleep Mode Current for V_{CC}	$I_{CC, Sleep}$		-	2	10	µA

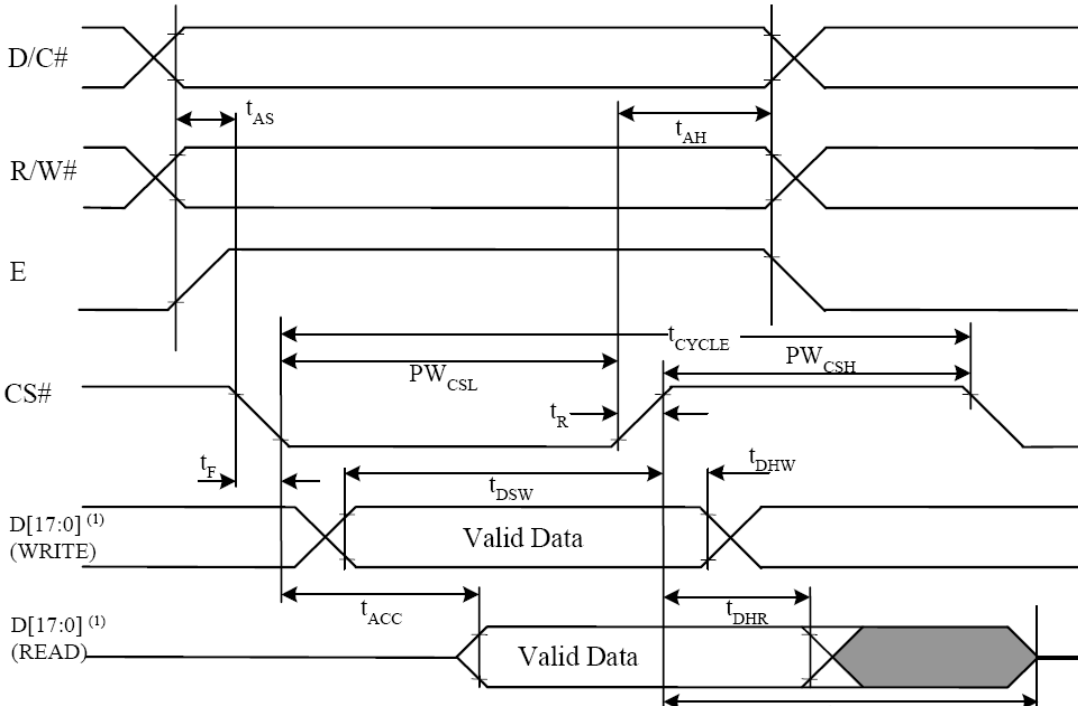
Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{CI} = 2.8V, V_{CC} = 13.0V, 30% Display Area Turn on.
Note 7: V_{CI} = 2.8V, V_{CC} = 13.0V, 50% Display Area Turn on.
Note 8: V_{CI} = 2.8V, V_{CC} = 13.0V, 100% Display Area Turn on.
* Software configuration follows Section 4.4 Initialization.

6.3 AC Characteristics

6.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7		
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_F	Rise Time	-	15	ns
t_R	Fall Time	-	15	ns

* (V_{CI} - V_{SS} = 2.4V to 3.5V, V_{DDIO} - V_{SS} = 1.65V to V_{CI}, T_a = 25°C)

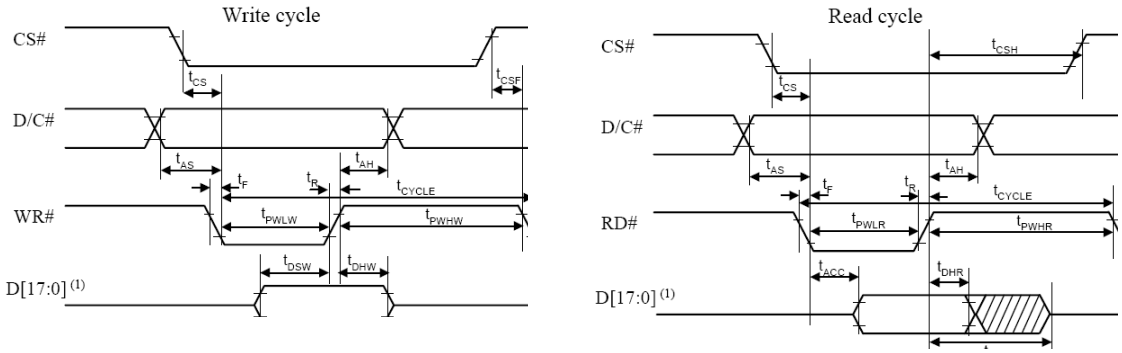


* (1) When 8-bit Used: D[7:0] Instead

6.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description		Min	Max	Unit	Port
t_{AH8}	Address Setup Timing		5	-	ns	CSB
t_{AS8}	Address Hold Timing		5	-	ns	RS
t_{CYC8}	System Cycle Timing (Read)		200	-	ns	RDB
t_{RDLR6}	Read “L” Pulse Width		90	-	ns	
t_{RDHR6}	Read “H” Pulse Width		90	-	ns	
t_{CYC8}	System Cycle Timing (Write)		100	-	ns	WRB
t_{WRLW8}	Write “L” Pulse Width		45	-	ns	
t_{WRHW8}	Write “H” Pulse Width		45	-	ns	
t_{RDD8}	Read Data Output Delay Time	*CL = 15pF	-	60	ns	D[17:9]
t_{RDH8}	Data Hold Timing		0	60	ns	
t_{DS8}	Write Data Setup Timing		30	-	ns	
t_{DH8}	Write Data Hold Timing		10	-	ns	

* (V_{CI} - V_{SS} = 2.4V to 3.5V, V_{DDIO} - V_{SS} = 1.65V to V_{CI}, T_a = 25°C)

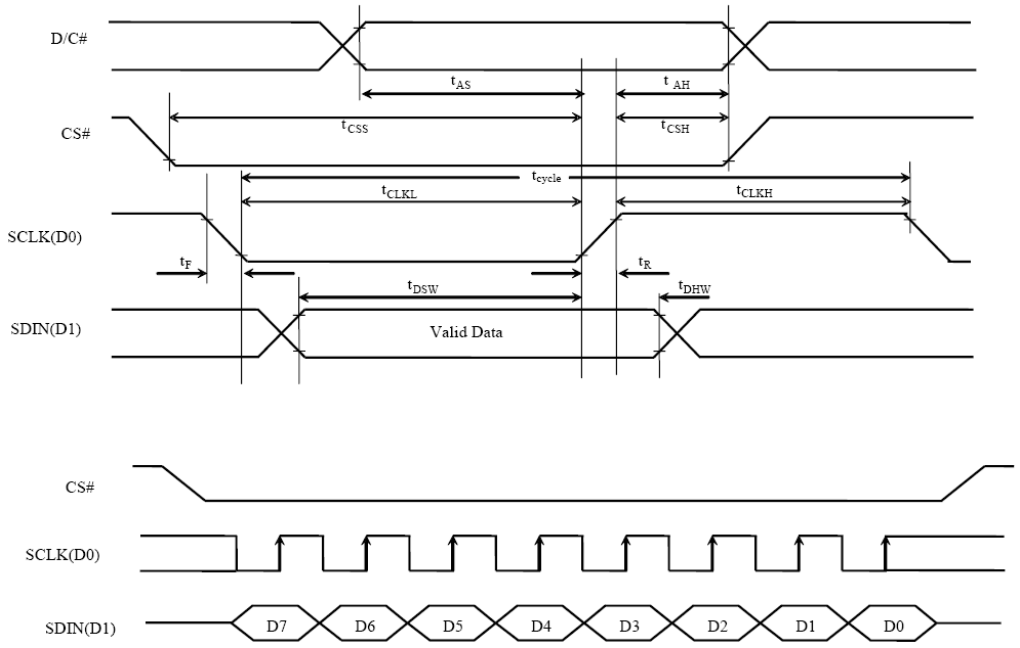


* (1) When 8-bit Used: D[7:0] Instead

6.3.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

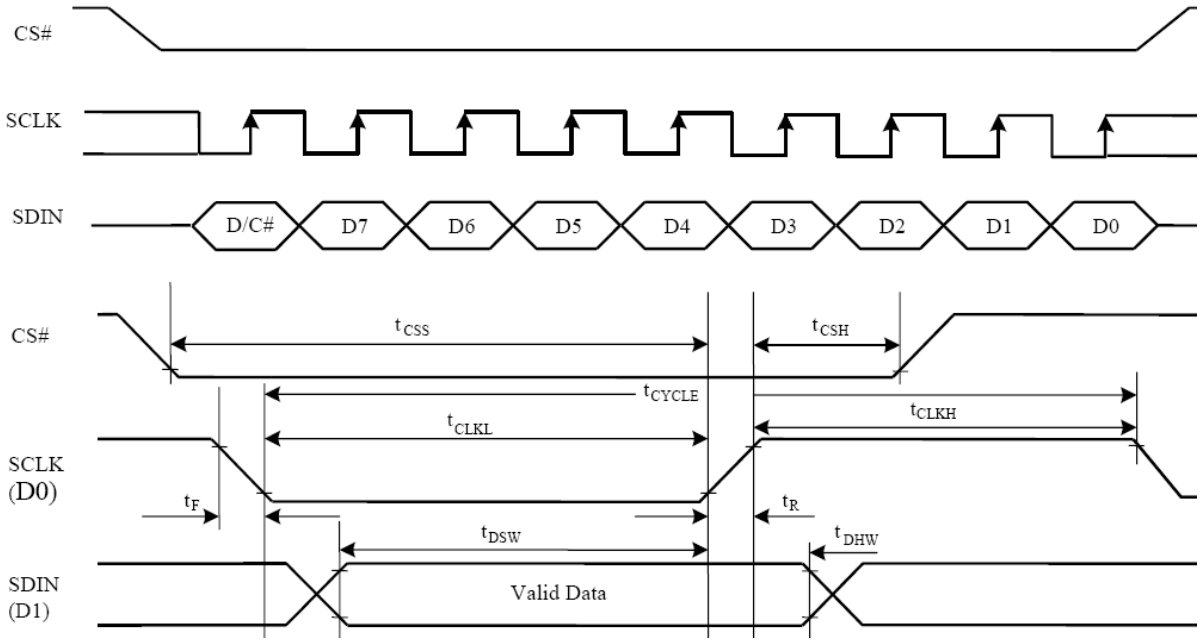
* (V_{CI} - V_{SS} = 2.4V to 3.5V, V_{DDIO} - V_{SS} = 1.65V to V_{CI}, T_a = 25°C)



6.3.4 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{CI} - V_{SS} = 2.4V to 3.5V, V_{DDIO} - V_{SS} = 1.65V to V_{CI}, T_a = 25°C)



7 Functional Specification

7.1 Commands

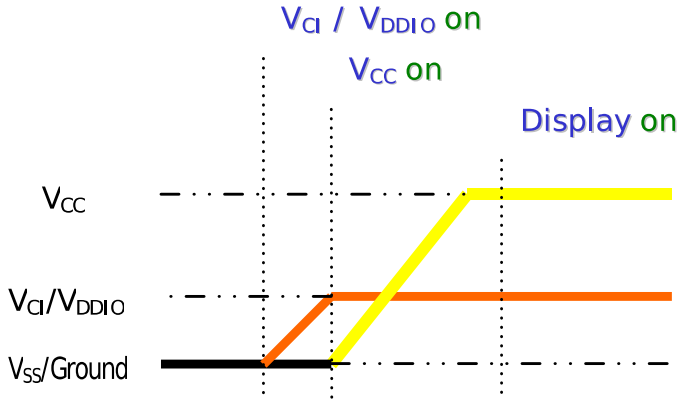
Refer to Technical Manual for the SSD1351

7.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

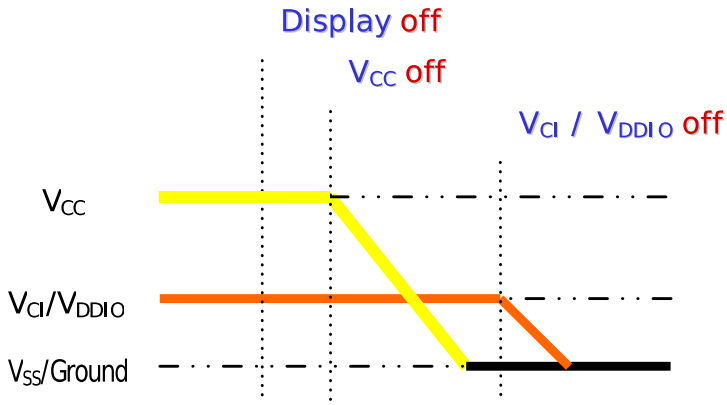
7.2.1 Power up Sequence:

1) Power up V_{CI} / V_{DDIO}
2) Send Display off command
3) Initialization
4) Clear Screen
5) Power up V_{CC}
6) Delay 200ms
   (When V_{CC} is stable)
7) Send Display on command



7.2.2 Power down Sequence:

1) Send Display off Command
2) Power down V_{CC}
3) Delay 100ms
   (When VCC is reach 0 and panel is completely discharged)
4) Power down V_{CI} / V_{DDIO}



Note 9:

1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{CI} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{DDIO}, V_{CC}) can never be pulled to ground under any circumstance.

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7.3 Reset Circuit

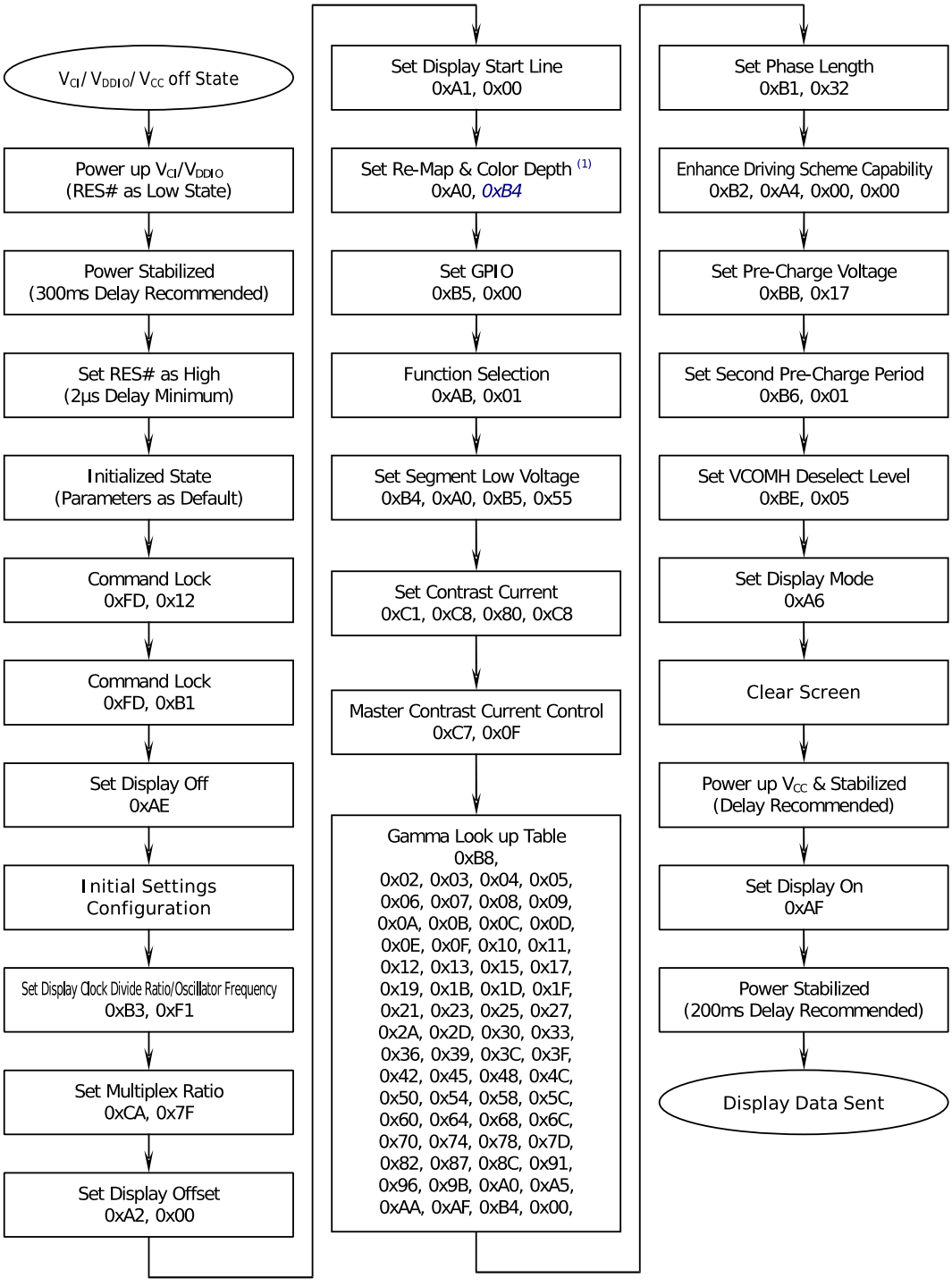
When RES# input is low, the chip is initialized with the following status:

1) Display is OFF
2) 128(RGB) x 128 Display Mode
3) Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4) Display start line is set at display RAM address 0
5) Column address counter is set at 0
6) Normal scan direction of the COM outputs
7) Command A2h, B1h, B3h, BBh, BEh are locked by command FDh

7.4 Actual Application Example

Command usage and explanation of an actual example

<Power up sequence>



(1) This command could be programmable to fit various applications.

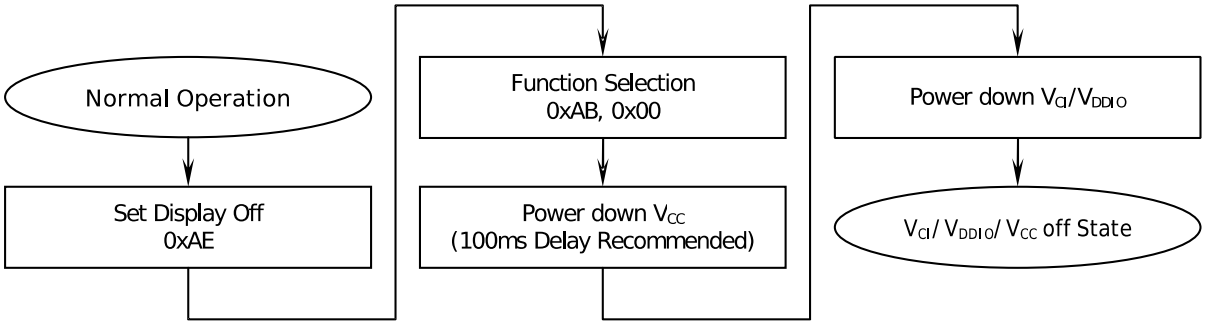
0xB4 → 262,144 Colors Mode

0x74 → 65,536 Colors Mode

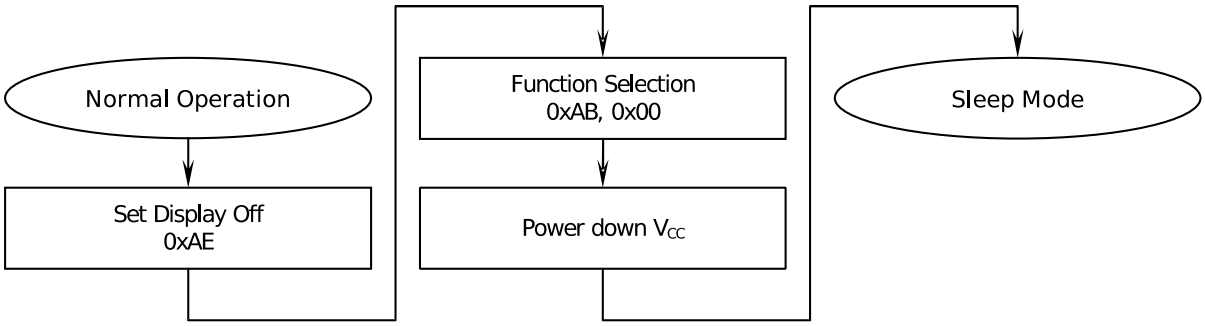
Others → Please contact us for further information.

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

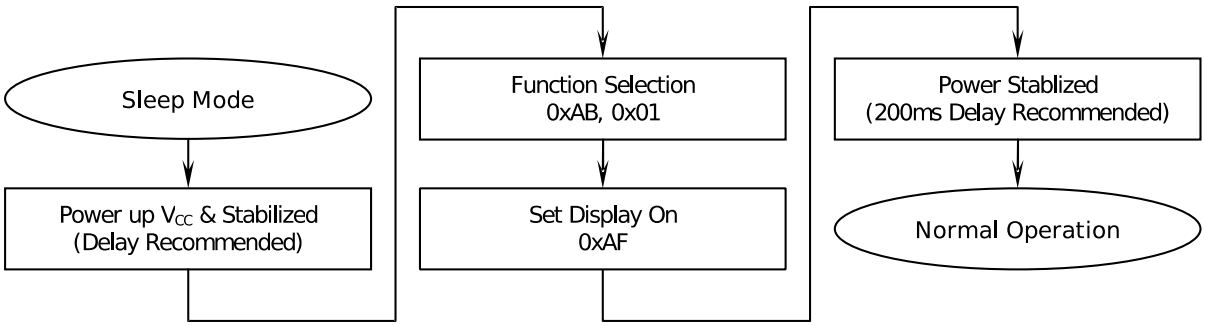
<Power down sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



8 Reliability

8.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70 °C,240 hrs	The operational functions work
Low Temperature Operation	-40 °C,240 hrs	
High Temperature Storage	85 °C,240 hrs	
Low Temperature Storage	-40 °C,240 hrs	
High Temperature / Humidity Operation	60 °C, 90%RH , 240 hrs	
Thermal Shock	-40 °C ↔ 85°C,24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

8.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

9 Outgoing Quality Control Specification

9.1 Environment required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

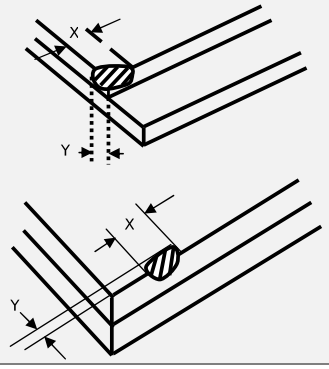
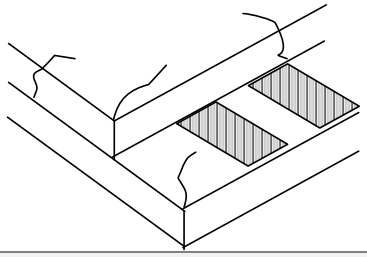
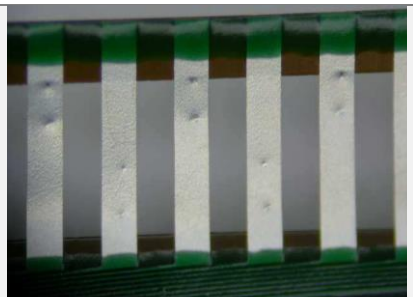
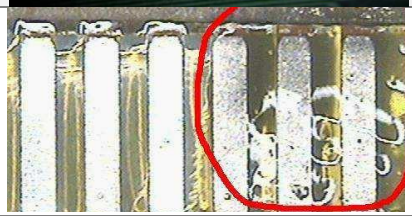
9.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

9.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

9.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 
Panel Crack	Minor	Any crack is not allowable 
Copper Exposed (Even pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore If Any

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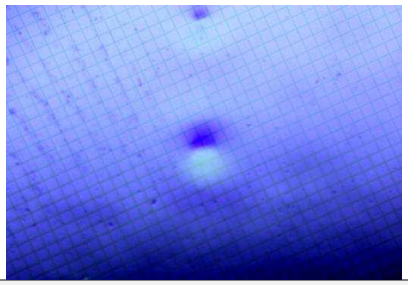
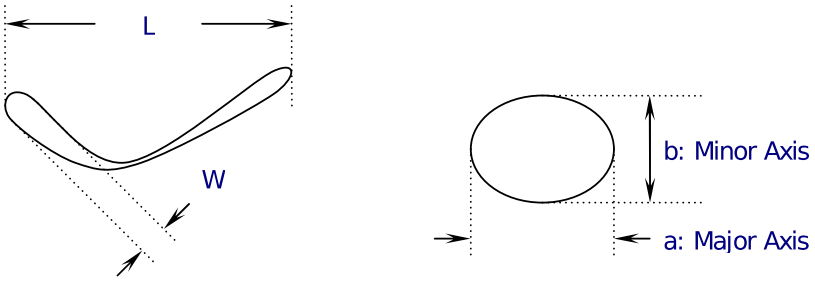
9.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary

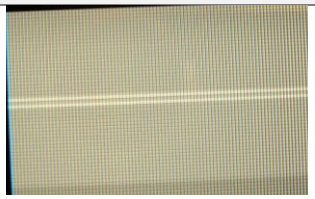
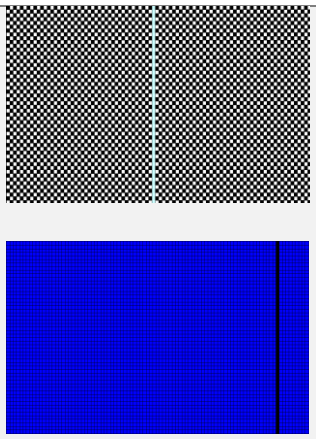
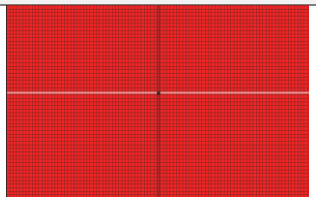
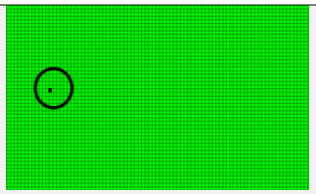
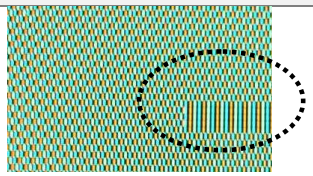
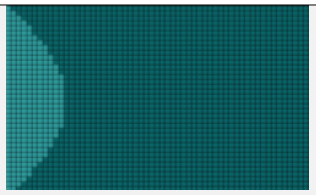
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore if polarizer is not affected
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 → Ignore if no influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & W (Unit: mm): W = (a + b) / 2



9.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	Not Allowable
Bright line	Major	
Missed Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-Uniform (Luminance Variation within a Display)	Major	

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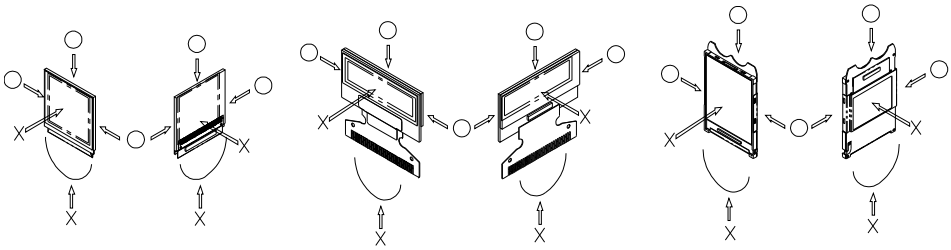
10 Precautions When Using These OEL Display Modules

10.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighbourhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

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10.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

10.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{CI}). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighbouring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1351
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

10.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

10.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the COF & FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.

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4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

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