- **State-of-the-Art Advanced BiCMOS Technology (ABT)** *Widebus*™ **Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation**

- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})**

- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**

- **Power Off Disables Outputs, Permitting Live Insertion**

- **High-Impedance State During Power Up and Power Down Prevents Driver Conflict**

- **Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating**

- **Output Ports Have Equivalent 30-Ω Series Resistors, So No External Resistors Are Required**

- **Auto3-State Eliminates Bus Current Loading When Output Exceeds V_{CC} + 0.5 V**

- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model; and Exceeds 1000 V Using Charged-Device Model, Robotic Method**

- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**

- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**

- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

NOTE: For order entry:
The DGG package is abbreviated to G, and
the DGV package is abbreviated to V.

SN54ALVTH162827 . . . WD PACKAGE
SN74ALVTH162827 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1$\overline{OE1}$	1		56		1$\overline{OE2}$
1Y1	2		55		1A1
1Y2	3		54		1A2
GND	4		53		GND
1Y3	5		52		1A3
1Y4	6		51		1A4
V_{CC}	7		50		V_{CC}
1Y5	8		49		1A5
1Y6	9		48		1A6
1Y7	10		47		1A7
GND	11		46		GND
1Y8	12		45		1A8
1Y9	13		44		1A9
1Y10	14		43		1A10
2Y1	15		42		2A1
2Y2	16		41		2A2
2Y3	17		40		2A3
GND	18		39		GND
2Y4	19		38		2A4
2Y5	20		37		2A5
2Y6	21		36		2A6
V_{CC}	22		35		V_{CC}
2Y7	23		34		2A7
2Y8	24		33		2A8
GND	25		32		GND
2Y9	26		31		2A9
2Y10	27		30		2A10
2$\overline{OE1}$	28		29		2$\overline{OE2}$

description

The 'ALVTH162827 devices are 20-bit buffers/line drivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

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description (continued)

The devices are composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (1$\overline{\text{OE1}}$ and 1$\overline{\text{OE2}}$, or 2$\overline{\text{OE1}}$ and 2$\overline{\text{OE2}}$) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

All outputs are designed to sink up to 12 mA, and include equivalent 30-Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ALVTH162827 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALVTH162827 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
$\overline{\text{OE1}}$	$\overline{\text{OE2}}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic diagram (positive logic)
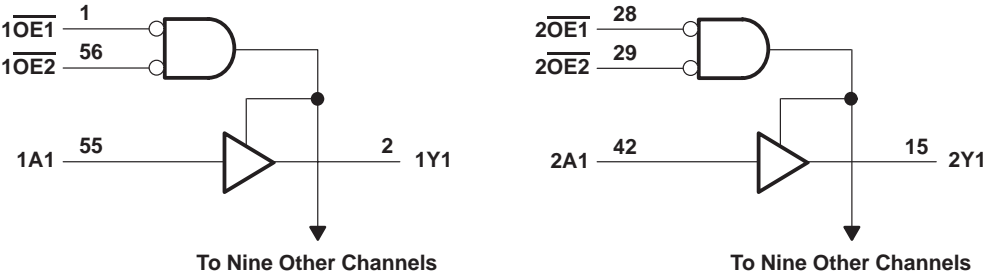
To Nine Other Channels   To Nine Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to 7 V
Output current in the low state, I_O: SN54ALVTH162827	96 mA
SN74ALVTH162827	128 mA
Output current in the high state, I_O: SN54ALVTH162827	–48 mA
SN74ALVTH162827	–64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions, V_{CC} = 2.5 V ± 0.2 V (see Note 3)

			SN54ALVTH162827			SN74ALVTH162827			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		2.3		2.7	2.3		2.7	V
V_{IH}	High-level input voltage		1.7			1.7			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_I	Input voltage		0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current				–6			–8	mA
I_{OL}	Low-level output current				8			12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			µs/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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recommended operating conditions, V_{CC} = 3.3 V $\pm$ 0.3 V (see Note 3)

			SN54ALVTH162827			SN74ALVTH162827			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		3		3.6	3		3.6	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input voltage		0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current				−8			−12	mA
I_{OL}	Low-level output current				8			12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			μs/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH162827			SN74ALVTH162827			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 2.3 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 2.3 V to 2.7 V,	I_{OH} = −100 µA	V_{CC}−0.2			V_{CC}−0.2			V
		V_{CC} = 2.3 V	I_{OH} = −6 mA	1.7						
			I_{OH} = −8 mA				1.7			
V_{OL}		V_{CC} = 2.3 V to 2.7 V,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 2.3 V	I_{OL} = 8 mA			0.7				
			I_{OL} = 12 mA						0.7	
I_I	Control inputs	V_{CC} = 2.7 V,	$V_I = V_{CC}$ or GND			±1			±1	µA
		V_{CC} = 0 or 2.7 V,	V_I = 5.5 V			10			10	
	Data inputs	V_{CC} = 2.7 V	V_I = 5.5 V			10			10	
			$V_I = V_{CC}$			1			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{BHL}‡		V_{CC} = 2.3 V,	V_I = 0.7 V		115			115		µA
I_{BHH}§		V_{CC} = 2.3 V,	V_I = 1.7 V		−10			−10		µA
I_{BHLO}¶		V_{CC} = 2.7 V,	V_I = 0 to V_{CC}	300			300			µA
I_{BHHO}#		V_{CC} = 2.7 V,	V_I = 0 to V_{CC}	−300			−300			µA
I_{EX}‖		V_{CC} = 2.3 V,	V_O = 5.5 V			125			125	µA
$I_{OZ(PU/PD)}$✮		V_{CC} ≤ 1.2 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{OZH}		V_{CC} = 2.7 V	V_O = 2.3 V, V_I = 0.7 V or 1.7 V			5			5	µA
I_{OZL}		V_{CC} = 2.7 V	V_O = 0.5 V, V_I = 0.7 V or 1.7 V			−5			−5	µA
I_{CC}		V_{CC} = 2.7 V, I_O = 0, $V_I = V_{CC}$ or GND	Outputs high		0.04	0.1		0.04	0.1	mA
			Outputs low		2.3	5		2.3	5	
			Outputs disabled		0.04	0.1		0.04	0.1	
C_i		V_{CC} = 2.5 V,	V_I = 2.5 V or 0		3.5			3.5		pF
C_o		V_{CC} = 2.5 V,	V_O = 2.5 V or 0		6			6		pF

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.
‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
¶ An external driver must source at least I_{BHLO} to switch this node from low to high.
# An external driver must sink at least I_{BHHO} to switch this node from high to low.
‖ Current into an output in the high state when $V_O > V_{CC}$
✮ High-impedance state during power up or power down

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH162827			SN74ALVTH162827			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 3 V to 3.6 V,	I_{OH} = −100 µA	V_{CC}−0.2			V_{CC}−0.2			V
		V_{CC} = 3 V	I_{OH} = −8 mA	2						
			I_{OH} = −12 mA				2			
V_{OL}		V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA			0.2			0.2	V
		V_{CC} = 3 V	I_{OL} = 8 mA			0.8				
			I_{OL} = 12 mA						0.8	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	Data inputs	V_{CC} = 3.6 V	V_I = 5.5 V			10			10	
			V_I = V_{CC}			1			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{BHL}‡		V_{CC} = 3 V,	V_I = 0.8 V	75			75			µA
I_{BHH}§		V_{CC} = 3 V,	V_I = 2 V	−75			−75			µA
I_{BHLO}¶		V_{CC} = 3.6 V,	V_I = 0 to V_{CC}	500			500			µA
I_{BHHO}#		V_{CC} = 3.6 V,	V_I = 0 to V_{CC}	−500			−500			µA
I_{EX}‖		V_{CC} = 3 V,	V_O = 5.5 V			125			125	µA
$I_{OZ(PU/PD)}$☆		$V_{CC} \leq$ 1.2 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{OZH}		V_{CC} = 3.6 V	V_O = 3 V, V_I = 0.8 V or 2 V			5			5	µA
I_{OZL}		V_{CC} = 3.6 V	V_O = 0.5 V, V_I = 0.8 V or 2 V			−5			−5	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high	0.07	0.1		0.07	0.1		mA
			Outputs low	3.2	5.5		3.2	5.5		
			Outputs disabled	0.07	0.1		0.07	0.1		
ΔI_{CC}□		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.4			0.4	mA
C_i		V_{CC} = 3.3 V,	V_I = 3.3 V or 0		3.5			3.5		pF
C_o		V_{CC} = 3.3 V,	V_O = 3.3 V or 0		6			6		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
¶ An external driver must source at least I_{BHLO} to switch this node from low to high.
# An external driver must sink at least I_{BHHO} to switch this node from high to low.
‖ Current into an output in the high state when $V_O > V_{CC}$
☆ High-impedance state during power up or power down
□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended operating free-air temperature range, C_L = 30 pF, V_{CC} = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH162827		SN74ALVTH162827		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.7	4.1	1.7	4.1	ns
t_{PHL}			1.6	4	1.6	4	
t_{PZH}	$\overline{OE}$	Y	2.1	4.8	2.1	4.8	ns
t_{PZL}			1.9	4.8	1.9	4.8	
t_{PHZ}	$\overline{OE}$	Y	2.4	6	2.4	6	ns
t_{PLZ}			1.7	5	1.7	5	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH162827		SN74ALVTH162827		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3.9	1	3.9	ns
t_{PHL}			1.5	3.7	1.5	3.7	
t_{PZH}	$\overline{OE}$	Y	1	5.6	1	5.6	ns
t_{PZL}			1.7	4.1	1.7	4.1	
t_{PHZ}	$\overline{OE}$	Y	3.6	6.3	3.6	6.3	ns
t_{PLZ}			1.7	5.1	1.7	5.1	

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PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V $\pm$ 0.2 V
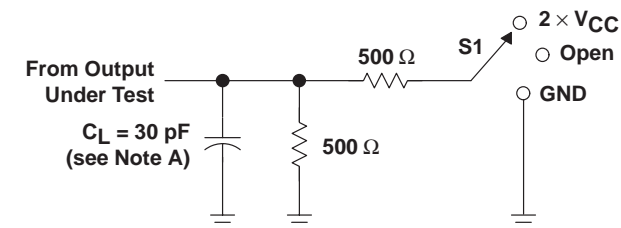
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**
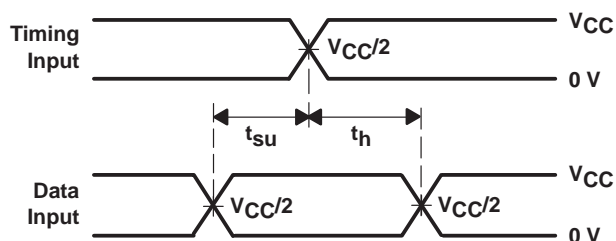
**VOLTAGE WAVEFORMS
PULSE DURATION**
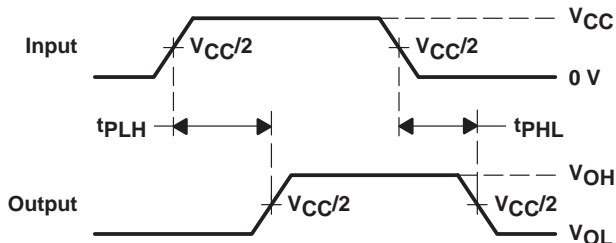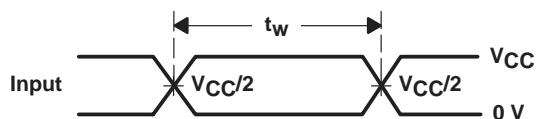
**VOLTAGE WAVEFORMS
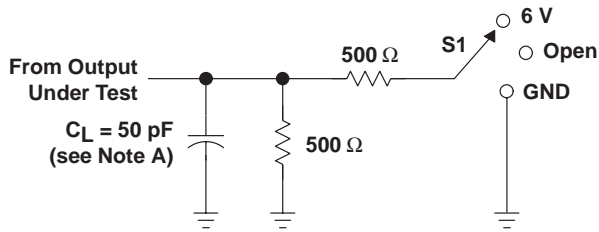PROPAGATION DELAY TIMES**
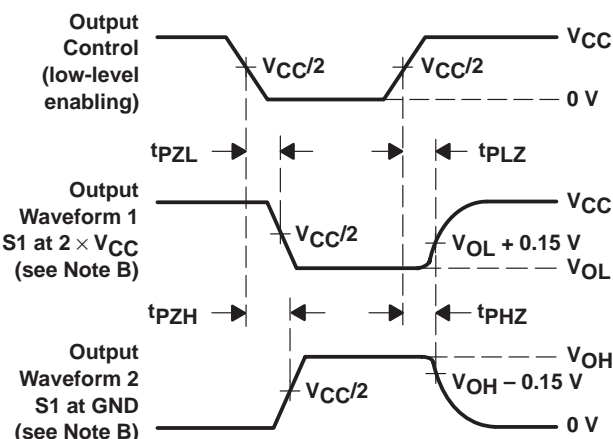
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2 ns, $t_f \leq$ 2 ns.
   D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V ± 0.3 V

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform22 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   D. The outputs are measured one at a time with one transition per measurement.
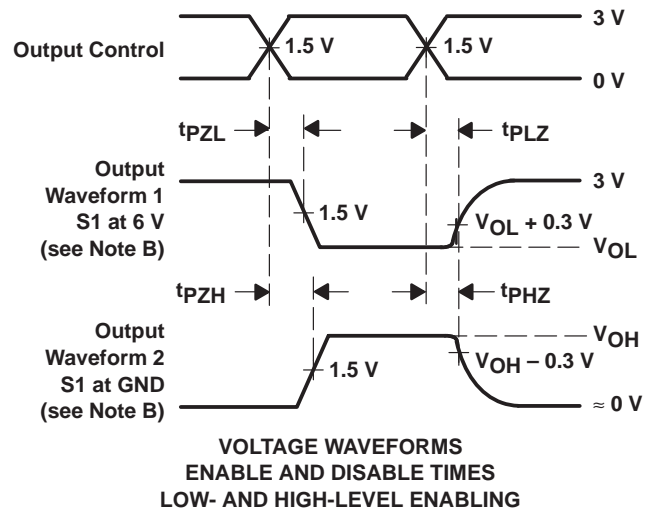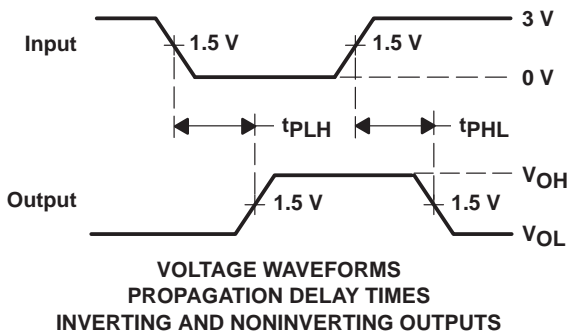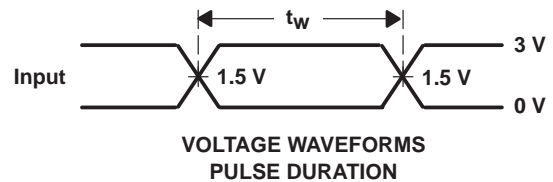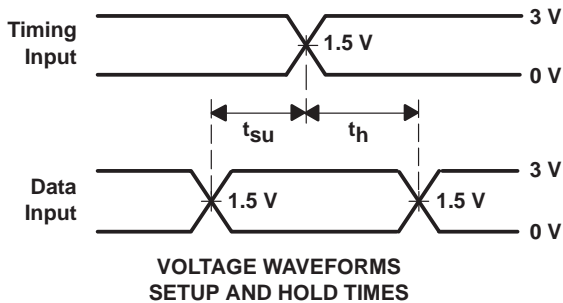
Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74ALVTH162827GRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH162827VRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH162827DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH162827GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH162827LR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH162827VR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G**) **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS **	14	16	20	24	38	48	56
DIM							
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

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MECHANICAL DATA

DL (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

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DGG (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

0,50

0,27 / 0,17 ⊕ 0,08 Ⓜ

48 25

6,20 / 6,00   8,30 / 7,90

0,15 NOM

Gage Plane

0,25

0°−8°

0,75 / 0,50

1 24

A

1,20 MAX

0,15 / 0,05

Seating Plane

△ 0,10

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
                            Post Office Box 655303 Dallas, Texas 75265