

# 74AVC16T245

16-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 6 — 9 September 2013

Product data sheet

## 1. General description

The 74AVC16T245 is a 16-bit transceiver with bidirectional level voltage translation and 3-state outputs. The device can be used as two 8-bit transceivers or as a 16-bit transceiver. It has dual supplies ( $V_{CC(A)}$  and  $V_{CC(B)}$ ) for voltage translation and four 8-bit input-output ports (nAn and nBn) each with its own output enable ( $\overline{nOE}$ ) and send/receive ( $nDIR$ ) input for direction control.  $V_{CC(A)}$  and  $V_{CC(B)}$  can be independently supplied at any voltage between 0.8 V and 3.6 V making the device suitable for low voltage translation between any of the following voltages: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V. A HIGH on  $nDIR$  selects transmission from nAn to nBn while a LOW on  $nDIR$  selects transmission from nBn to nAn. A HIGH on  $\overline{nOE}$  causes the outputs to assume a high-impedance OFF-state

The device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either  $V_{CC(A)}$  or  $V_{CC(B)}$  are at GND level, both nAn and nBn are in the high-impedance OFF-state.

## 2. Features and benefits

- Wide supply voltage range:
  - ◆  $V_{CC(A)}$ : 0.8 V to 3.6 V
  - ◆  $V_{CC(B)}$ : 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - ◆ JESD8-12 (0.8 V to 1.3 V)
  - ◆ JESD8-11 (0.9 V to 1.65 V)
  - ◆ JESD8-7 (1.2 V to 1.95 V)
  - ◆ JESD8-5 (1.8 V to 2.7 V)
  - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114F Class 3B exceeds 8000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101D exceeds 1000 V
- Maximum data rates:
  - ◆ 380 Mbit/s ( $\geq 1.8$  V to 3.3 V translation)
  - ◆ 200 Mbit/s ( $\geq 1.1$  V to 3.3 V translation)
  - ◆ 200 Mbit/s ( $\geq 1.1$  V to 2.5 V translation)
  - ◆ 200 Mbit/s ( $\geq 1.1$  V to 1.8 V translation)
  - ◆ 150 Mbit/s ( $\geq 1.1$  V to 1.5 V translation)



- ◆ 100 Mbit/s ( $\geq 1.1$  V to 1.2 V translation)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC16T245DGG	$-40$ °C to $+125$ °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74AVC16T245DGV	$-40$ °C to $+125$ °C	TSSOP48 <sup>[1]</sup>	plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm	SOT480-1
74AVC16T245EV	$-40$ °C to $+125$ °C	VFBGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body $4.5 \times 7 \times 0.65$ mm	SOT702-1
74AVC16T245BX	$-40$ °C to $+125$ °C	HXQFN60	plastic compatible thermal enhanced extremely thin quad flat package; no leads; 60 terminals; body $4 \times 6 \times 0.5$ mm	SOT1134-2

[1] Also known as TVSOP48.

### 4. Functional diagram

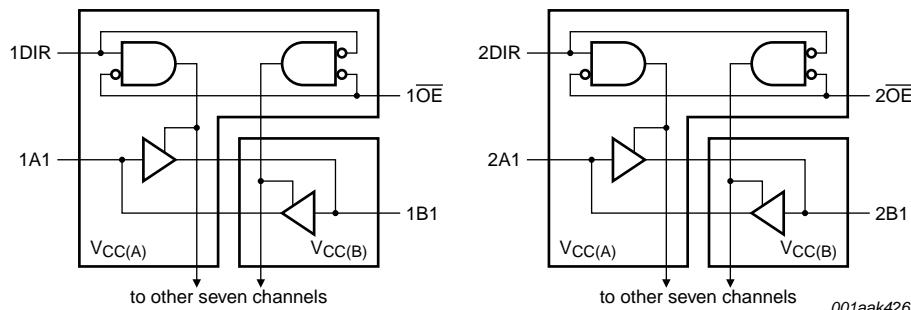


Fig 1. Logic diagram

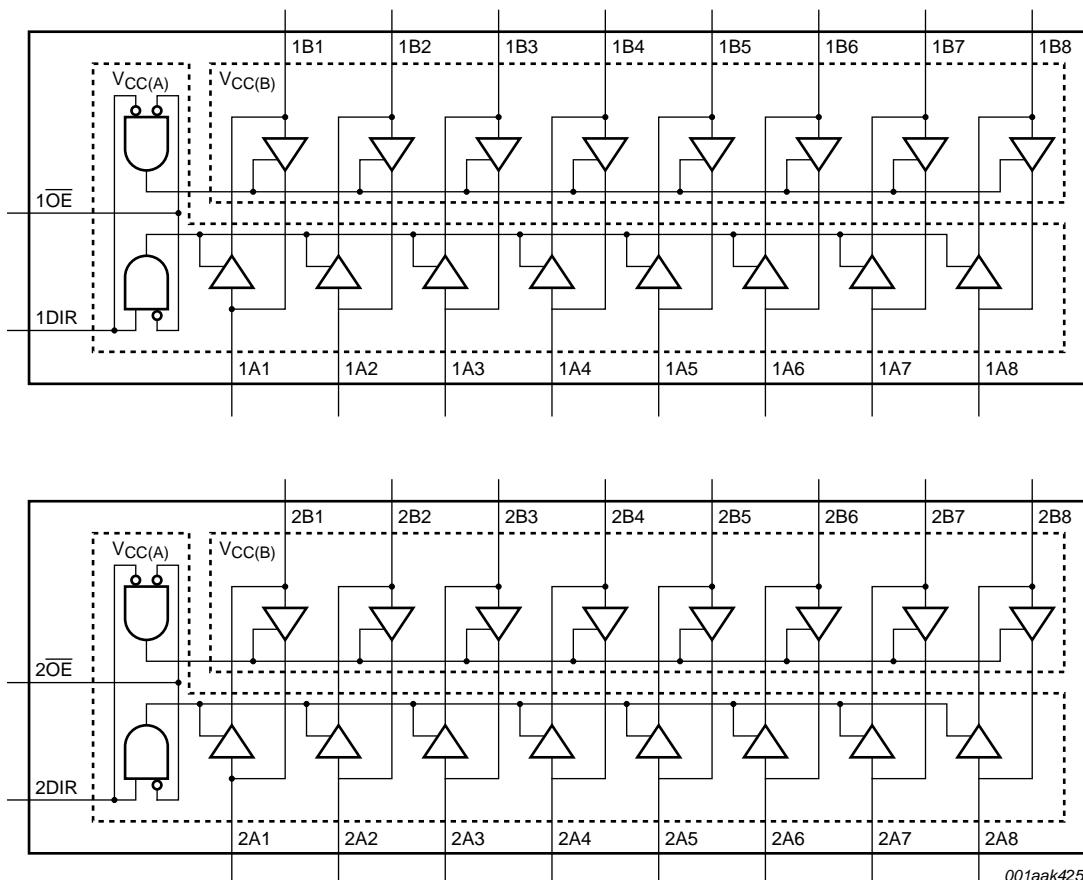


Fig 2. Logic symbol

## 5. Pinning information

### 5.1 Pinning

74AVC16T245	
1DIR	1
1B1	2
1B2	3
GND	4
1B3	5
1B4	6
V <sub>CC(B)</sub>	7
1B5	8
1B6	9
GND	10
1B7	11
1B8	12
2B1	13
2B2	14
GND	15
2B3	16
2B4	17
V <sub>CC(B)</sub>	18
2B5	19
2B6	20
GND	21
2B7	22
2B8	23
2DIR	24
	001aak427
	48
	1 $\bar{OE}$
	47
	1A1
	46
	1A2
	45
	GND
	44
	1A3
	43
	1A4
	42
	V <sub>CC(A)</sub>
	41
	1A5
	40
	1A6
	39
	GND
	38
	1A7
	37
	1A8
	36
	2A1
	35
	2A2
	34
	GND
	33
	2A3
	32
	2A4
	31
	V <sub>CC(A)</sub>
	30
	2A5
	29
	2A6
	28
	GND
	27
	2A7
	26
	2A8
	25
	2 $\bar{OE}$

ball A1  
index area

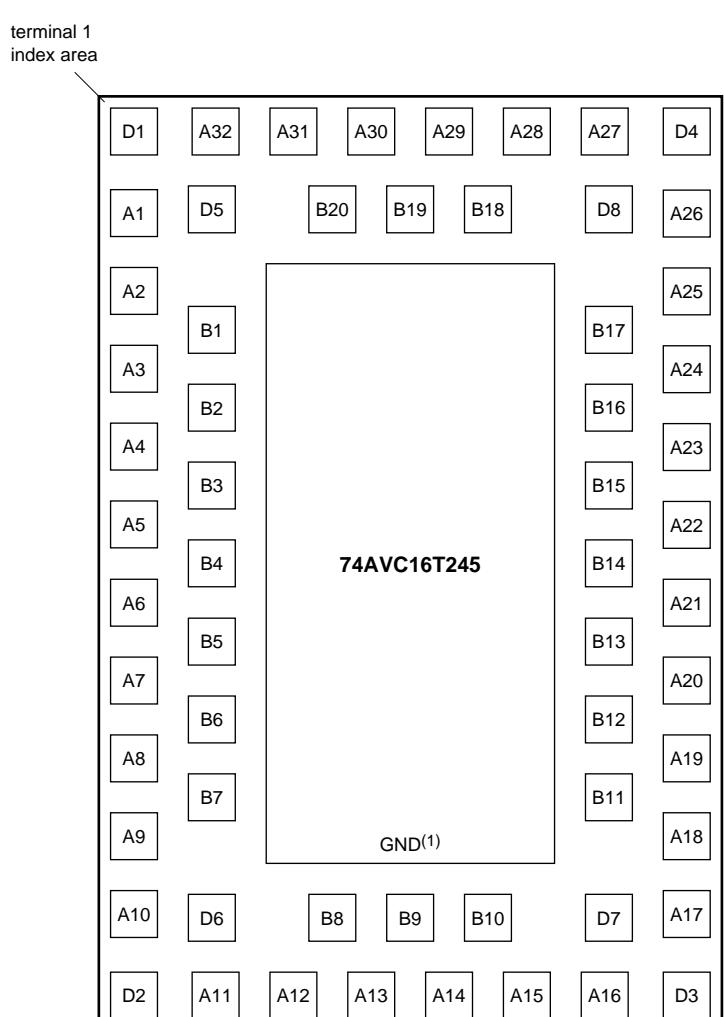
74AVC16T245

001aak428

Transparent top view

Fig 3. Pin configuration SOT362-1 and SOT480-1 (TSSOP48)

Fig 4. Pin configuration SOT702-1 (VFBGA56)



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

**Fig 5. Pin configuration SOT1134-2 (HXQFN60)**

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin				Description
		SOT362-1 and SOT480-1	SOT702-1	SOT1134-2	
1DIR, 2DIR	1, 24		A1, K1	A30, A13	direction control
1B1 to 1B8	2, 3, 5, 6, 8, 9, 11, 12		B2, B1, C2, C1, D2, D1, E2, E1	B20, A31, D5, D1, A2, B2, B3, A5	data input or output
2B1 to 2B8	13, 14, 16, 17, 19, 20, 22, 23		F1, F2, G1, G2, H1, H2, J1, J2	A6, B5, B6, A9, D2, D6, A12, B8	data input or output
GND <sup>[1]</sup>	4, 10, 15, 21, 28, 34, 39, 45		B3, D3, G3, J3, J4, G4, D4, B4	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)
V <sub>CC(B)</sub>	7, 18		C3, H3	A1, A10	supply voltage B (nBn inputs are referenced to V <sub>CC(B)</sub> )
1OE, 2OE	48, 25		A6, K6	A29, A14	output enable input (active LOW)
1A1 to 1A8	47, 46, 44, 43, 41, 40, 38, 37		B5, B6, C5, C6, D5, D6, E5, E6	B18, A28, D8, D4, A25, B16, B15, A22	data input or output
2A1 to 2A8	36, 35, 33, 32, 30, 29, 27, 26		F6, F5, G6, G5, H6, H5, J6, J5	A21, B13, B12, A18, D3, D7, A15, B10	data input or output
V <sub>CC(A)</sub>	31, 42		C4, H4	A17, A26	supply voltage A (nAn, nOE and nDIR inputs are referenced to V <sub>CC(A)</sub> )
n.c.	-		A2, A3, A4, A5, K2, K3, K4, K5	A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19	not connected

[1] All GND pins must be connected to ground (0 V).

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Supply voltage	Input	Input/output <sup>[3]</sup>		
V <sub>CC(A)</sub> , V <sub>CC(B)</sub>	nOE <sup>[2]</sup>	nDIR <sup>[2]</sup>	nAn <sup>[2]</sup>	nBn <sup>[2]</sup>
0.8 V to 3.6 V	L	L	nAn = nBn	input
0.8 V to 3.6 V	L	H	input	nBn = nAn
0.8 V to 3.6 V	H	X	Z	Z
GND <sup>[3]</sup>	X	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The nAn, nDIR and nOE input circuit is referenced to V<sub>CC(A)</sub>; The nBn input circuit is referenced to V<sub>CC(B)</sub>.

[3] If at least one of V<sub>CC(A)</sub> or V<sub>CC(B)</sub> is at GND level, the device goes into suspend mode.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V	
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V	
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA	
$V_I$	input voltage		[1]	-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA	
$V_O$	output voltage	Active mode	[1][2][3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode	[1]	-0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$	[2]	-	$\pm 50$	mA
$I_{CC}$	supply current	per $V_{CC(A)}$ or $V_{CC(B)}$ pin	-	100	mA	
$I_{GND}$	ground current	per GND pin	-100	-	mA	
$T_{stg}$	storage temperature		-65	+150	°C	
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C; TSSOP48 package VFBGA56 package HXQFN60 package	[4]	-	500	mW
			[5]	-	1000	mW
			[5]	-	1000	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

[3]  $V_{CCO} + 0.5$  V should not exceed 4.6 V.

[4] Above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

[5] Above 70 °C the value of  $P_{tot}$  derates linearly with 1.8 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{CC(A)}$	supply voltage A		0.8	3.6	V	
$V_{CC(B)}$	supply voltage B		0.8	3.6	V	
$V_I$	input voltage		0	3.6	V	
$V_O$	output voltage	Active mode	[1]	0	$V_{CCO}$	V
		Suspend or 3-state mode	0	3.6	V	
$T_{amb}$	ambient temperature		-40	+125	°C	
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8$ V to 3.6 V	[2]	-	5	ns/V

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the input port.

## 9. Static characteristics

**Table 6. Typical static characteristics at  $T_{amb} = 25^{\circ}\text{C}$** <sup>[1][2]</sup>

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ $I_O = -1.5 \text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$	-	0.69	-	V	
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ $I_O = 1.5 \text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$	-	0.07	-	V	
$I_I$	input leakage current	nDIR, nOE input; $V_I = 0 \text{ V}$ or $3.6 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8 \text{ V}$ to $3.6 \text{ V}$	-	$\pm 0.025$	$\pm 0.25$	$\mu\text{A}$	
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0 \text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = V_{CC(B)} = 3.6 \text{ V}$	[3]	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode A port; $V_O = 0 \text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = 3.6 \text{ V}$ ; $V_{CC(B)} = 0 \text{ V}$		-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode B port; $V_O = 0 \text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = 0 \text{ V}$ ; $V_{CC(B)} = 3.6 \text{ V}$		-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0 \text{ V}$ to $3.6 \text{ V}$ ; $V_{CC(A)} = 0 \text{ V}$ ; $V_{CC(B)} = 0.8 \text{ V}$ to $3.6 \text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$	
		B port; $V_I$ or $V_O = 0 \text{ V}$ to $3.6 \text{ V}$ ; $V_{CC(B)} = 0 \text{ V}$ ; $V_{CC(A)} = 0.8 \text{ V}$ to $3.6 \text{ V}$		-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	nDIR, nOE input; $V_I = 0 \text{ V}$ or $3.3 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3 \text{ V}$	-	2.0	-	pF	
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3 \text{ V}$ or $0 \text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3 \text{ V}$	-	4.5	-	pF	

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

**Table 7. Static characteristics**<sup>[1][2]</sup>

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	data input					
		$V_{CCI} = 0.8 \text{ V}$	0.70 $V_{CCI}$	-	0.70 $V_{CCI}$	-	V
		$V_{CCI} = 1.1 \text{ V}$ to $1.95 \text{ V}$	0.65 $V_{CCI}$	-	0.65 $V_{CCI}$	-	V
		$V_{CCI} = 2.3 \text{ V}$ to $2.7 \text{ V}$	1.6	-	1.6	-	V
		$V_{CCI} = 3.0 \text{ V}$ to $3.6 \text{ V}$	2	-	2	-	V
		nDIR, nOE input					
		$V_{CC(A)} = 0.8 \text{ V}$	0.70 $V_{CC(A)}$	-	0.70 $V_{CC(A)}$	-	V
		$V_{CC(A)} = 1.1 \text{ V}$ to $1.95 \text{ V}$	0.65 $V_{CC(A)}$	-	0.65 $V_{CC(A)}$	-	V
		$V_{CC(A)} = 2.3 \text{ V}$ to $2.7 \text{ V}$	1.6	-	1.6	-	V
		$V_{CC(A)} = 3.0 \text{ V}$ to $3.6 \text{ V}$	2	-	2	-	V

Table 7. Static characteristics ...continued<sup>[1][2]</sup>

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Max	Min	Max		
V <sub>IL</sub>	LOW-level input voltage	data input						
		V <sub>CCI</sub> = 0.8 V	-	0.30V <sub>CCI</sub>	-	0.30V <sub>CCI</sub>	V	
		V <sub>CCI</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CCI</sub>	-	0.35V <sub>CCI</sub>	V	
		V <sub>CCI</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V	
		V <sub>CCI</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V	
		nDIR, nOE input						
		V <sub>CC(A)</sub> = 0.8 V	-	0.30V <sub>CC(A)</sub>	-	0.30V <sub>CC(A)</sub>	V	
		V <sub>CC(A)</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CC(A)</sub>	-	0.35V <sub>CC(A)</sub>	V	
		V <sub>CC(A)</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V	
		V <sub>CC(A)</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	V <sub>CCO</sub> - 0.1	-	V <sub>CCO</sub> - 0.1	-	V	
		I <sub>O</sub> = -3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	0.85	-	0.85	-	V	
		I <sub>O</sub> = -6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	1.05	-	1.05	-	V	
		I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	1.2	-	1.2	-	V	
		I <sub>O</sub> = -9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	1.75	-	1.75	-	V	
		I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	2.3	-	2.3	-	V	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	0.1	-	0.1	V	
		I <sub>O</sub> = 3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	-	0.25	-	0.25	V	
		I <sub>O</sub> = 6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-	0.35	-	0.35	V	
		I <sub>O</sub> = 8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-	0.45	-	0.45	V	
		I <sub>O</sub> = 9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-	0.55	-	0.55	V	
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-	0.7	-	0.7	V	
I <sub>I</sub>	input leakage current	nDIR, nOE input; V <sub>I</sub> = 0 V or 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±1	-	±5	μA	
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V	[3]	-	±5	-	±30	μA
		suspend mode A port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	[3]	-	±5	-	±30	μA
		suspend mode B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	[3]	-	±5	-	±30	μA

**Table 7. Static characteristics ...continued<sup>[1][2]</sup>**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	µA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	µA
I <sub>CC</sub>	supply current	A port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	30	-	125	µA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	25	-	100	µA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	25	-	100	µA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-5	-	-20	-	µA
		B port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	30	-	125	µA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	25	-	100	µA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-5	-	-20	-	µA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-	25	-	100	µA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	55	-	185	µA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	45	-	150	µA

[1] V<sub>CCO</sub> is the supply voltage associated with the output port.[2] V<sub>CCI</sub> is the supply voltage associated with the data input port.[3] For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.**Table 8. Typical total supply current (I<sub>CC(A)</sub> + I<sub>CC(B)</sub>)**

V <sub>CC(A)</sub>	V <sub>CC(B)</sub>								Unit
		0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0	0.1	0.1	0.1	0.1	0.1	0.1	µA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.3	1.6	µA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.8	µA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.4	µA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.2	µA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	0.1	µA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	0.1	µA

## 10. Dynamic characteristics

**Table 9. Typical power dissipation capacitance at  $V_{CC(A)} = V_{CC(B)}$  and  $T_{amb} = 25^\circ C$  [1][2]**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C <sub>PD</sub>	power dissipation capacitance	A port: (direction nAn to nBn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nAn to nBn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nBn to nAn); output enabled	9	9.7	9.8	10.3	11.7	13.7	pF
		A port: (direction nBn to nAn); output disabled	0.6	0.6	0.6	0.7	0.7	0.7	pF
		B port: (direction nAn to nBn); output enabled	9	9.7	9.8	10.3	11.7	13.7	pF
		B port: (direction nAn to nBn); output disabled	0.6	0.6	0.6	0.7	0.7	0.7	pF
		B port: (direction nBn to nAn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction nBn to nAn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu W$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

[2] f<sub>i</sub> = 10 MHz; V<sub>i</sub> = GND to V<sub>CC</sub>; t<sub>r</sub> = t<sub>f</sub> = 1 ns; C<sub>L</sub> = 0 pF; R<sub>L</sub> =  $\infty \Omega$ .

**Table 10. Typical dynamic characteristics at  $V_{CC(A)} = 0.8$  V and  $T_{amb} = 25$  °C [1]**Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	nAn to nBn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		nBn to nAn	14.4	12.4	12.1	11.9	11.8	11.8	ns
$t_{dis}$	disable time	nOE to nAn	16.2	16.2	16.2	16.2	16.2	16.2	ns
		nOE to nBn	17.6	10.0	9.0	9.1	8.7	9.3	ns
$t_{en}$	enable time	nOE to nAn	21.9	21.9	21.9	21.9	21.9	21.9	ns
		nOE to nBn	22.2	11.1	9.8	9.4	9.4	9.6	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .**Table 11. Typical dynamic characteristics at  $V_{CC(B)} = 0.8$  V and  $T_{amb} = 25$  °C [1]**Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	nAn to nBn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		nBn to nAn	14.4	7.0	6.2	6.0	5.9	6.0	ns
$t_{dis}$	disable time	nOE to nAn	16.2	5.9	4.4	4.2	3.1	3.5	ns
		nOE to nBn	17.6	14.2	13.7	13.6	13.3	13.1	ns
$t_{en}$	enable time	nOE to nAn	21.9	6.4	4.4	3.5	2.6	2.3	ns
		nOE to nBn	22.2	17.7	17.2	17.0	16.8	16.7	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

Table 12. Dynamic characteristics for temperature range  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  [1]Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#).

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit	
			1.2 V $\pm$ 0.1 V		1.5 V $\pm$ 0.1 V		1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.2	0.5	6.9	0.5	6.0	0.5	5.1	0.5	4.9	ns	
		nBn to nAn	0.5	9.2	0.5	8.7	0.5	8.5	0.5	8.2	0.5	8.0	ns	
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	11.6	1.5	11.6	1.5	11.6	1.5	11.6	1.5	11.6	ns	
		n $\overline{\text{OE}}$ to nBn	1.5	12.5	1.5	9.7	1.5	9.5	1.0	8.1	1.0	8.9	ns	
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	14.5	1.0	14.5	1.0	14.5	1.0	14.5	1.0	14.5	ns	
		n $\overline{\text{OE}}$ to nBn	1.1	14.9	1.1	11.0	1.1	9.6	1.0	8.1	1.0	7.7	ns	
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.7	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	ns	
		nBn to nAn	0.5	6.9	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	ns	
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	ns	
		n $\overline{\text{OE}}$ to nBn	1.5	11.4	1.5	8.7	1.5	7.5	1.0	6.5	1.0	6.3	ns	
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	10.1	1.0	10.1	1.0	10.1	1.0	10.1	1.0	10.1	ns	
		n $\overline{\text{OE}}$ to nBn	1.0	13.5	1.0	10.1	0.5	8.1	0.5	5.9	0.5	5.2	ns	
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.5	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	ns	
		nBn to nAn	0.5	6.0	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	ns	
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	ns	
		n $\overline{\text{OE}}$ to nBn	1.5	11.1	1.5	8.4	1.5	7.1	1.0	5.9	1.0	5.7	ns	
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	ns	
		n $\overline{\text{OE}}$ to nBn	1.0	13.0	1.0	9.2	0.5	7.4	0.5	5.3	0.5	4.5	ns	
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.2	0.5	5.6	0.5	4.6	0.5	3.3	0.5	2.8	ns	
		nBn to nAn	0.5	5.1	0.5	4.1	0.5	3.7	0.5	3.4	0.5	3.2	ns	
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.0	6.1	1.0	6.1	1.0	6.1	1.0	6.1	1.0	6.1	ns	
		n $\overline{\text{OE}}$ to nBn	1.0	10.6	1.0	7.9	1.0	6.6	1.0	6.1	1.0	5.2	ns	
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns	
		n $\overline{\text{OE}}$ to nBn	0.5	12.5	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	ns	
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.0	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	ns	
		nBn to nAn	0.5	4.9	0.5	3.7	0.5	3.3	0.5	2.9	0.5	2.7	ns	
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	ns	
		n $\overline{\text{OE}}$ to nBn	1.0	10.3	1.0	7.7	1.0	6.5	1.0	5.2	0.5	5.0	ns	
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	4.3	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4.0	ns	
		n $\overline{\text{OE}}$ to nBn	0.5	12.4	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4.0	ns	

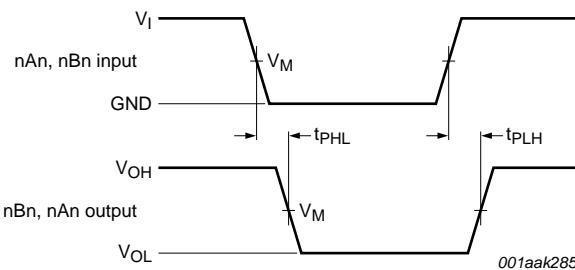
[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

Table 13. Dynamic characteristics for temperature range  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  [1]Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit	
			1.2 V $\pm$ 0.1 V		1.5 V $\pm$ 0.1 V		1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
<b>V<sub>CC(A)</sub> = 1.1 V to 1.3 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	10.2	0.5	7.6	0.5	6.6	0.5	5.7	0.5	5.4	ns	
		nBn to nAn	0.5	10.2	0.5	9.6	0.5	9.4	0.5	9.1	0.5	8.8	ns	
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	12.8	1.5	12.8	1.5	12.8	1.5	12.8	1.5	12.8	ns	
		n $\overline{\text{OE}}$ to nBn	1.5	13.8	1.5	10.7	1.5	10.5	1.0	9.0	1.5	9.8	ns	
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	16.0	1.0	16.0	1.0	16.0	1.0	16.0	1.0	16.0	ns	
		n $\overline{\text{OE}}$ to nBn	1.1	16.4	1.1	12.1	1.1	10.6	1.0	9.0	1.0	8.5	ns	
<b>V<sub>CC(A)</sub> = 1.4 V to 1.6 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.6	0.5	6.9	0.5	5.8	0.5	4.6	0.5	4.1	ns	
		nBn to nAn	0.5	7.6	0.5	6.9	0.5	6.5	0.5	6.2	0.5	6.1	ns	
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	10.1	1.5	10.1	1.5	10.1	1.5	10.1	1.5	10.1	ns	
		n $\overline{\text{OE}}$ to nBn	1.5	12.6	1.5	9.6	1.5	8.3	1.0	7.2	1.0	7.0	ns	
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	11.2	1.0	11.2	1.0	11.2	1.0	11.2	1.0	11.2	ns	
		n $\overline{\text{OE}}$ to nBn	1.0	14.9	1.0	11.2	0.5	9.0	0.5	6.5	0.5	5.8	ns	
<b>V<sub>CC(A)</sub> = 1.65 V to 1.95 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.4	0.5	6.5	0.5	5.3	0.5	4.1	0.5	3.7	ns	
		nBn to nAn	0.5	6.6	0.5	5.8	0.5	5.3	0.5	5.0	0.5	4.9	ns	
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	1.5	8.5	ns	
		n $\overline{\text{OE}}$ to nBn	1.5	12.3	1.5	9.3	1.5	7.9	1.0	6.5	1.0	6.3	ns	
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	8.6	1.0	8.6	1.0	8.6	1.0	8.6	1.0	8.6	ns	
		n $\overline{\text{OE}}$ to nBn	1.0	14.3	1.0	10.2	0.5	8.2	0.5	5.9	0.5	5.0	ns	
<b>V<sub>CC(A)</sub> = 2.3 V to 2.7 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.1	0.5	6.2	0.5	5.1	0.5	3.7	0.5	3.1	ns	
		nBn to nAn	0.5	5.7	0.5	4.6	0.5	4.1	0.5	3.8	0.5	3.6	ns	
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	ns	
		n $\overline{\text{OE}}$ to nBn	1.0	11.7	1.0	8.7	1.0	7.3	1.0	6.8	1.0	5.8	ns	
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	5.9	0.5	5.9	0.5	5.9	0.5	5.9	0.5	5.9	ns	
		n $\overline{\text{OE}}$ to nBn	0.5	13.8	0.5	10.4	0.5	8.1	0.5	5.7	0.5	5.0	ns	
<b>V<sub>CC(A)</sub> = 3.0 V to 3.6 V</b>														
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.8	0.5	6.1	0.5	4.9	0.5	3.6	0.5	3.0	ns	
		nBn to nAn	0.5	5.4	0.5	4.1	0.5	3.7	0.5	3.2	0.5	3.0	ns	
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	0.5	5.5	0.5	5.5	0.5	5.5	0.5	5.5	0.5	5.5	ns	
		n $\overline{\text{OE}}$ to nBn	1.0	11.4	1.0	8.5	1.0	7.2	1.0	5.8	0.5	5.5	ns	
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	4.8	0.5	4.8	0.5	4.7	0.5	4.6	0.5	4.4	ns	
		n $\overline{\text{OE}}$ to nBn	0.5	13.7	0.5	10.3	0.5	8.0	0.5	5.4	0.5	4.4	ns	

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

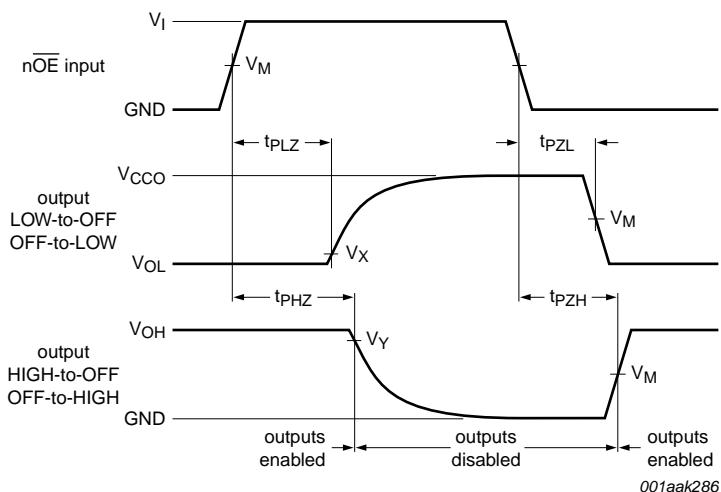
## 11. Waveforms



Measurement points are given in [Table 14](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times**



Measurement points are given in [Table 14](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

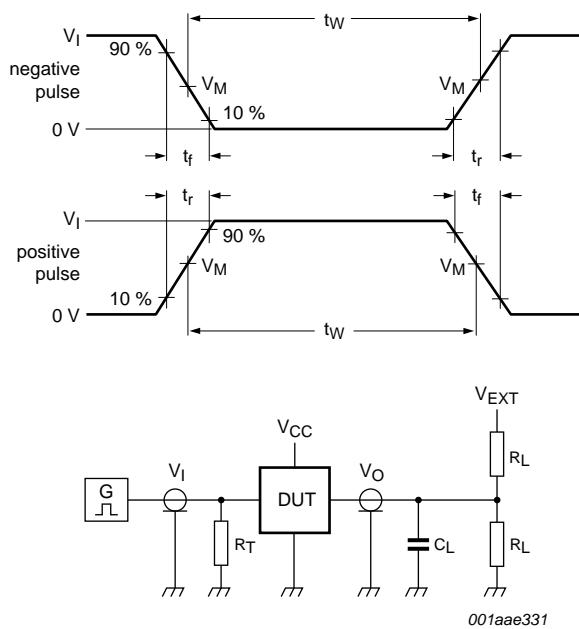
**Fig 7. Enable and disable times**

**Table 14. Measurement points**

Supply voltage	Input <sup>[1]</sup>	Output <sup>[2]</sup>		
$V_{CC(A)}, V_{CC(B)}$	$V_M$	$V_M$	$V_X$	$V_Y$
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1$ V	$V_{OH} - 0.1$ V
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.



Test data is given in [Table 15](#).

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 8. Test circuit for measuring switching times**

**Table 15. Test data**

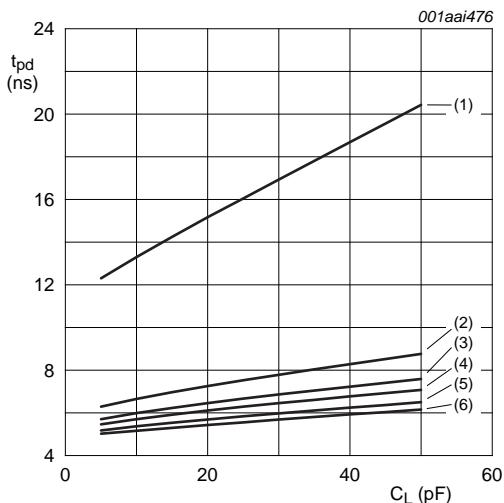
Supply voltage	Input	Load		$V_{EXT}$			
$V_{CC(A)}, V_{CC(B)}$	$V_I^{[1]}$	$\Delta t/\Delta V^{[2]}$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}^{[3]}$
0.8 V to 1.6 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CC0}$
1.65 V to 2.7 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CC0}$
3.0 V to 3.6 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CC0}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

[2]  $dV/dt \geq 1.0 \text{ V/ns}$

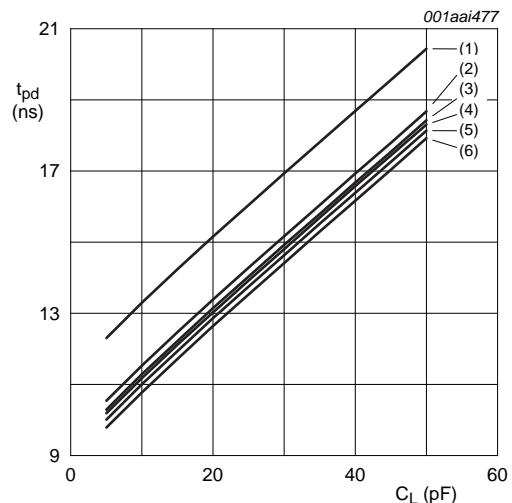
[3]  $V_{CC0}$  is the supply voltage associated with the output port.

## 12. Typical propagation delay characteristics



a. Propagation delay (nAn to nBn);  $V_{CC(A)} = 0.8$  V

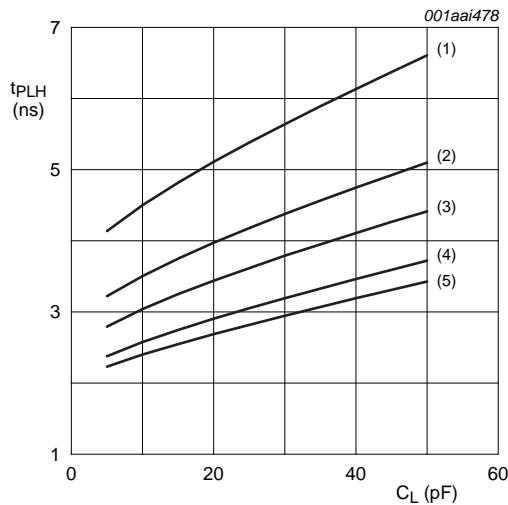
- (1)  $V_{CC(B)} = 0.8$  V.
- (2)  $V_{CC(B)} = 1.2$  V.
- (3)  $V_{CC(B)} = 1.5$  V.
- (4)  $V_{CC(B)} = 1.8$  V.
- (5)  $V_{CC(B)} = 2.5$  V.
- (6)  $V_{CC(B)} = 3.3$  V.



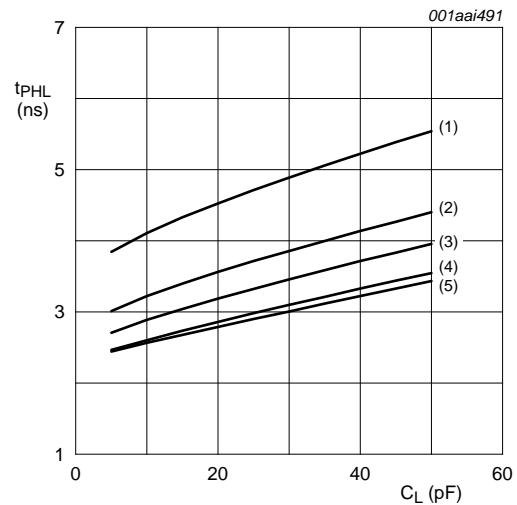
b. Propagation delay (nAn to nBn);  $V_{CC(B)} = 0.8$  V

- (1)  $V_{CC(A)} = 0.8$  V.
- (2)  $V_{CC(A)} = 1.2$  V.
- (3)  $V_{CC(A)} = 1.5$  V.
- (4)  $V_{CC(A)} = 1.8$  V.
- (5)  $V_{CC(A)} = 2.5$  V.
- (6)  $V_{CC(A)} = 3.3$  V.

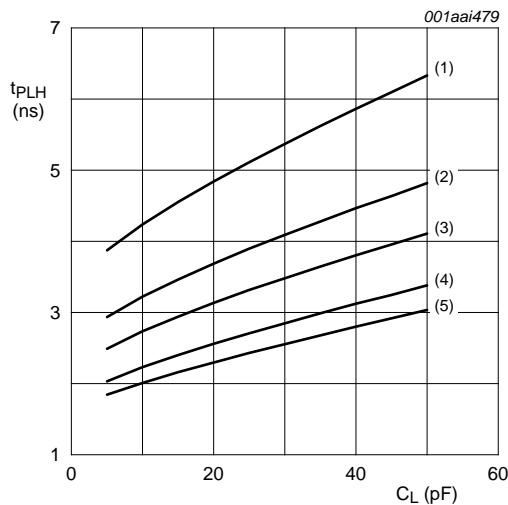
Fig 9. Typical propagation delay versus load capacitance;  $T_{amb} = 25$  °C



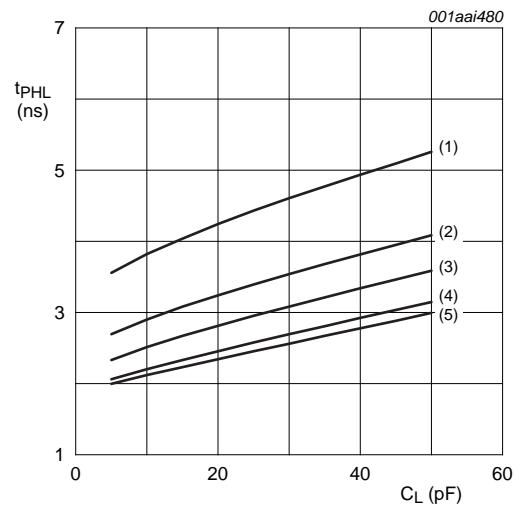
a. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.2$  V



b. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.2$  V



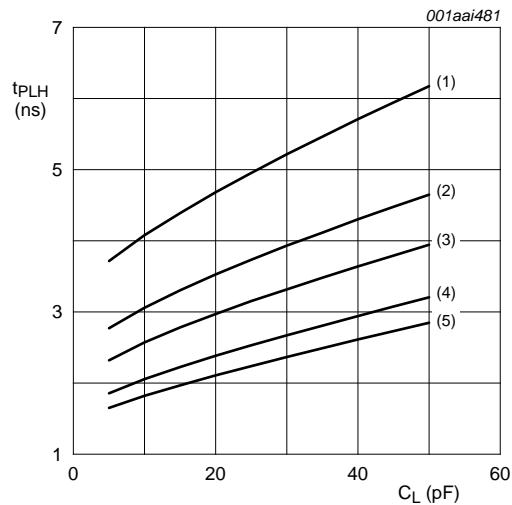
c. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.5$  V



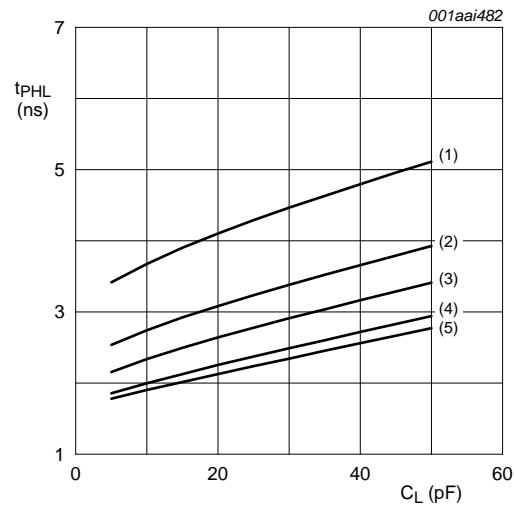
d. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.5$  V

(1)  $V_{CC(B)} = 1.2$  V.  
(2)  $V_{CC(B)} = 1.5$  V.  
(3)  $V_{CC(B)} = 1.8$  V.  
(4)  $V_{CC(B)} = 2.5$  V.  
(5)  $V_{CC(B)} = 3.3$  V.

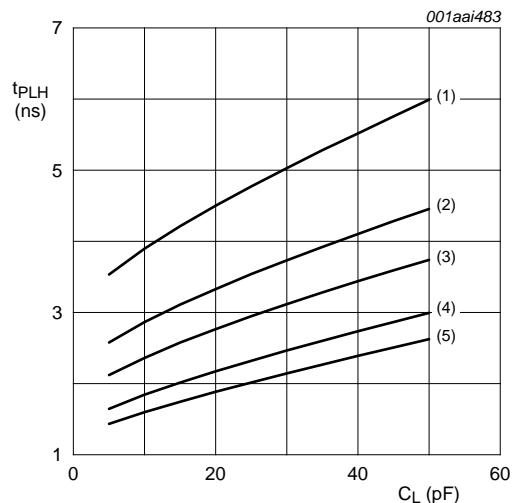
Fig 10. Typical propagation delay versus load capacitance;  $T_{amb} = 25$  °C



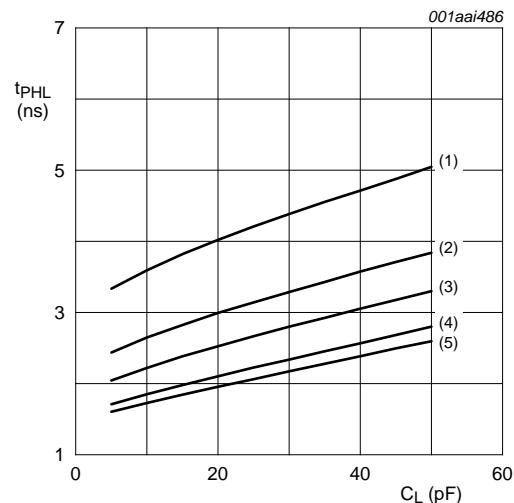
a. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.8$  V



b. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.8$  V



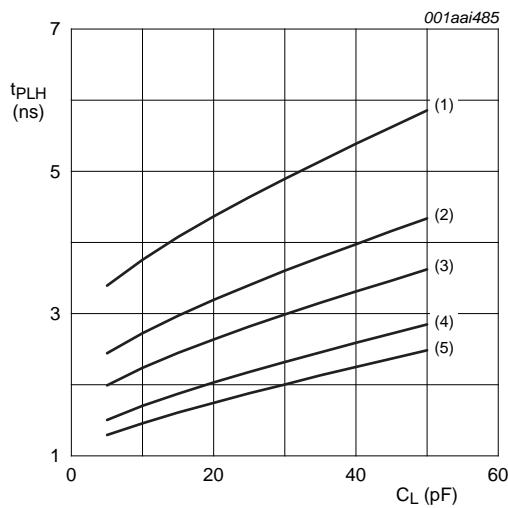
c. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 2.5$  V



d. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 2.5$  V

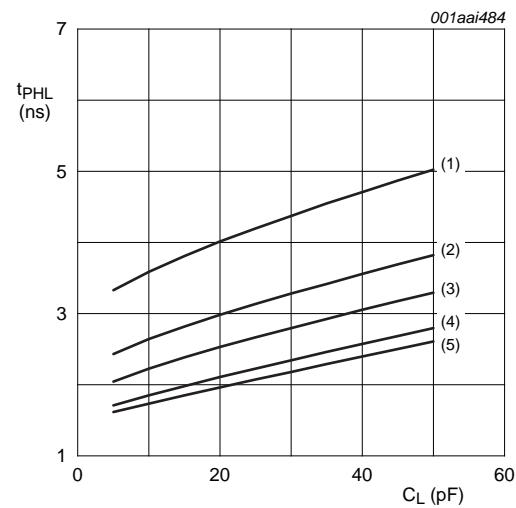
(1)  $V_{CC(B)} = 1.2$  V.  
(2)  $V_{CC(B)} = 1.5$  V.  
(3)  $V_{CC(B)} = 1.8$  V.  
(4)  $V_{CC(B)} = 2.5$  V.  
(5)  $V_{CC(B)} = 3.3$  V.

Fig 11. Typical propagation delay versus load capacitance;  $T_{amb} = 25$  °C



a. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 3.3$  V

- (1)  $V_{CC(B)} = 1.2$  V.
- (2)  $V_{CC(B)} = 1.5$  V.
- (3)  $V_{CC(B)} = 1.8$  V.
- (4)  $V_{CC(B)} = 2.5$  V.
- (5)  $V_{CC(B)} = 3.3$  V.



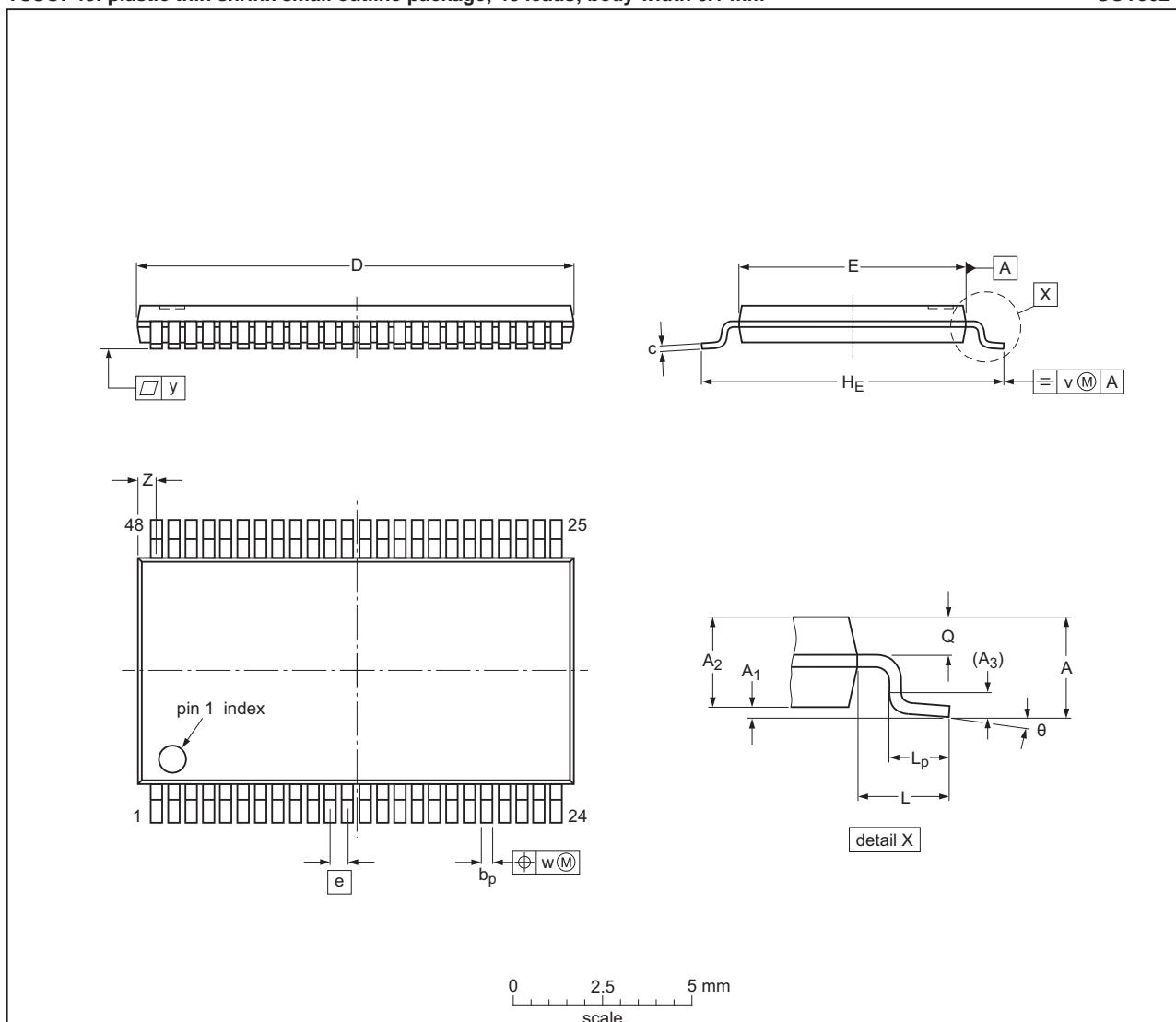
b. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 3.3$  V

Fig 12. Typical propagation delay versus load capacitance;  $T_{amb} = 25$  °C

## 13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	max	0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50			0.8	8°	
mm	nom	1.2		0.25					0.5		1			0.25	0.08	0.1		
mm	min	0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35			0.4	0°	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				03-02-19- 13-08-05

Fig 13. Package outline SOT362-1 (TSSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads;  
body width 4.4 mm; lead pitch 0.4 mm

SOT480-1

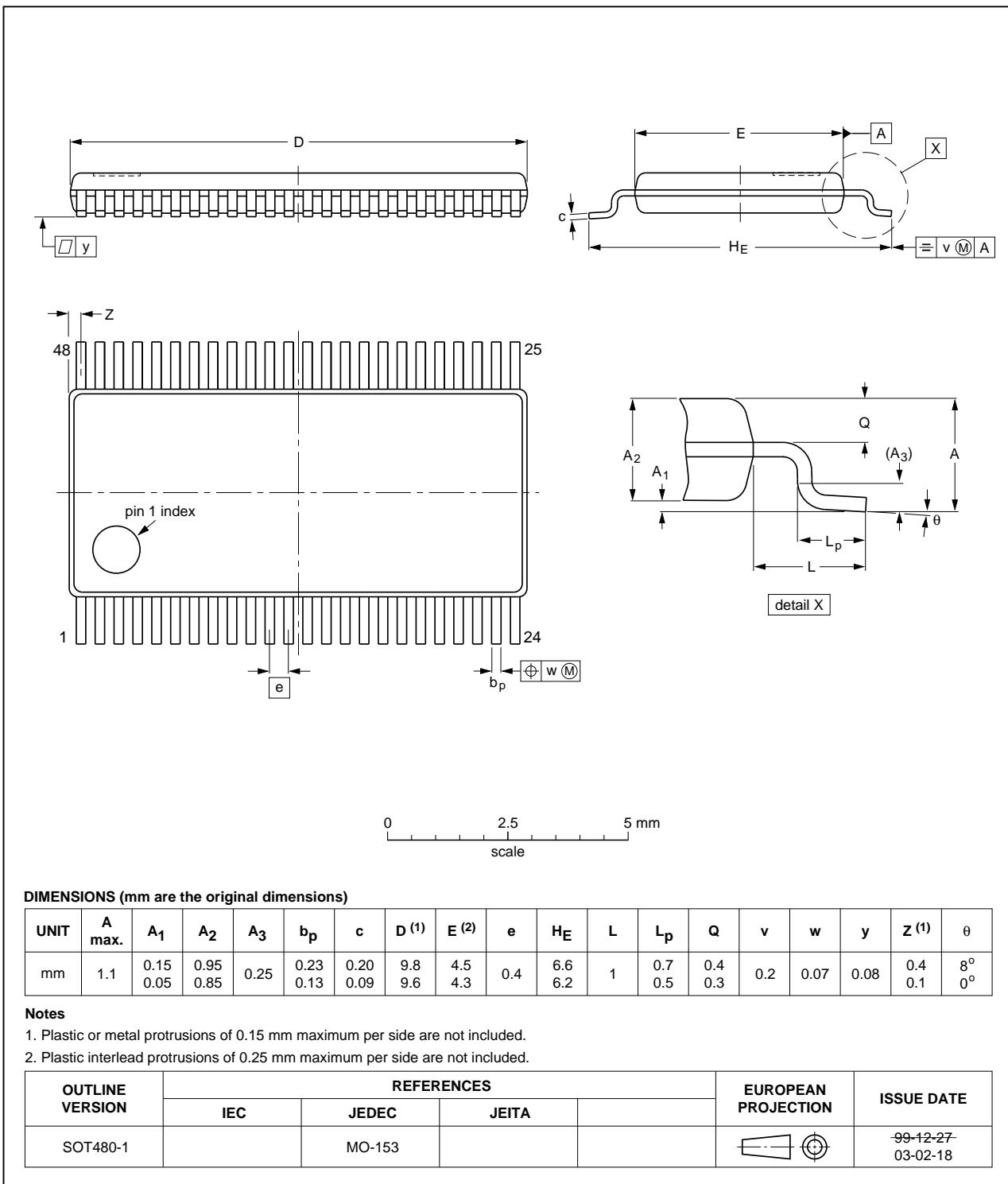


Fig 14. Package outline SOT480-1 (TSSOP48)

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm

SOT702-1

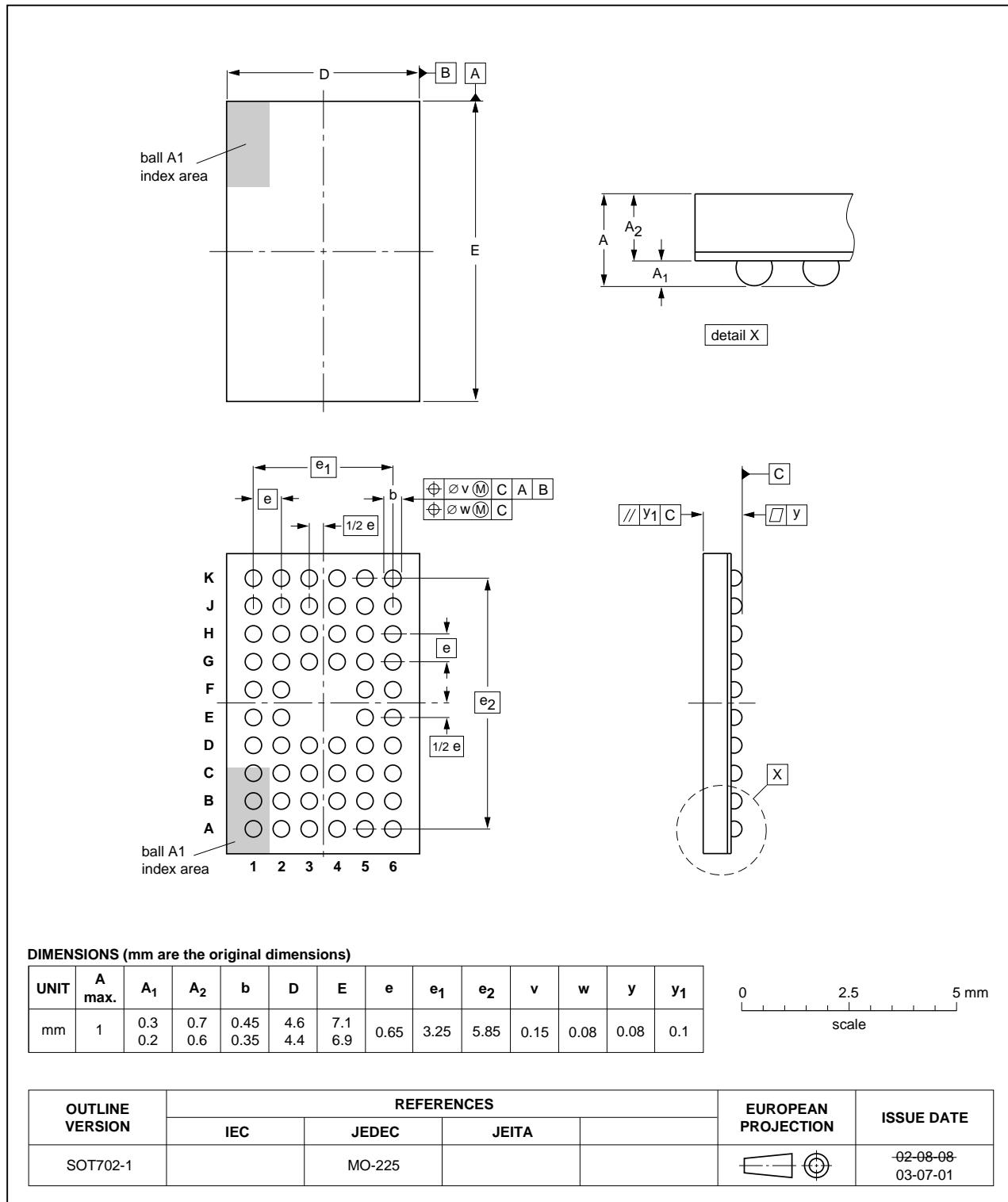


Fig 15. Package outline SOT702-1 (VFBGA56)

HXQFN60: plastic compatible thermal enhanced extremely thin quad flat package; no leads;  
60 terminals; body 4 x 6 x 0.5 mm

SOT1134-2

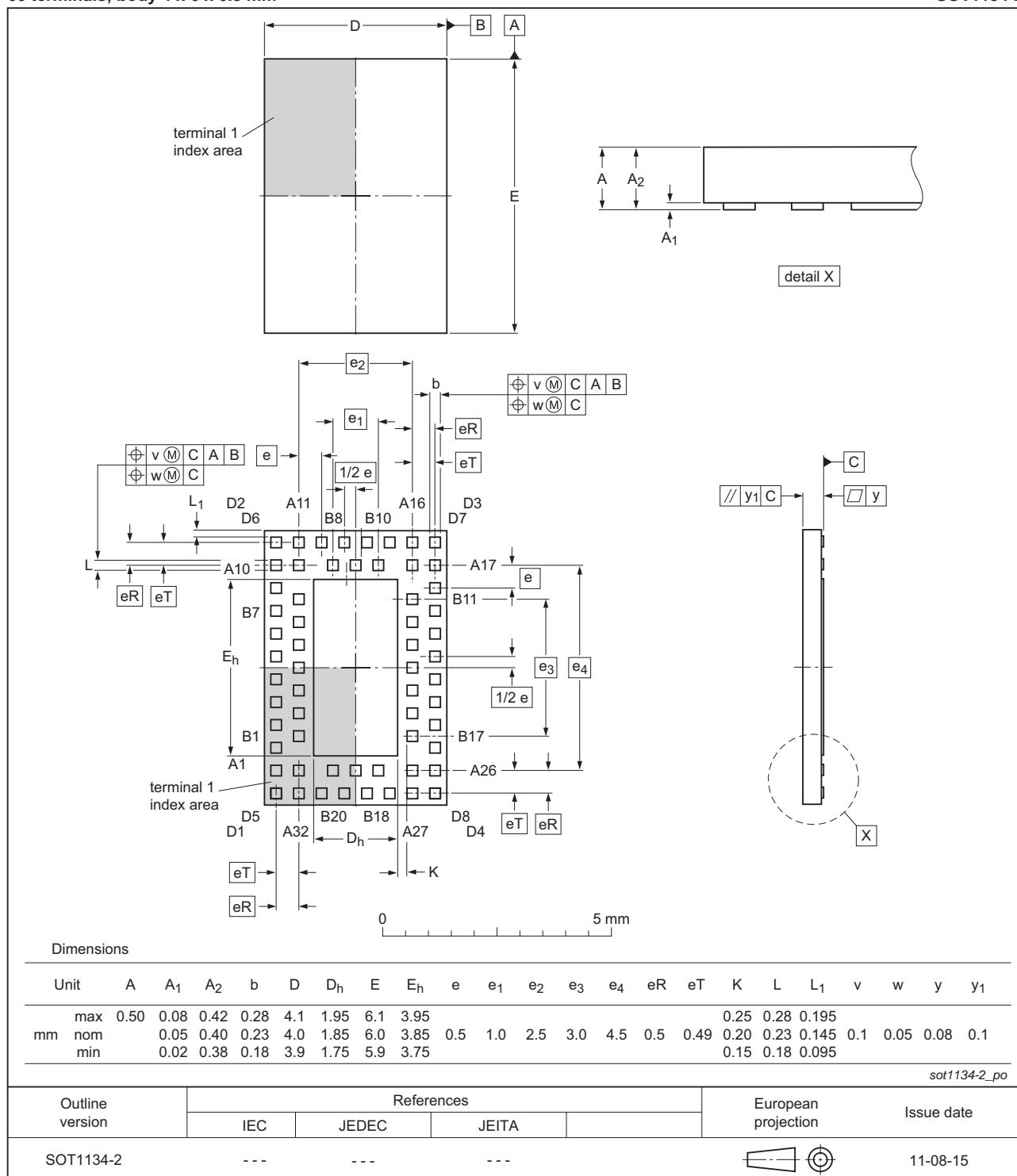


Fig 16. Package outline SOT1134-2 (HXQFN60)

## 14. Abbreviations

**Table 16. Abbreviations**

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 15. Revision history

**Table 17. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC16T245 v.6	20130909	Product data sheet	-	74AVC16T245 v.5
Modifications:		• <a href="#">Table 4</a> : conditions $I_{CC}$ and $I_{GND}$ changed (errata).		
74AVC16T245 v.5	20120309	Product data sheet	-	74AVC16T245 v.4
Modifications:		• For type number 74AVC16T245BX the sot code has changed to SOT1134-2.		
74AVC16T245 v.4	20111208	Product data sheet	-	74AVC16T245 v.3
Modifications:		• Legal pages updated.		
74AVC16T245 v.3	20110609	Product data sheet	-	74AVC16T245 v.2
74AVC16T245 v.2	20100330	Product data sheet	-	74AVC16T245 v.1
74AVC16T245 v.1	20091001	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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