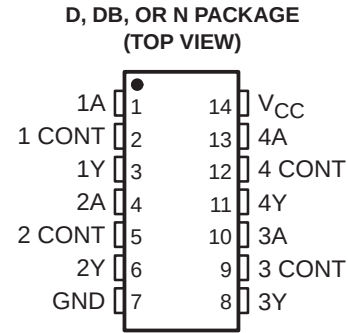


SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

SLLS041G – OCTOBER 1988 – REVISED JANUARY 2000

- Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28
- Low Supply Current . . . 420 μ A Typ
- Preset On-Chip Input Noise Filter
- Built-in Input Hysteresis
- Response and Threshold Control Inputs
- Push-Pull Outputs
- Functionally Interchangeable and Pin-to-Pin Compatible With Texas Instruments SN75189/SN75189A and Motorola MC1489/MC1489A
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages, and Standard Plastic (N) DIP



description

The SN75C189 and SN75C189A are low-power, bipolar, quadruple line receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices have been designed to conform to TIA/EIA-232-F.

The SN75C189 has a 0.33-V typical hysteresis, compared with 0.97 V for the SN75C189A. Each receiver has provision for adjustment of the overall input threshold levels. This is achieved by choosing external series resistors and voltages to provide bias levels for the response-control pins. The output is in the high logic state if the input is open circuit or shorted to ground.

These devices have an on-chip filter that rejects input pulses of less than 1- μ s duration. An external capacitor can be connected from the control pins to ground to provide further input noise filtering for each receiver.

The SN75C189 and SN75C189A have been designed using low-power techniques in a bipolar technology. In most applications, these receivers interface to single inputs of peripheral devices such as UARTs, ACEs, or microprocessors. By using sampling, such peripheral devices usually are insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN75C189 and SN75C189A outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN75C189 and SN75C189A are characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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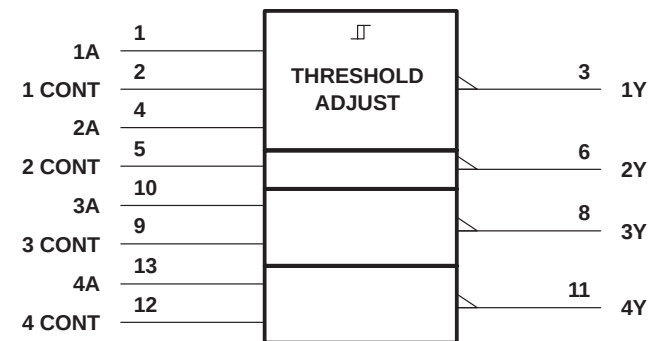
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SN75C189, SN75C189A

QUADRUPLE LOW-POWER LINE RECEIVERS

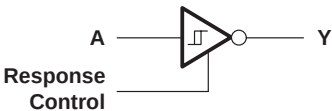
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logic symbol†

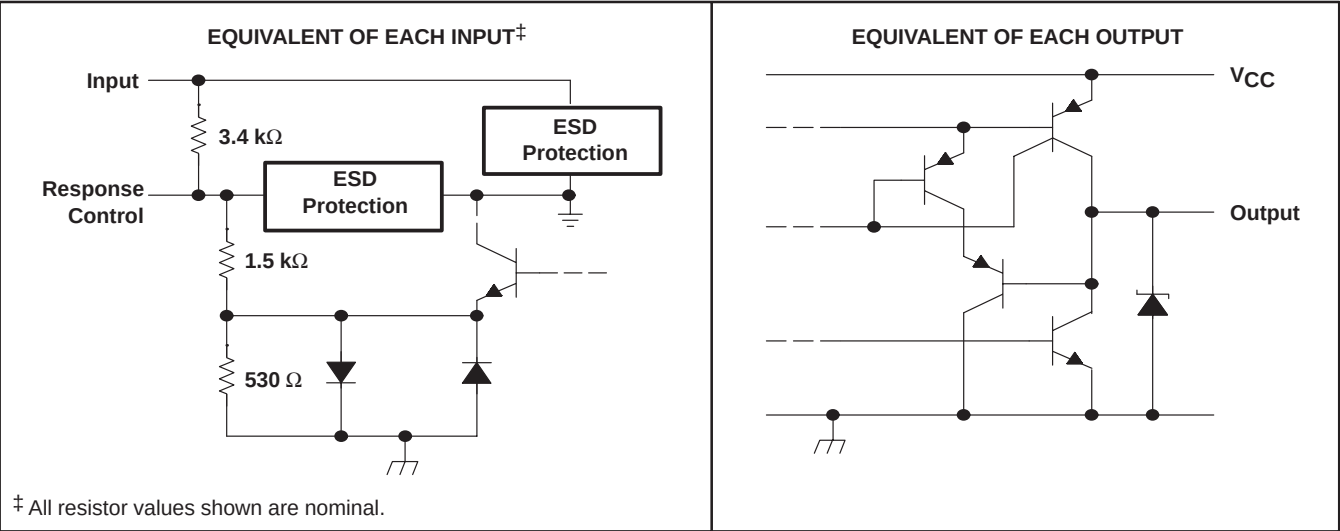


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (each receiver)



schematic of inputs and outputs



‡ All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage range, V_I	–30 V to 30 V
Output voltage range, V_O	–0.3 V to $V_{CC} + 0.3$ V
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. The package thermal impedance is calculated in accordance with JESD 51.

SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

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recommended operating conditions

	MIN	NOM	MAX	UNIT
V _{CC} Supply voltage	4.5	5	6	V
V _I Input voltage (see Note 3)	–25		25	V
I _{OH} High-level output current			–3.2	mA
I _{OL} Low-level output current			3.2	mA
Response-control current			±1	mA
T _A Operating free-air temperature	0		70	°C

NOTE 3: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is a maximum, the typical value is a more negative voltage.

electrical characteristics over recommended free-air temperature range, V_{CC} = 5 V ±10% (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{IT+} Positive-going input threshold voltage	See Figure 1	1		1.5	V
		1.6		2.25	
V _{IT–} Negative-going input threshold voltage	See Figure 1	0.75		1.25	V
		0.75	1	1.25	
V _{hys} Input hysteresis voltage (V _{IT+} – V _{IT–})	See Figure 1	0.15	0.33		V
		0.65	0.97		
V _{OH} High-level output voltage	V _{CC} = 4.5 V to 6 V, V _I = 0.75 V, I _{OH} = –20 µA	3.5			V
	V _{CC} = 4.5 V to 6 V, V _I = 0.75 V, I _{OH} = –3.2 mA	2.5			
V _{OL} Low-level output voltage	V _{CC} = 4.5 V to 6 V, V _I = 3 V, I _{OL} = 3.2 mA			0.4	V
I _{IH} High-level input current	See Figure 2	V _I = 25 V	3.6	8.3	mA
		V _I = 3 V	0.43	1	
I _{IL} Low-level input current	See Figure 2	V _I = –25 V	–3.6	–8.3	mA
		V _I = –3 V	–0.43	–1	
I _{OS} Short-circuit output current	See Figure 3			–35	mA
I _{CC} Supply current	V _I = 5 V, No load, See Figure 2		420	700	µA

[†] All typical values are at T_A = 25°C.

NOTE 4: All characteristics are measured with response-control terminal open.

switching characteristics, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low- to high-level output	R _L = 5 kΩ, C _L = 50 pF, See Figure 4			6	µs
t _{PHL} Propagation delay time, high- to low-level output				6	µs
t _{TLH} Transition time, low- to high-level output [‡]				500	ns
t _{THL} Transition time, high- to low-level output [‡]				300	ns
t _{w(N)} Duration of longest pulse rejected as noise [§]		1		6	µs

[‡] Measured between 10% and 90% points of output waveform

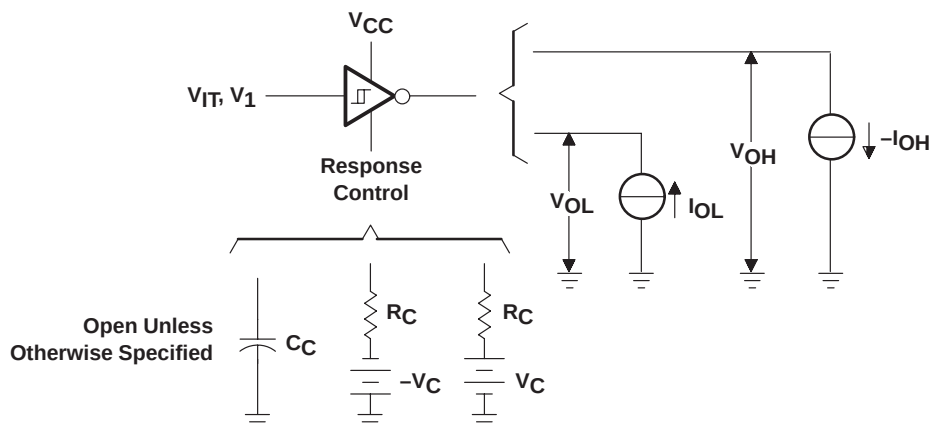
[§] The receiver ignores any positive- or negative-going pulse that is less than the minimum value of t_{w(N)} and accepts any positive- or negative-going pulse greater than the maximum of t_{w(N)}.



SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

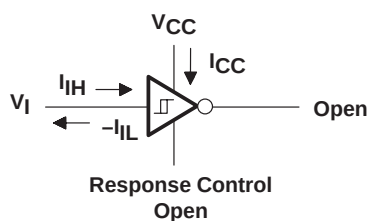
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PARAMETER MEASUREMENT INFORMATION



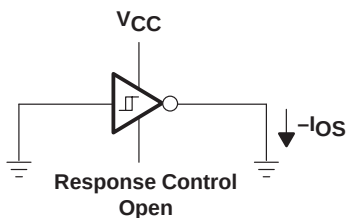
NOTE A: Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 1. V_{T+} , V_{IT-} , V_{OH} , V_{OL}



NOTE A: Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

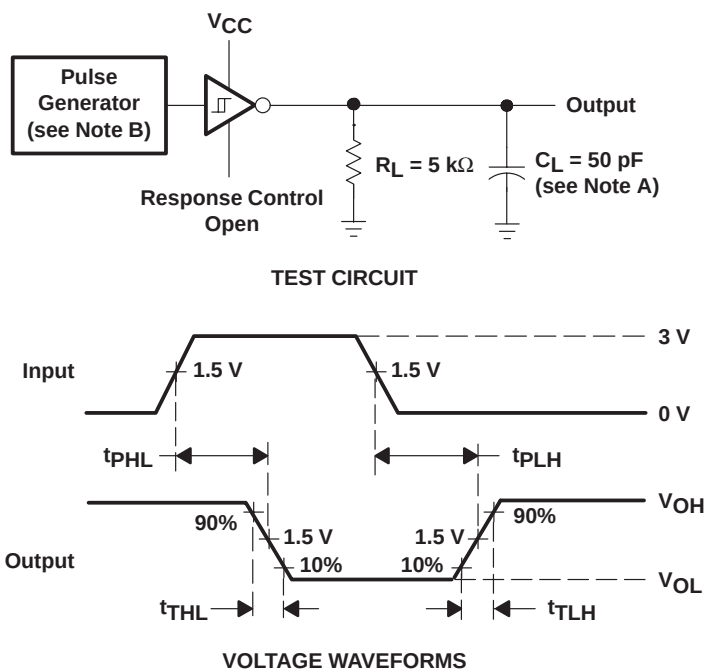
Figure 2. I_{IH} , I_{IL} , I_{CC}



NOTE A: Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 3. I_{OS}

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitances.
B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, $t_W = 25 \mu s$.

Figure 4. Test Circuit and Voltage Waveforms

SN75C189, SN75C189A
QUADRUPLE LOW-POWER LINE RECEIVERS

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TYPICAL CHARACTERISTICS

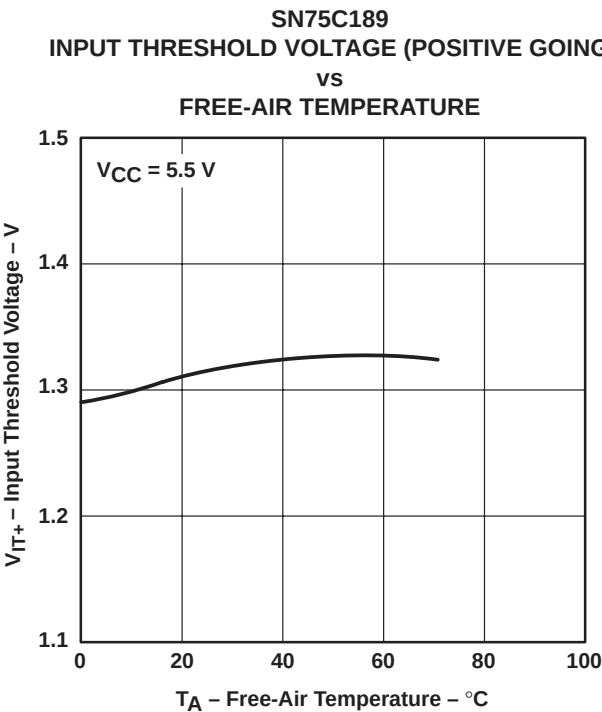


Figure 5

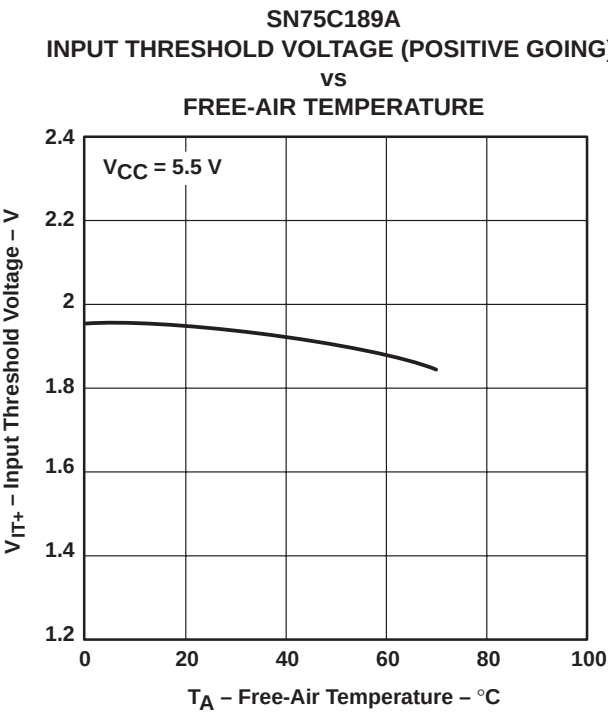


Figure 6

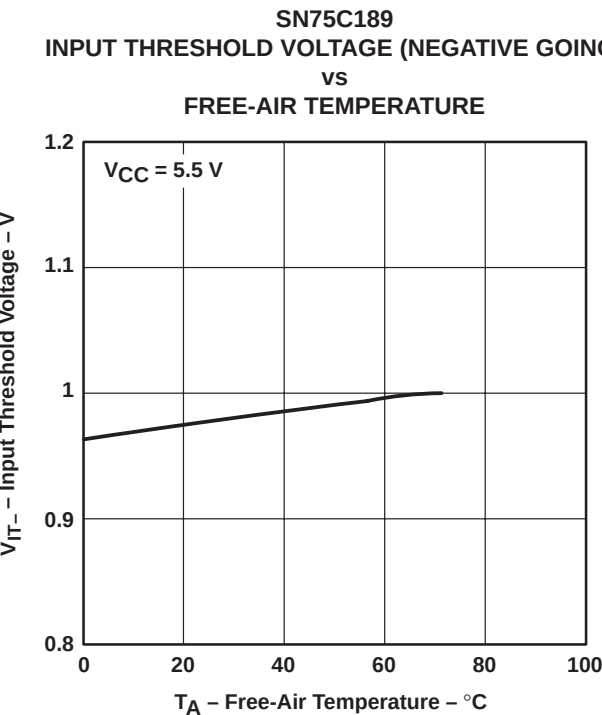


Figure 7

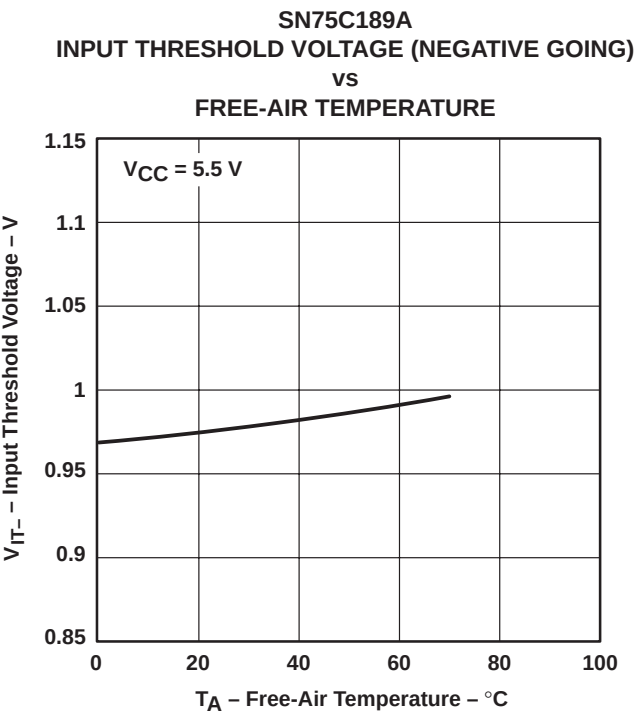


Figure 8

TYPICAL CHARACTERISTICS

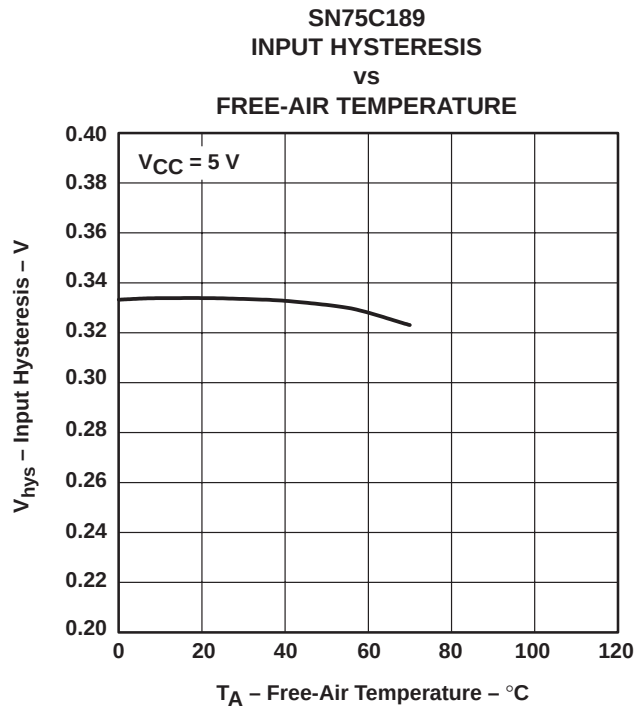


Figure 9

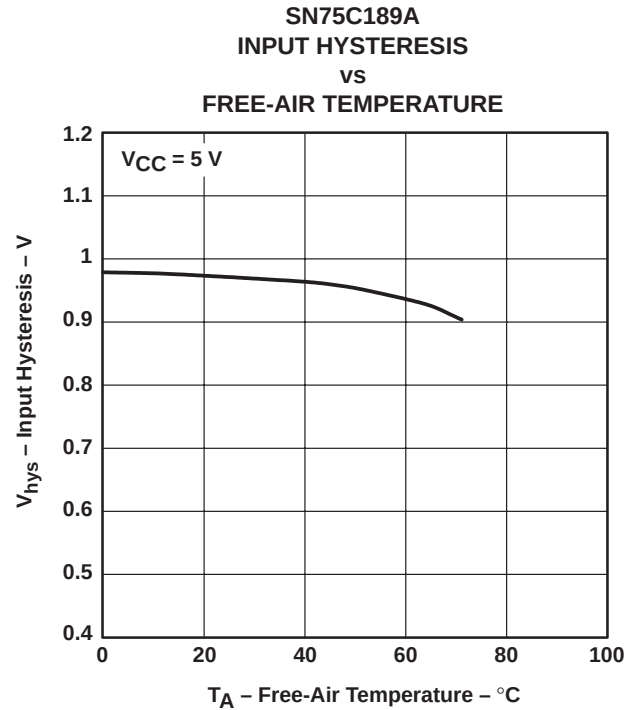


Figure 10

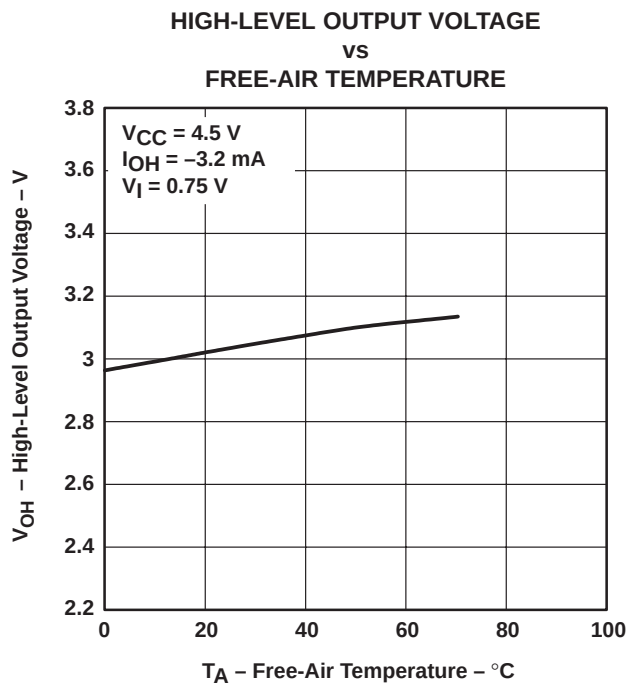


Figure 11

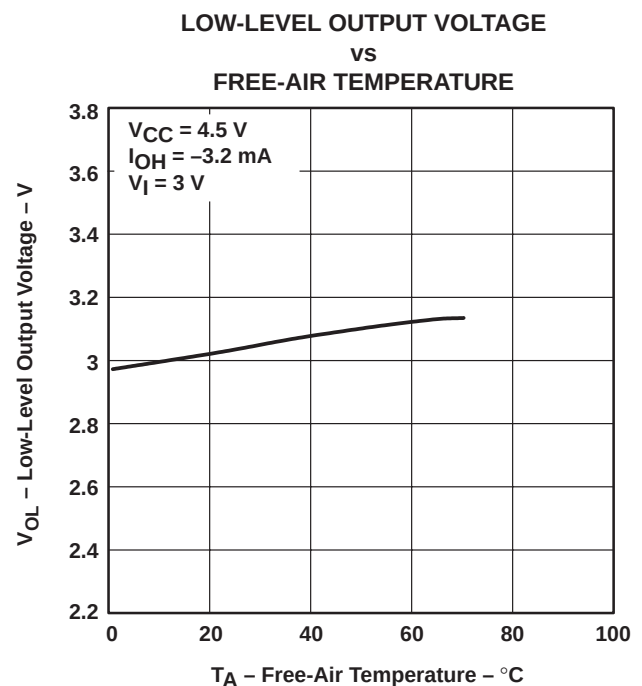


Figure 12

SN75C189, SN75C189A
QUADRUPLE LOW-POWER LINE RECEIVERS

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TYPICAL CHARACTERISTICS

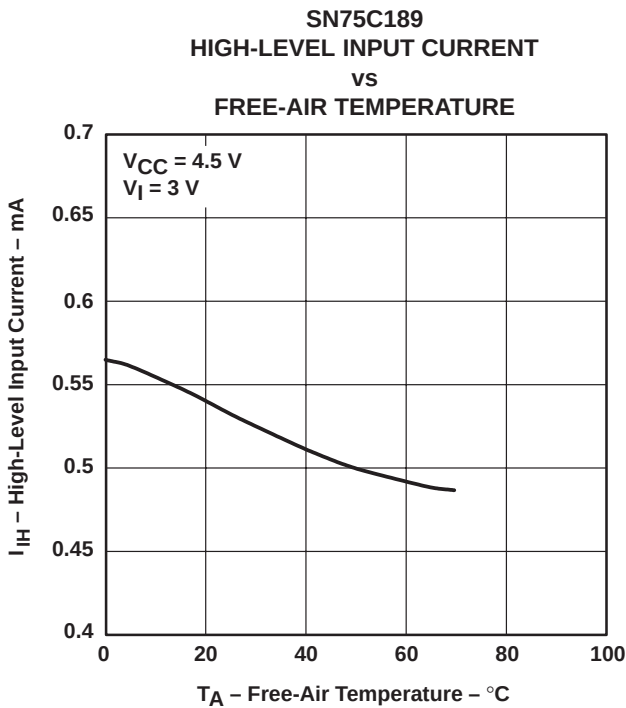


Figure 13

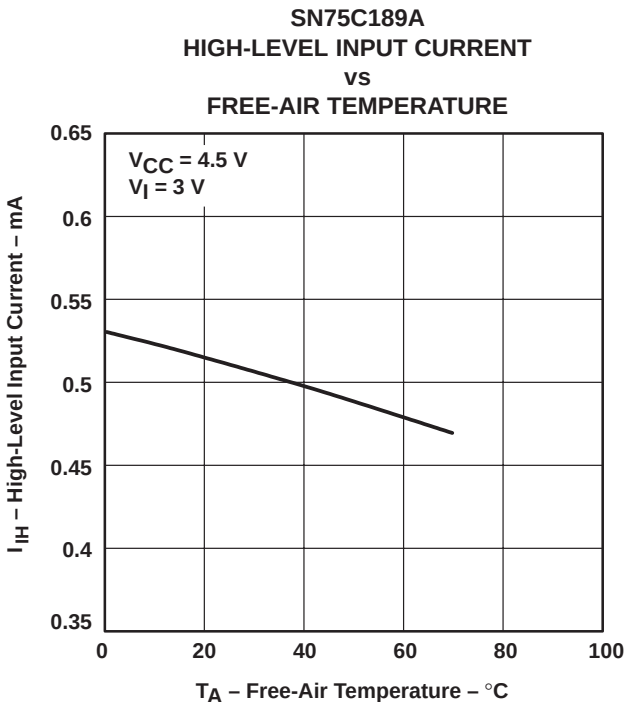


Figure 14

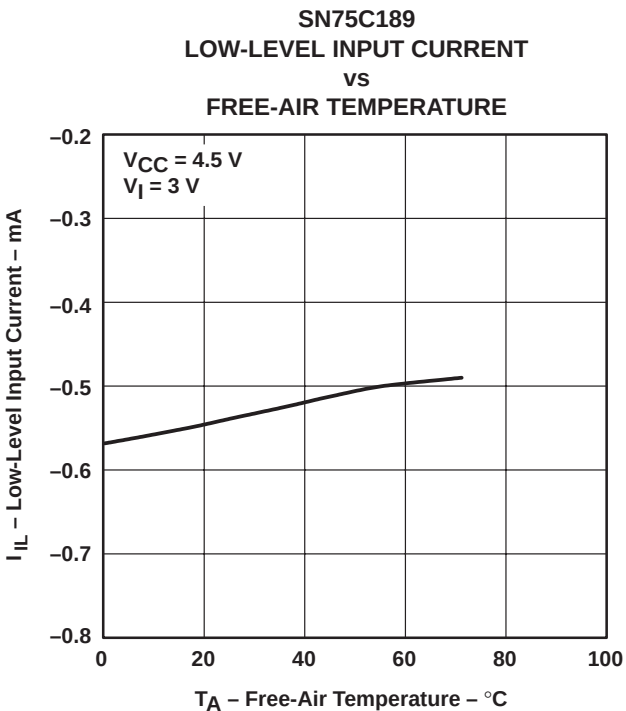


Figure 15

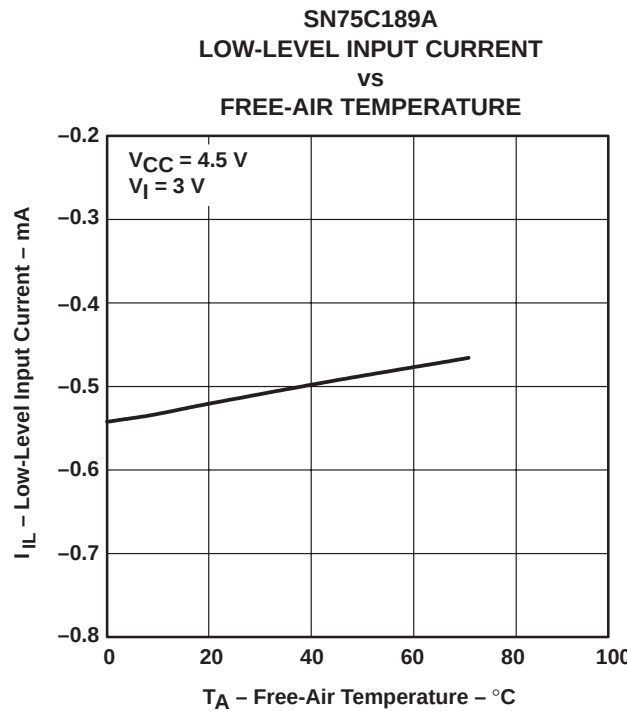


Figure 16

TYPICAL CHARACTERISTICS

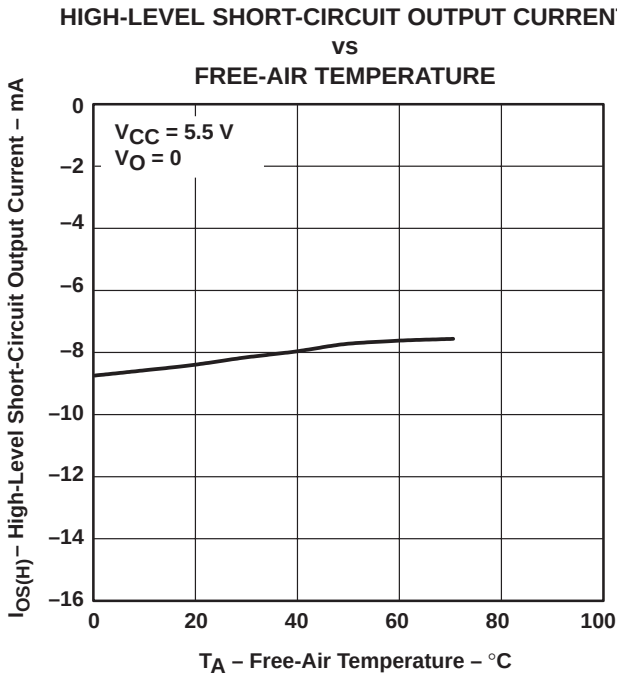


Figure 17

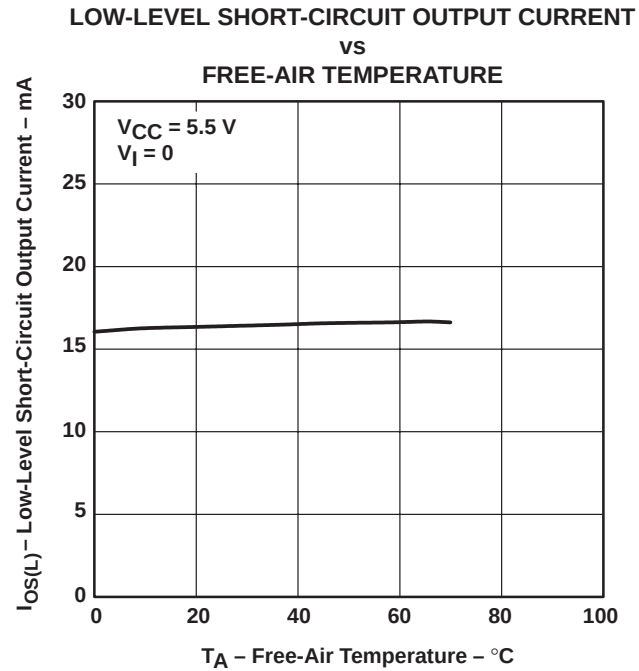


Figure 18

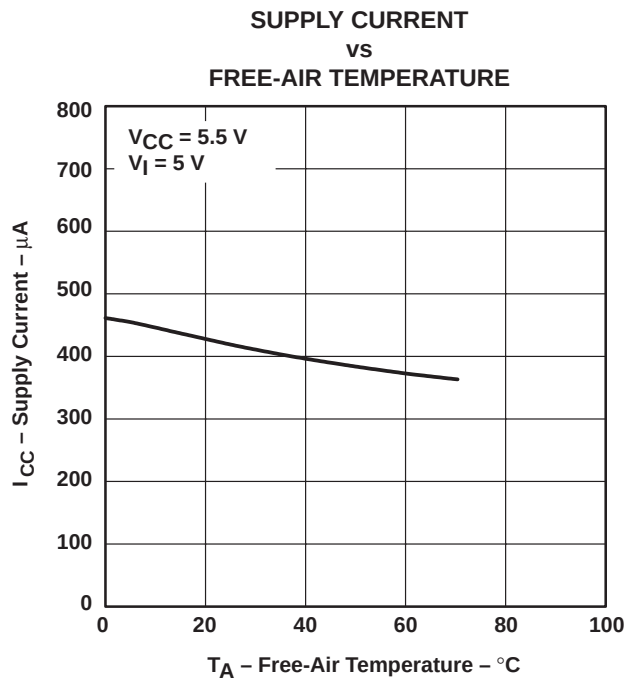


Figure 19

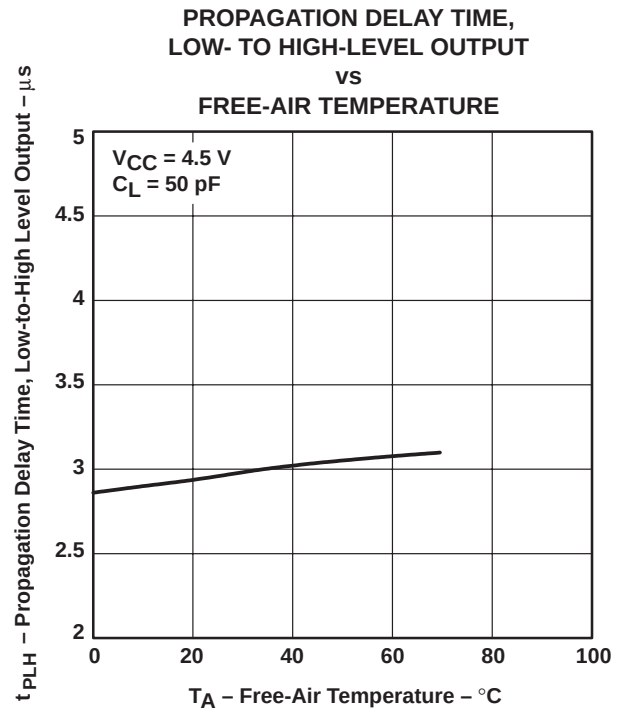


Figure 20

SN75C189, SN75C189A
QUADRUPLE LOW-POWER LINE RECEIVERS

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TYPICAL CHARACTERISTICS

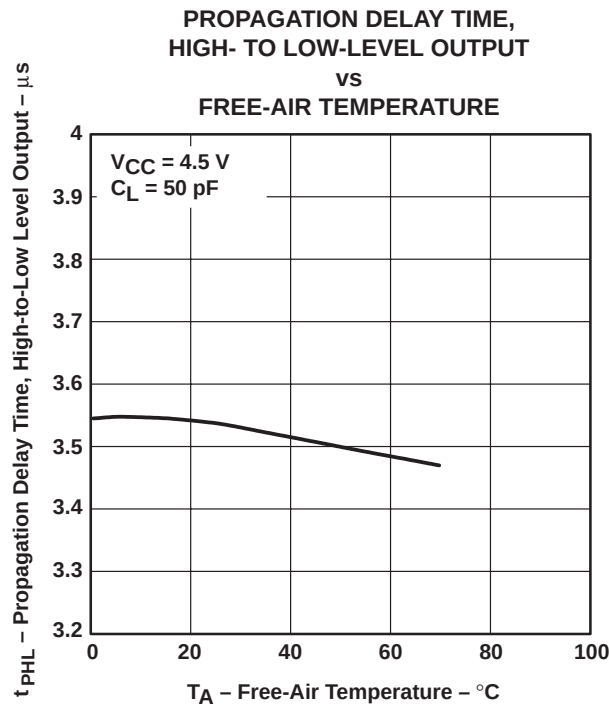


Figure 21

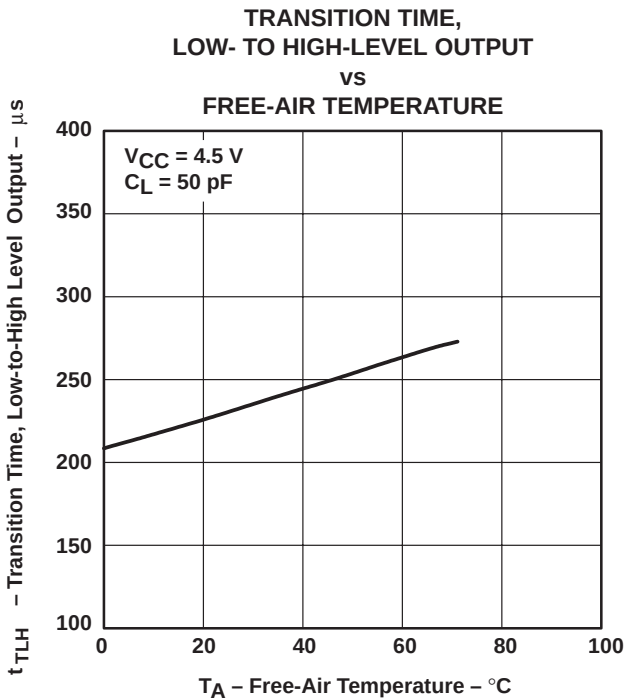


Figure 22

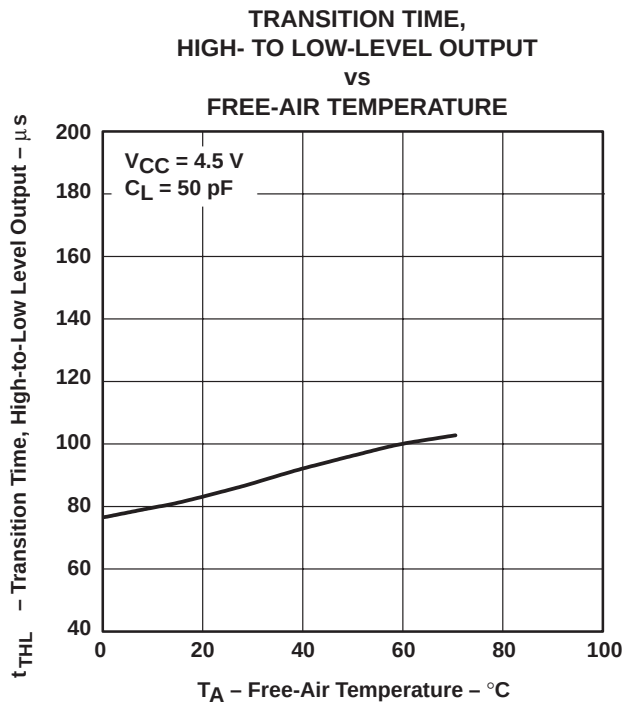


Figure 23

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75C189AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN75C189ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75C189ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75C189ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75C189NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75C189NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C189NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75C189NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

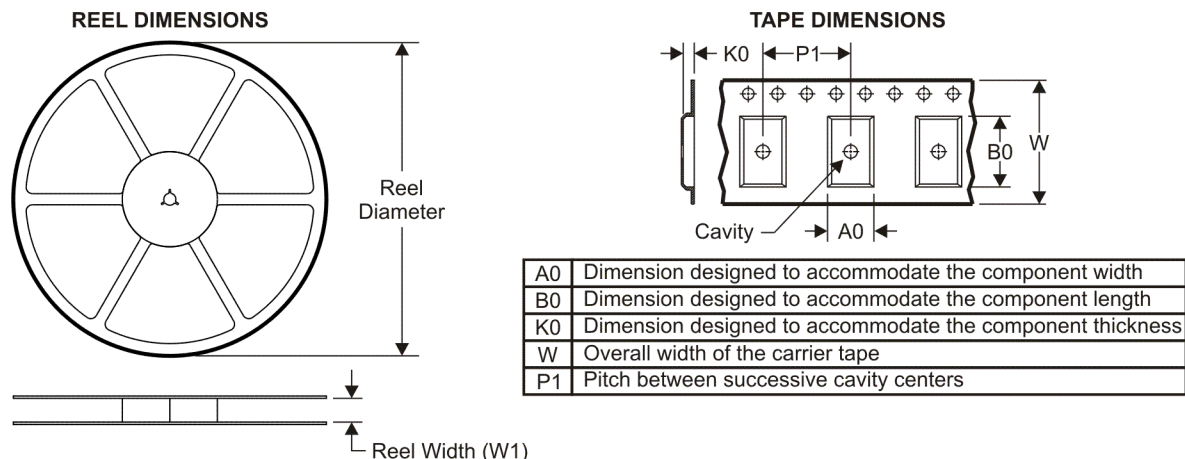
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

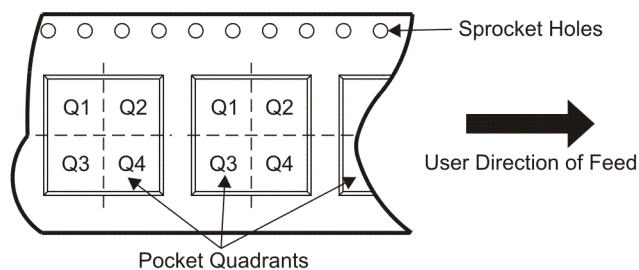
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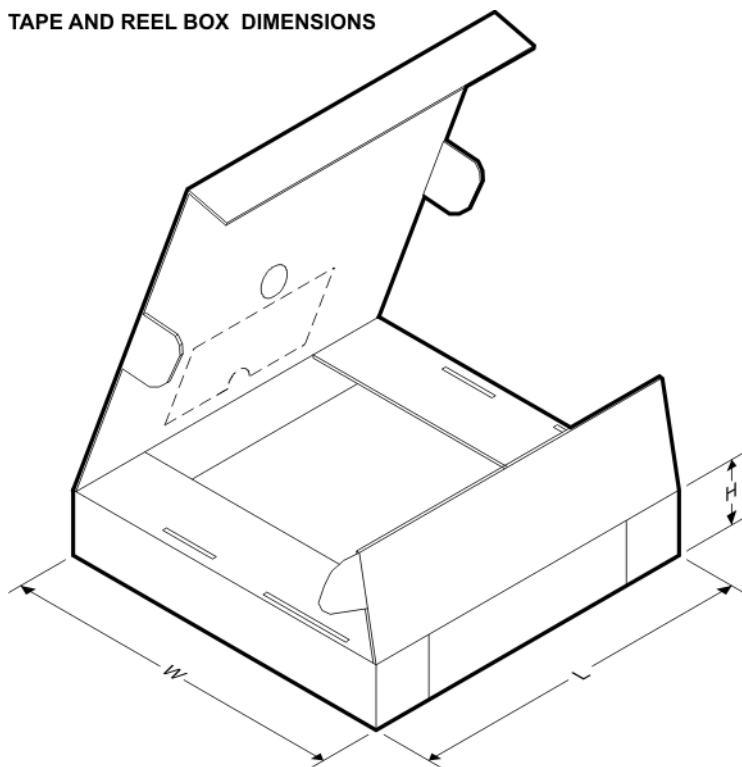
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C189ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75C189ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75C189ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75C189ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75C189DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75C189NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



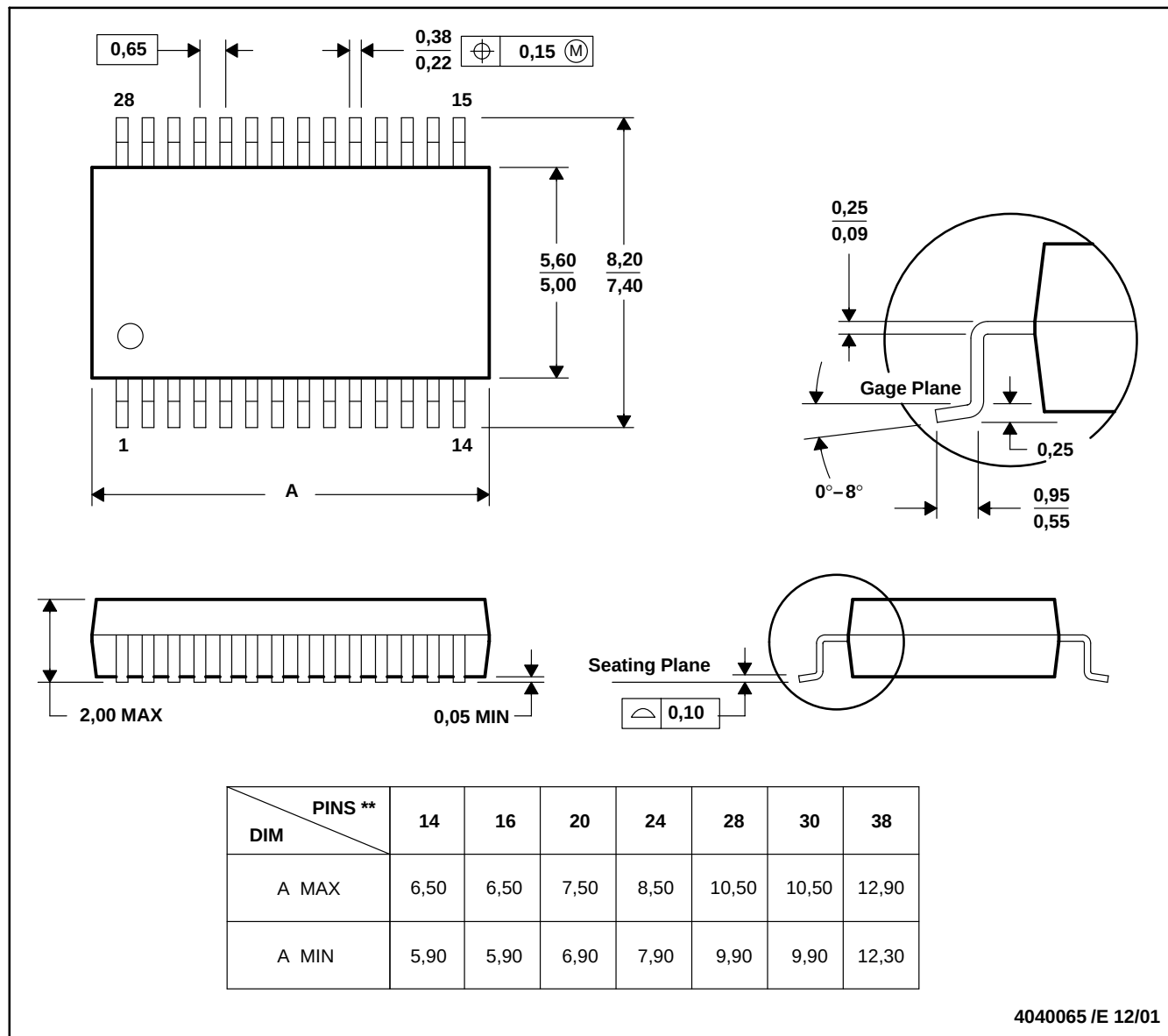
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C189ADBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN75C189ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN75C189ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN75C189ANSR	SO	NS	14	2000	346.0	346.0	33.0
SN75C189DR	SOIC	D	14	2500	346.0	346.0	33.0
SN75C189NSR	SO	NS	14	2000	346.0	346.0	33.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



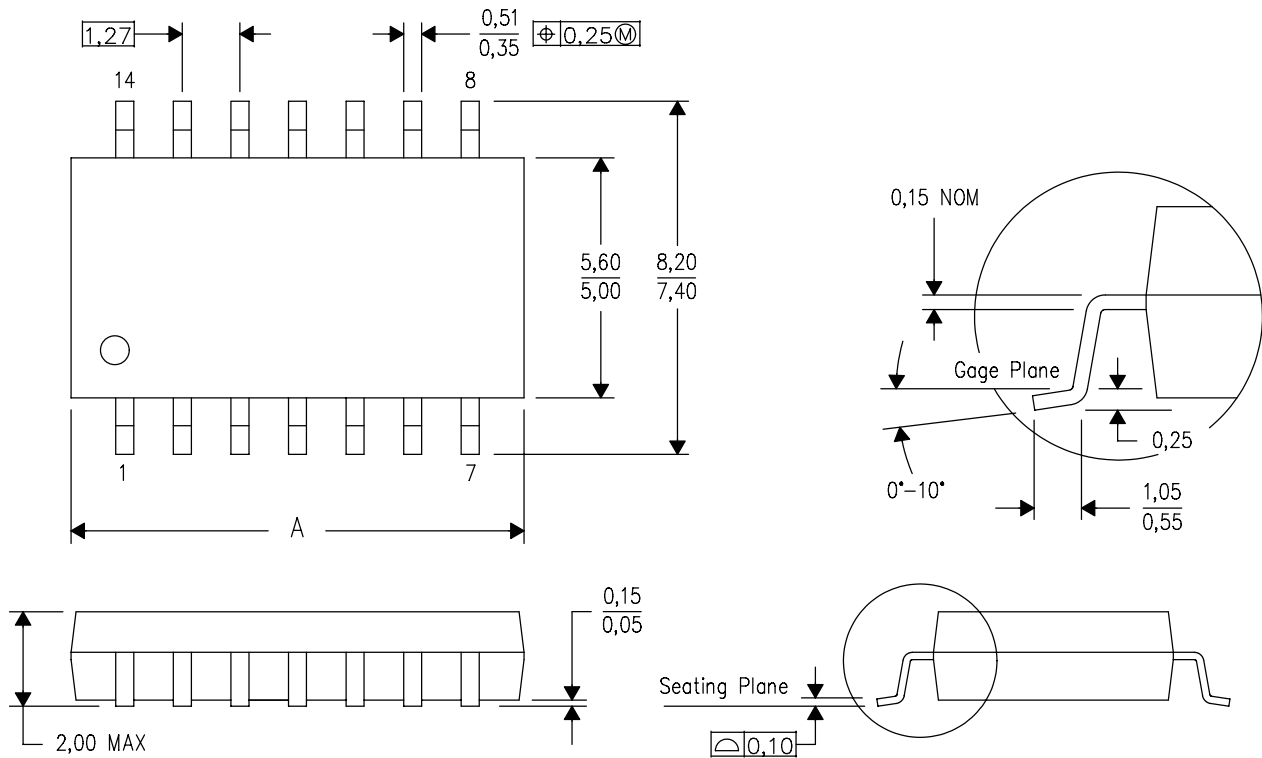
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



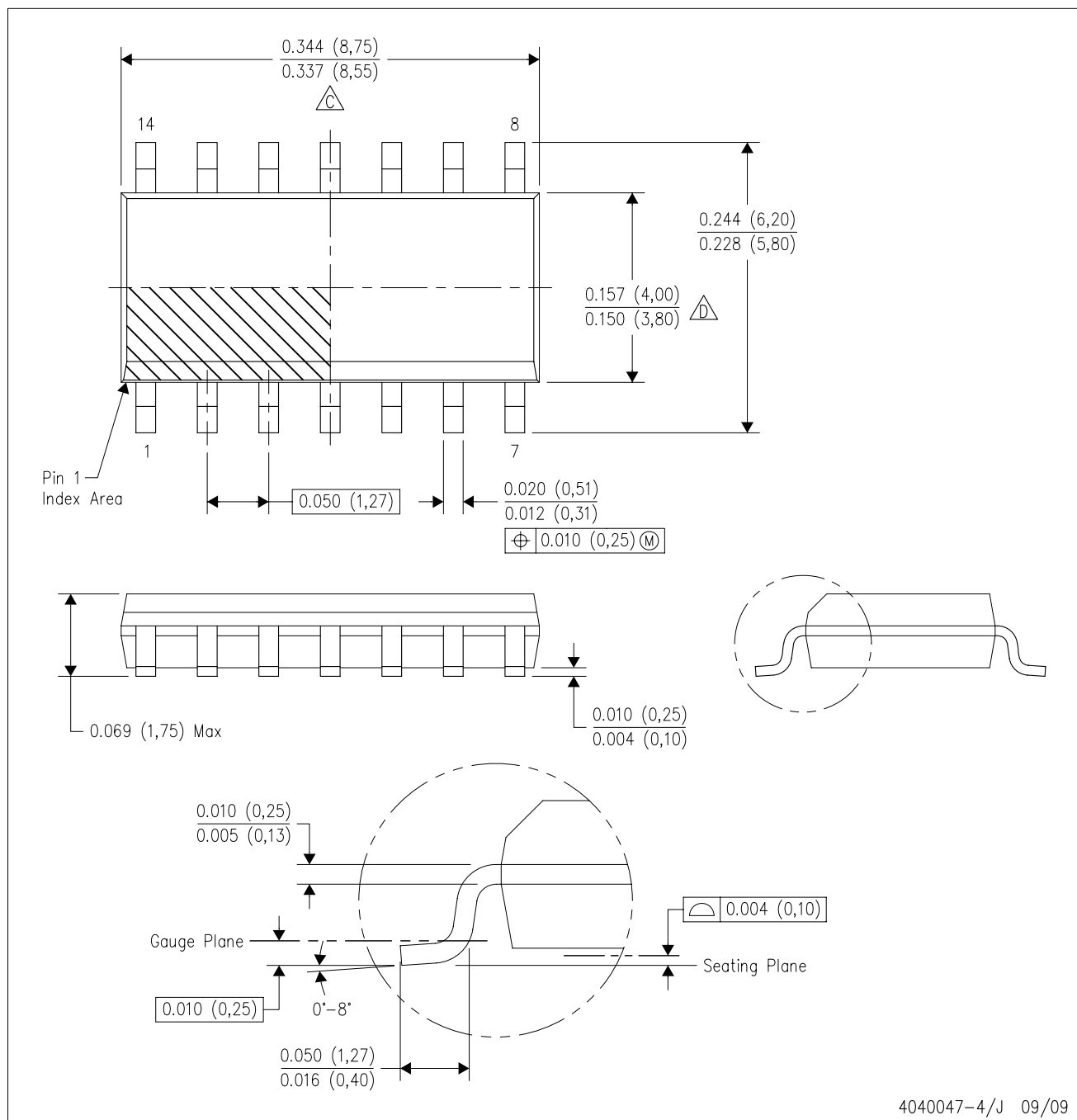
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/J 09/09

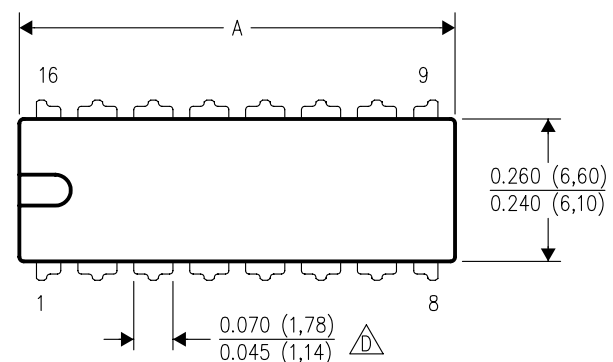
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

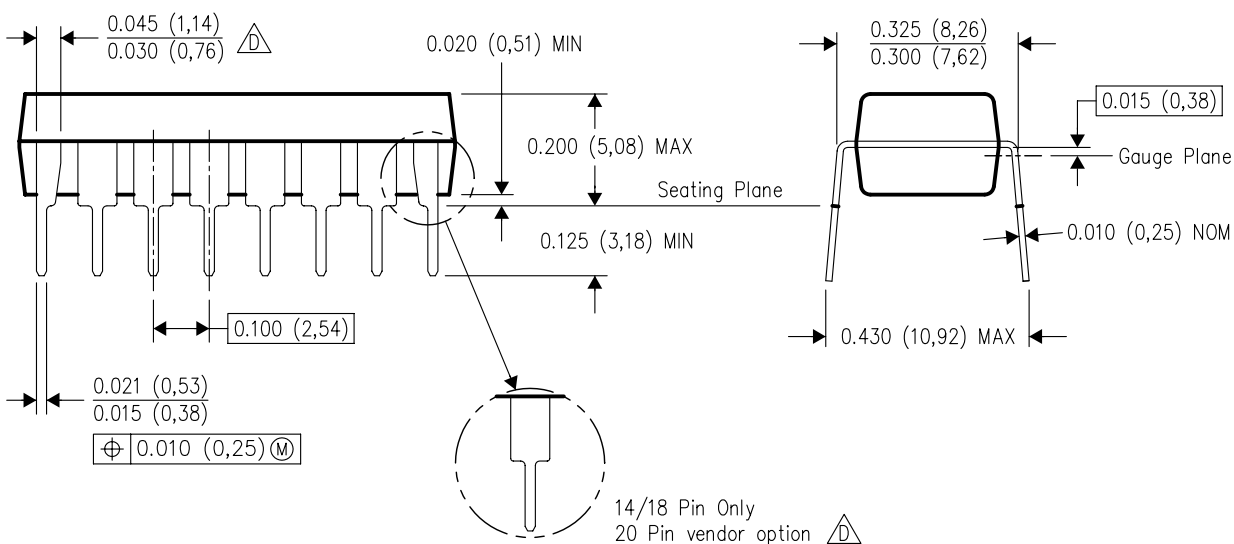
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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