

LME49811 Audio Power Amplifier Series High Fidelity 200 Volt Power Amplifier Input Stage with Shutdown

Check for Samples: [LME49811](#)

FEATURES

- Very High Voltage Operation
- Scalable Output Power
- Minimum External Components
- External Compensation
- Thermal Shutdown

APPLICATIONS

- Powered Subwoofers
- Pro Audio
- Powered Studio Monitors
- Audio Video Receivers
- Guitar Amplifiers
- High Voltage Industrial Applications

KEY SPECIFICATIONS

- Wide Operating Voltage Range: $\pm 20V$ to $\pm 100V$
- PSRR (f = DC): 115dB (Typ)
- THD+N (f = 1kHz): 0.00035% (Typ)
- Output Drive Current: 9mA

DESCRIPTION

The LME49811 is a high fidelity audio power amplifier input stage designed for demanding consumer and pro-audio applications. Amplifier output power may be scaled by changing the supply voltage and number of output devices. The LME49811 is capable of driving an output stage to deliver in excess of 500 watts single-ended into an 8 ohm load in the presence of 10% high line headroom and 20% supply regulation.

The LME49811 includes thermal shut down circuitry that activates when the die temperature exceeds 150°C. The LME49811's shutdown function when activated, forces the LME49811 into shutdown state.

TYPICAL APPLICATION

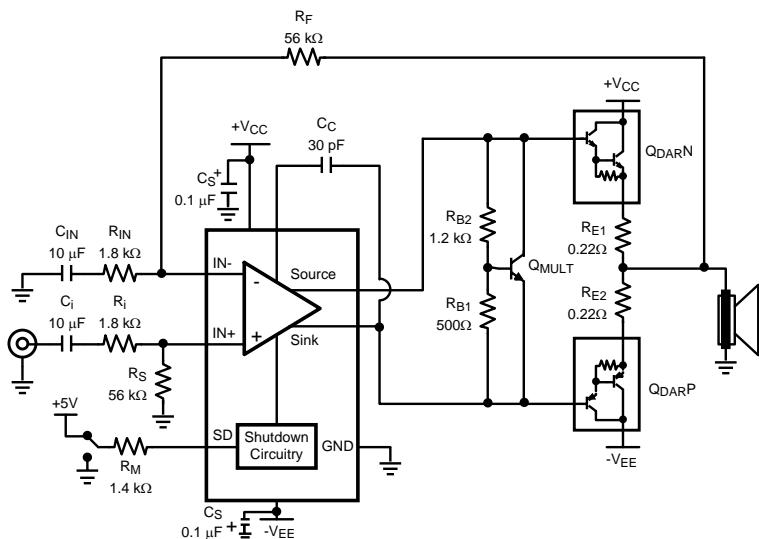


Figure 1. Typical Audio Amplifier Application Circuit



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Connection Diagram

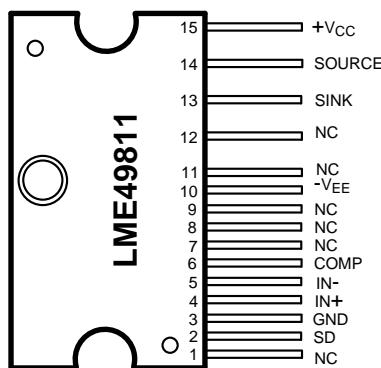


Figure 2. Top View
See Package Number NDN0015A

PIN DESCRIPTIONS

Pin	Pin Name	Description
1	NC	No Connect, Pin electrically isolated
2	SD	Shutdown Control
3	GND	Device Ground
4	IN+	Non-Inverting Input
5	IN-	Inverting Input
6	Comp	External Compensation Connection
7	NC	No Connect, Pin electrically isolated
8	NC	No Connect, Pin electrically isolated
9	NC	No Connect, Pin electrically isolated
10	-V _{EE}	Negative Power Supply
11	NC	No Connect, Pin electrically isolated
12	NC	No Connect, Pin electrically isolated
13	Sink	Output Sink
14	Source	Output Source
15	+V _{CC}	Positive Power Supply



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Supply Voltage $ V^+ + V^- $		200V
Differential Input Voltage		+/-6V
Common Mode Input Range		0.4 V_{EE} to 0.4 V_{CC}
Power Dissipation ⁽³⁾		4W
ESD Rating ⁽⁴⁾		2kV
ESD Rating ⁽⁵⁾		200V
Junction Temperature (T_{JMAX}) ⁽⁶⁾		150°C
Soldering Information	NDN Package (10 seconds)	260°C
Storage Temperature		-40°C to +150°C
Thermal Resistance	θ_{JA}	73°C/W
	θ_{JC}	4°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.
- (4) Human body model, applicable std. JESD22-A114C.
- (5) Machine model, applicable std. JESD22-A115-A.
- (6) The maximum operating junction temperature is 150°C.

OPERATING RATINGS⁽¹⁾⁽²⁾

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$	-40°C $\leq T_A \leq +85$ °C
Supply Voltage $ V^+ + V^- $		+/-20V $\leq V_{TOTAL} \leq +/100$ V

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- (2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

ELECTRICAL CHARACTERISTICS $+V_{CC} = -V_{EE} = 50V^{(1)(2)}$

The following specifications apply for $I_{SD} = 1.5mA$, [Figure 1](#), unless otherwise specified. Limits apply for $T_A = 25^\circ C$, $C_C = 30pF$.

Symbol	Parameter	Conditions	LME49811		Units (Limits)
			Typical ⁽³⁾	Limit ⁽⁴⁾	
I_{CC}	Total Quiescent Power Supply Current	$V_{CM} = 0V$, $V_O = 0V$, $I_O = 0A$	14	17	mA (max)
I_{EE}	Total Quiescent Power Supply Current	$V_{CM} = 0V$, $V_O = 0V$, $I_O = 0A$	16	19	mA (max)
THD+N	Total Harmonic Distortion + Noise	No load, $A_V = 29dB$ $V_{OUT} = 20V_{RMS}$, $f = 1kHz$	0.00055	0.0015	% (max)
A_V	Closed Loop Voltage Gain			26	dB (min)
A_V	Open Loop Gain	$V_{IN} = 1mV_{RMS}$, $f = 1kHz$	93		dB
		$f = DC$	120		dB
V_{OM}	Output Voltage Swing	THD+N = 0.05%, Freq = 20Hz to 20kHz	33		V_{RMS}
V_{NOISE}	Output Noise	LPF = 30kHz, $A_V = 29dB$	100		μV
		A-weighted	70	180	μV (max)
I_{OUT}	Output Current	Outputs Shorted	8	6.5	mA(min)
I_{SD}	Current into Shutdown Pin	To put part in “play” mode	1.5	1 2	mA(min) mA (max)
SR	Slew Rate	$V_{IN} = 1.2V_{P-P}$, $f = 10kHz$ square Wave, Outputs shorted	16	13	$V/\mu s$ (min)
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $I_O = 0mA$	1	3	mV (max)
I_B	Input Bias Current	$V_{CM} = 0V$, $I_O = 0mA$	100		nA
PSRR	Power Supply Rejection Ratio	DC, Input Referred	115	105	dB (min)

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- (3) Typical values represent most likely parametric norms at $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) Data sheet min/max specification limits are ensured by test or statistical analysis.

ELECTRICAL CHARACTERISTICS $+V_{CC} = -V_{EE} = 100V^{(1)(2)}$

The following specifications apply for $I_{SD} = 1.5mA$, [Figure 1](#), unless otherwise specified. Limits apply for $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	LME49811		Units (Limits)
			Typical ⁽³⁾	Limit ⁽⁴⁾	
I_{CC}	Total Quiescent Power Supply Current	$V_{CM} = 0V, V_O = 0V, I_O = 0A$	17	22	mA (max)
I_{EE}	Total Quiescent Power Supply Current	$V_{CM} = 0V, V_O = 0V, I_O = 0A$	19	24	mA (max)
THD+N	Total Harmonic Distortion + Noise	No load, $A_V = 30dB$ $V_{OUT} = 30V_{RMS}, f = 1kHz$	0.00035	0.001	% (max)
A_V	Closed Loop Voltage Gain			26	dB (min)
A_V	Open Loop Gain	$V_{IN} = 1mV_{RMS}, f = 1kHz$	93		dB
		$f = DC$	120		dB
V_{OM}	Output Voltage Swing	THD+N = 0.05%, Freq = 20Hz to 20kHz	68		V_{RMS}
V_{NOISE}	Output Noise	LPF = 30kHz, $A_V = 29dB$	100		μV
		A-weighted	70	180	μV (max)
I_{OUT}	Output Current	Outputs Shorted	9	7	mA(min)
I_{SD}	Current into Shutdown Pin	To put part in "play" mode	1.5	1 2	mA(min) mA (max)
SR	Slew Rate	$V_{IN} = 1.2V_{P-P}, f = 10kHz$ square Wave, Outputs shorted	17	14	$V/\mu s$ (min)
V_{OS}	Input Offset Voltage	$V_{CM} = 0V, I_O = 0mA$	1	3	mV (max)
I_B	Input Bias Current	$V_{CM} = 0V, I_O = 0mA$	100		nA (max)
PSRR	Power Supply Rejection Ratio	$f = DC$, Input Referred	115	105	dB (min)

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- (3) Typical values represent most likely parametric norms at $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) Data sheet min/max specification limits are ensured by test or statistical analysis.

TYPICAL PERFORMANCE CHARACTERISTICS

Data taken with Bandwidth = 30kHz, $A_V = 29$ dB, $C_C = 30$ pF, and $T_A = 25^\circ\text{C}$ except where specified.

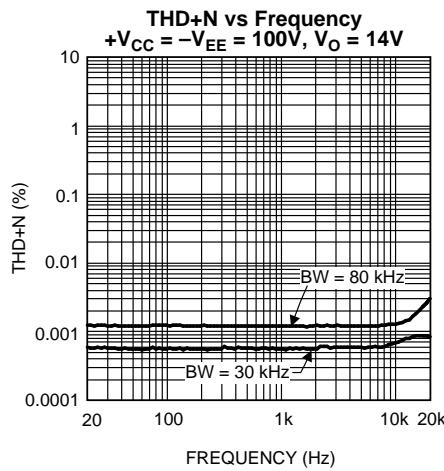


Figure 3.

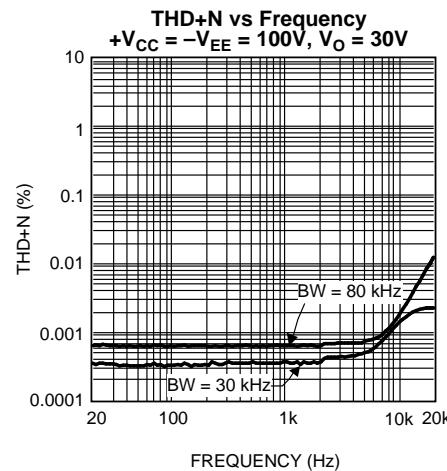


Figure 4.

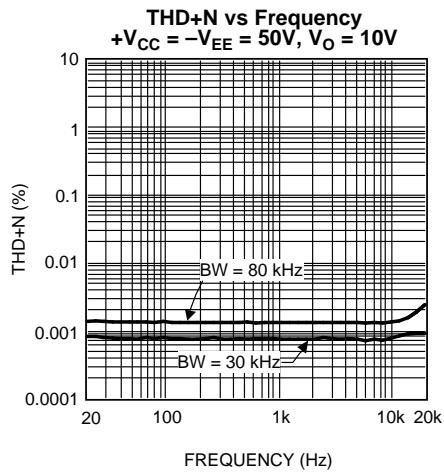


Figure 5.

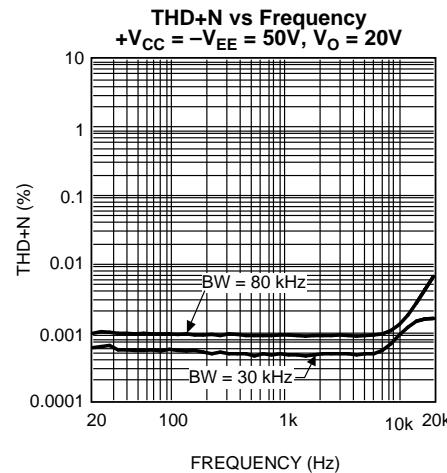


Figure 6.

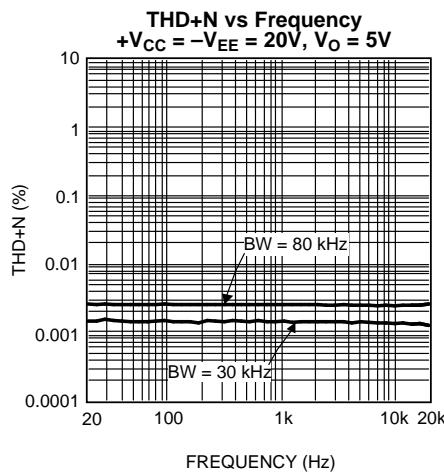


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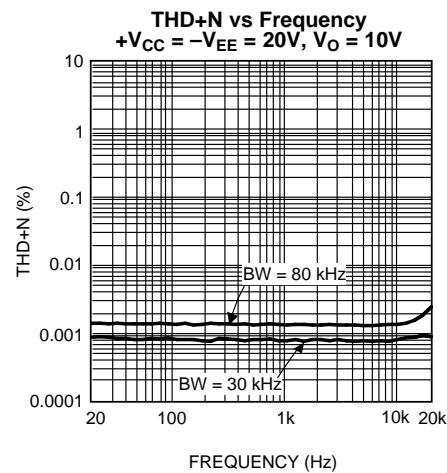


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Data taken with Bandwidth = 30kHz, $A_V = 29\text{dB}$, $C_C = 30\text{pF}$, and $T_A = 25^\circ\text{C}$ except where specified.

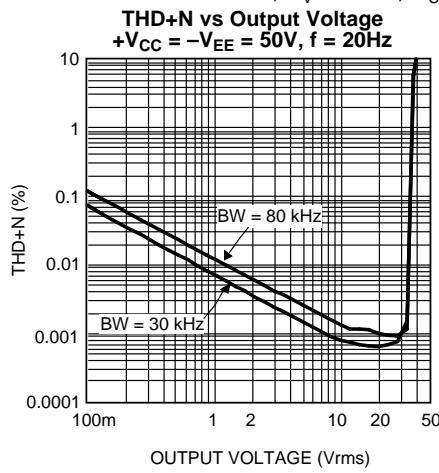


Figure 9.

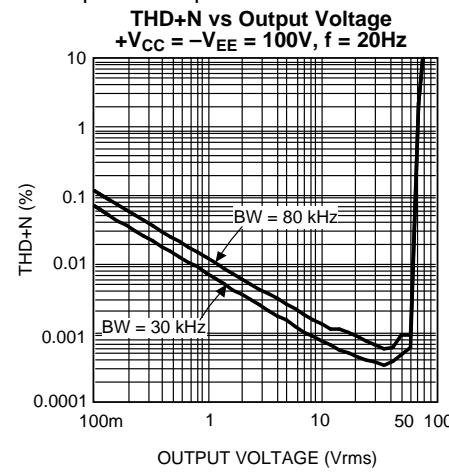


Figure 10.

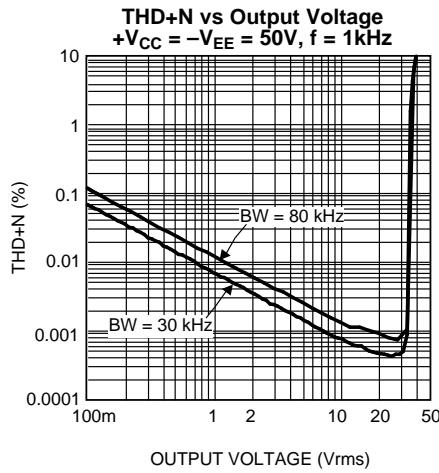


Figure 11.

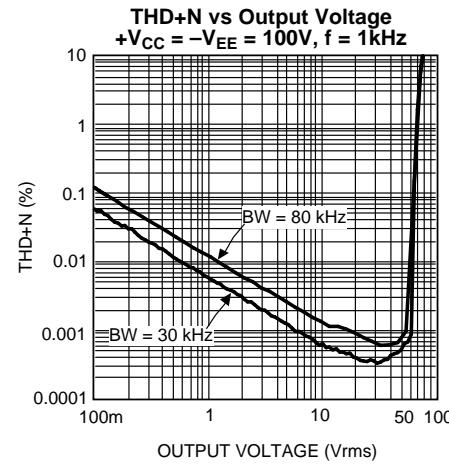


Figure 12.

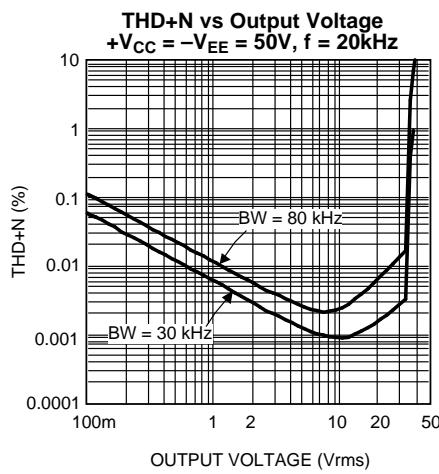


Figure 13.

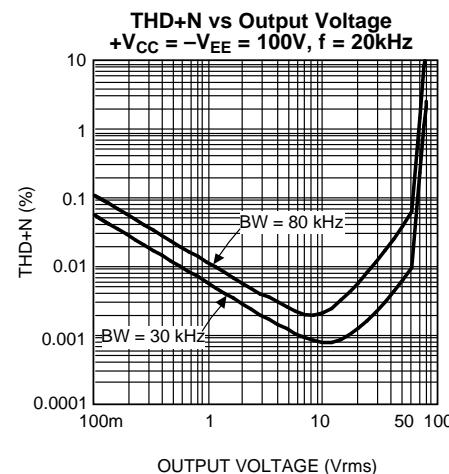


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Data taken with Bandwidth = 30kHz, $A_V = 29\text{dB}$, $C_C = 30\text{pF}$, and $T_A = 25^\circ\text{C}$ except where specified.

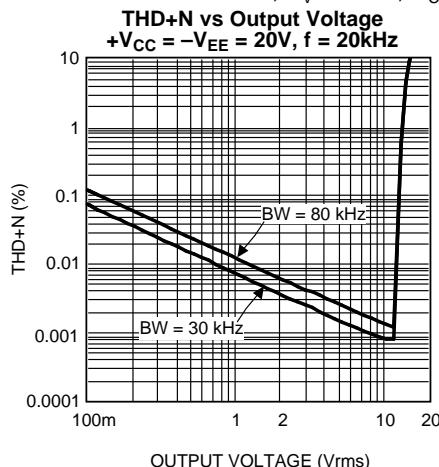


Figure 15.

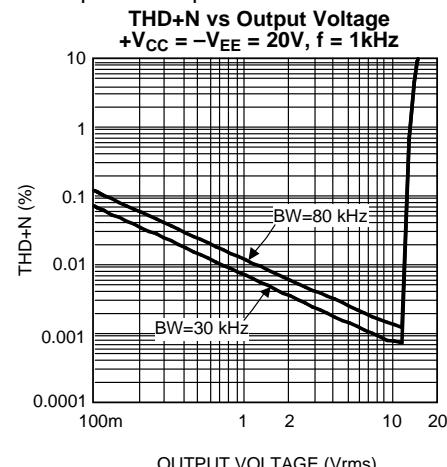


Figure 16.

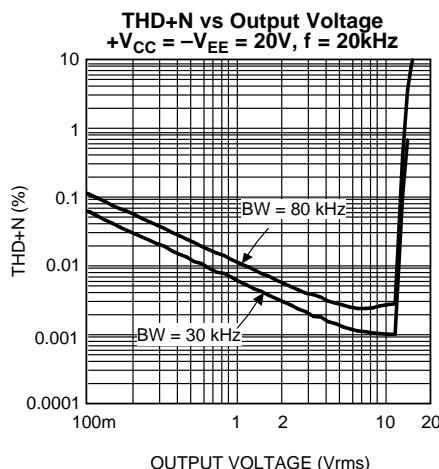


Figure 17.

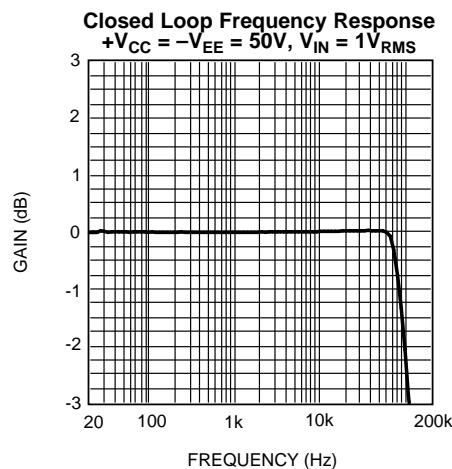


Figure 18.

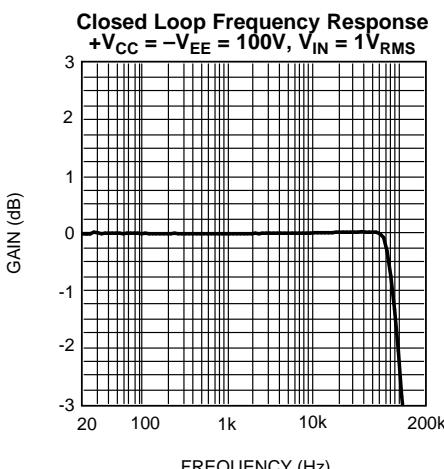


Figure 19.

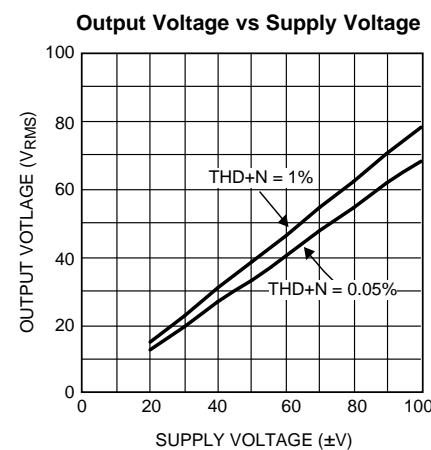


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Data taken with Bandwidth = 30kHz, $A_V = 29$ dB, $C_C = 30$ pF, and $T_A = 25^\circ\text{C}$ except where specified.

PSRR vs Frequency
 $+V_{CC} = -V_{EE} = 100$ V, No Filters
Input Referred, $V_{RIPPLE} = 1$ V_{RMS} on V_{CC} pin

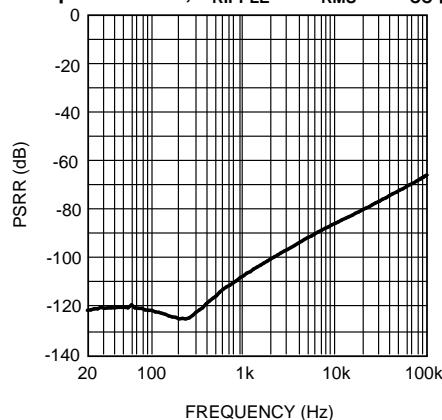


Figure 21.

PSRR vs Frequency
 $+V_{CC} = -V_{EE} = 50$ V, No Filters
Input Referred, $V_{RIPPLE} = 1$ V_{RMS} on V_{CC} pin

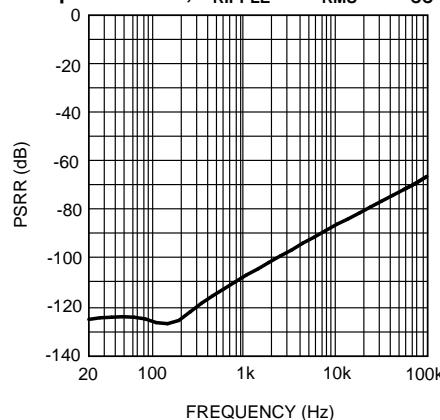


Figure 22.

PSRR vs Frequency
 $+V_{CC} = -V_{EE} = 100$ V, No Filters
Input Referred, $V_{RIPPLE} = 1$ V_{RMS} on V_{EE} pin

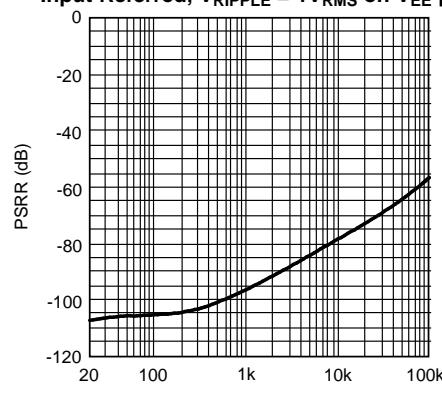


Figure 23.

PSRR vs Frequency
 $+V_{CC} = -V_{EE} = 50$ V, No Filters
Input Referred, $V_{RIPPLE} = 1$ V_{RMS} on V_{EE} pin

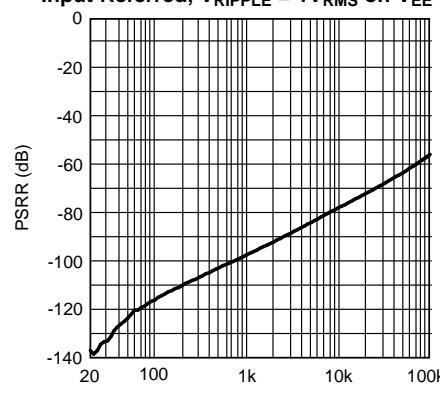


Figure 24.

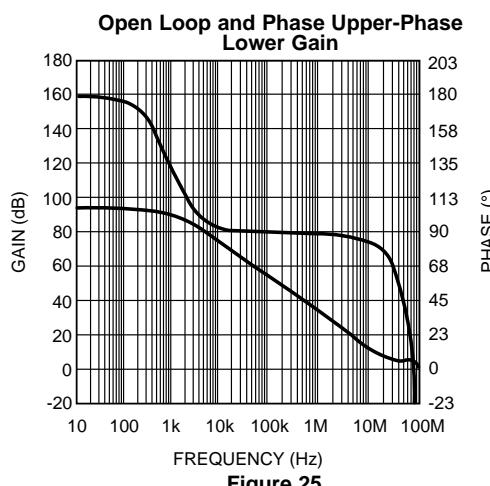


Figure 25.

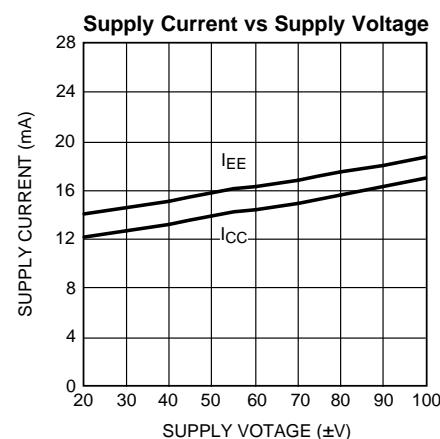


Figure 26.

TEST CIRCUIT

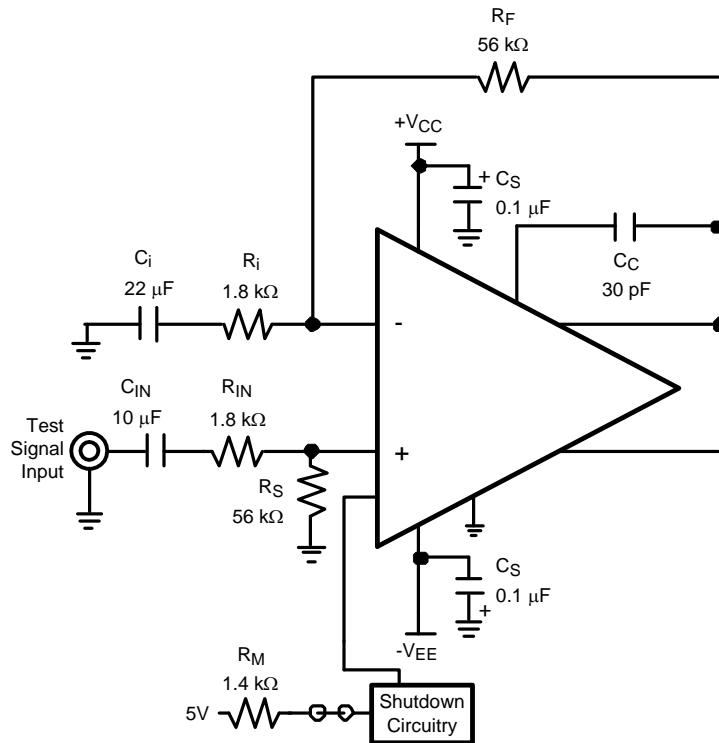


Figure 27. Test Circuit

APPLICATION INFORMATION

SHUTDOWN FUNCTION

The shutdown function of the LME49811 is controlled by the amount of current that flows into the shutdown pin. If there is less than 1mA of current flowing into the shutdown pin, the part will be in shutdown. This can be achieved by shorting the shutdown pin to ground or by floating the shutdown pin. If there is between 1mA and 2mA of current flowing into the shutdown pin, the part will be in “play” mode. This can be done by connecting a reference voltage to the shutdown pin through a resistor (R_M). The current into the shutdown pin can be determined by the equation $I_{SD} = (V_{REF} - 2.9) / R_M$. For example, if a 5V power supply is connected through a 1.4kΩ resistor to the shutdown pin, then the shutdown current will be 1.5mA, at the center of the specified range. It is also possible to use V_{CC} as the power supply for the shutdown pin, though R_M will have to be recalculated accordingly. It is not recommended to flow more than 2mA of current into the shutdown pin because damage to the LME49811 may occur.

It is highly recommended to switch between shutdown and “play” modes rapidly. This is accomplished most easily through using a toggle switch that alternatively connects the shutdown pin through a resistor to either ground or the shutdown pin power supply. Slowly increasing the shutdown current may result in undesired voltages on the outputs of the LME49811, which can damage an attached speaker.

THERMAL PROTECTION

The LME49811 has a thermal protection scheme to prevent long-term thermal stress of the device. When the temperature on the die exceeds 150°C, the LME49811 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur again above 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 150°C and 145°C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink used, the heat sink should be chosen so that thermal shutdown is not activated during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device, as discussed in the [DETERMINING THE CORRECT HEAT SINK](#) section.

POWER DISSIPATION AND HEAT SINKING

When in “play” mode, the LME49811 draws a constant amount of current, regardless of the input signal amplitude. Consequently, the power dissipation is constant for a given supply voltage and can be computed with the equation $P_{D\text{MAX}} = I_{CC} * (V_{CC} - V_{EE})$.

DETERMINING THE CORRECT HEAT SINK

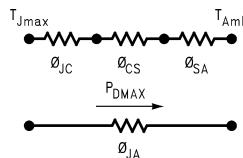
The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry is not activated under normal circumstances.

The thermal resistance from the die to the outside air, θ_{JA} (junction to ambient), is a combination of three thermal resistances, θ_{JC} (junction to case), θ_{CS} (case to sink), and θ_{SA} (sink to ambient). The thermal resistance, θ_{JC} (junction to case), of the LME49811 is 0.4 °C/W. Using Thermalloy Thermacote thermal compound, the thermal resistance, θ_{CS} (case to sink), is about 0.2°C/W. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LME49811 is equal to the following:

$$P_{D\text{MAX}} = (T_{J\text{MAX}} - T_{\text{AMB}}) / \theta_{JA}$$

where

- $T_{J\text{MAX}} = 150^\circ\text{C}$
- T_{AMB} is the system ambient temperature
- $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$

(1)


Once the maximum package power dissipation has been calculated using [Equation \(1\)](#), the maximum thermal resistance, θ_{SA} , (heat sink to ambient) in °C/W for a heat sink can be calculated. This calculation is made using [Equation \(2\)](#) which is derived by solving for θ_{SA} in [Equation \(1\)](#).

$$\theta_{SA} = [(T_{J\text{MAX}} - T_{\text{AMB}}) - P_{D\text{MAX}}(\theta_{JC} + \theta_{CS})] / P_{D\text{MAX}} \quad (2)$$

Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier requirements. If the ambient temperature that the audio amplifier is to be working under is higher than 25°C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components is required to meet the design targets of an application. The choice of external component values that will affect gain and low frequency response are discussed below.

The gain of each amplifier is set by resistors R_F and R_i for the non-inverting configuration shown in [Figure 1](#). The gain is found by [Equation \(3\)](#) below:

$$A_V = R_F / R_i \quad (\text{V/V}) \quad (3)$$

For best noise performance, lower values of resistors are used. A value of 1kΩ is commonly used for R_i and then setting the value of R_F for the desired gain. For the LME49811 the gain should be set no lower than 26dB. Gain settings below 26dB may experience instability.

The combination of R_i with C_i (see [Figure 1](#)) creates a high pass filter. The low frequency response is determined by these two components. The -3dB point can be found from [Equation \(4\)](#) shown below:

$$f_i = 1 / (2\pi R_i C_i) \quad (\text{Hz}) \quad (4)$$

If an input coupling capacitor is used to block DC from the inputs as shown in [Figure 1](#), there will be another high pass filter created with the combination of C_{IN} and R_{IN} . When using a input coupling capacitor R_{IN} is needed to set the DC bias point on the amplifier's input terminal. The resulting -3dB frequency response due to the combination of C_{IN} and R_{IN} can be found from [Equation \(5\)](#) shown below:

$$f_{IN} = 1 / (2\pi R_{IN} C_{IN}) \text{ (Hz)} \quad (5)$$

With large values of R_{IN} oscillations may be observed on the outputs when the inputs are left floating. Decreasing the value of R_{IN} or not letting the inputs float will remove the oscillations. If the value of R_{IN} is decreased then the value of C_{IN} will need to increase in order to maintain the same -3dB frequency response.

COMPENSATION CAPACITOR

The compensation capacitor (C_C) is one of the most critical external components in value, placement and type. The capacitor should be placed close to the LME49811 and a silver mica type will give good performance. The value of the capacitor will affect slew rate and stability. The highest slew rate is possible while also maintaining stability through out the power and frequency range of operation results in the best audio performance. The value shown in [Figure 1](#) should be considered a starting value with optimization done on the bench and in listening testing.

SUPPLY BYPASSING

The LME49811 has excellent power supply rejection and does not require a regulated supply. However, to eliminate possible oscillations all op amps and power op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as "motorboating" or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large electrolytic capacitor (10 μ F or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1 μ F) to prevent any high frequency feedback through the power supply lines. If adequate bypassing is not provided the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes low distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470 μ F or more.

OUTPUT STAGE USING BIPOLAR TRANSISTORS

With a properly designed output stage and supply voltage of $\pm 100V$, an output power up to 500W can be generated at 0.05% THD+N into an 8Ω speaker load. With an output current of several amperes, the output transistors need substantial base current drive because power transistors usually have quite low current gain—typical h_{FE} of 50 or so. To increase the current gain, audio amplifiers commonly use Darlington style devices or additional driver stages. Power transistors should be mounted together with the V_{BE} multiplier transistor on the same heat sink to avoid thermal run away. Please see the section [BIASING TECHNIQUES AND AVOIDING THERMAL RUNAWAY](#) for additional information.

BIASING TECHNIQUES AND AVOIDING THERMAL RUNAWAY

A class AB amplifier has some amount of distortion called Crossover distortion. To effectively minimize the crossover distortion from the output, a V_{BE} multiplier may be used instead of two biasing diodes. A V_{BE} multiplier normally consists of a bipolar transistor (Q_{MULT} , see [Figure 1](#)) and two resistors (R_{B1} and R_{B2} , see [Figure 1](#)). A trim pot can also be added in series with R_{B1} for optional bias adjustment. A properly designed output stage, combine with a V_{BE} multiplier, can eliminate the trim pot and virtually eliminate crossover distortion. The V_{CE} voltage of Q_{MULT} (also called BIAS of the output stage) can be set by following formula:

$$V_{BIAS} = V_{BE}(1 + R_{B2}/R_{B1}) \text{ (V)} \quad (6)$$

When using a bipolar output stage with the LME49811 (as in [Figure 1](#)), the designer must beware of thermal runaway. Thermal runaway is a result of the temperature dependence of V_{BE} (an inherent property of the transistor). As temperature increases, V_{BE} decreases. In practice, current flowing through a bipolar transistor heats up the transistor, which lowers the V_{BE} . This in turn increases the current gain, and the cycle repeats. If the system is not designed properly this positive feedback mechanism can destroy the bipolar transistors used in the output stage. One of the recommended methods of preventing thermal runaway is to use the same heat sink on the bipolar output stage transistor together with V_{BE} multiplier transistor. When the V_{BE} multiplier transistor is mounted to the same heat sink as the bipolar output stage transistors, its temperature will track that of the output transistors. Its V_{BE} is dependent upon temperature as well, and so it will draw more current as the output

transistors heat up, reducing the bias voltage to compensate. This will limit the base current into the output transistors, which counteracts thermal runaway. Another widely popular method of preventing thermal runaway is to use low value emitter degeneration resistors (R_{E1} and R_{E2}). As current increases, the voltage at the emitter also increases, which decreases the voltage across the base and emitter. This mechanism helps to limit the current and counteracts thermal runaway.

LAYOUT CONSIDERATION AND AVOIDING GROUND LOOPS

A proper layout is virtually essential for a high performance audio amplifier. It is very important to return the load ground, supply grounds of output transistors, and the low level (feedback and input) grounds to the circuit board common ground point through separate paths. When ground is routed in this fashion, it is called a star ground or a single point ground. It is advisable to keep the supply decoupling capacitors of $0.1\mu\text{F}$ close as possible to LME49811 to reduce the effects of PCB trace resistance and inductance. Following the general rules will optimize the PCB layout and avoid ground loops problems:

- Make use of symmetrical placement of components.
- Make high current traces, such as output path traces, as wide as possible to accommodate output stage current requirement.
- To reduce the PCB trace resistance and inductance, same ground returns paths should be as short as possible. If possible, make the output traces short and equal in length.
- To reduce the PCB trace resistance and inductance, ground returns paths should be as short as possible.
- If possible, star ground or a single point ground should be observed. Advanced planning before starting the PCB can improve audio performance.

Demonstration Board Layout

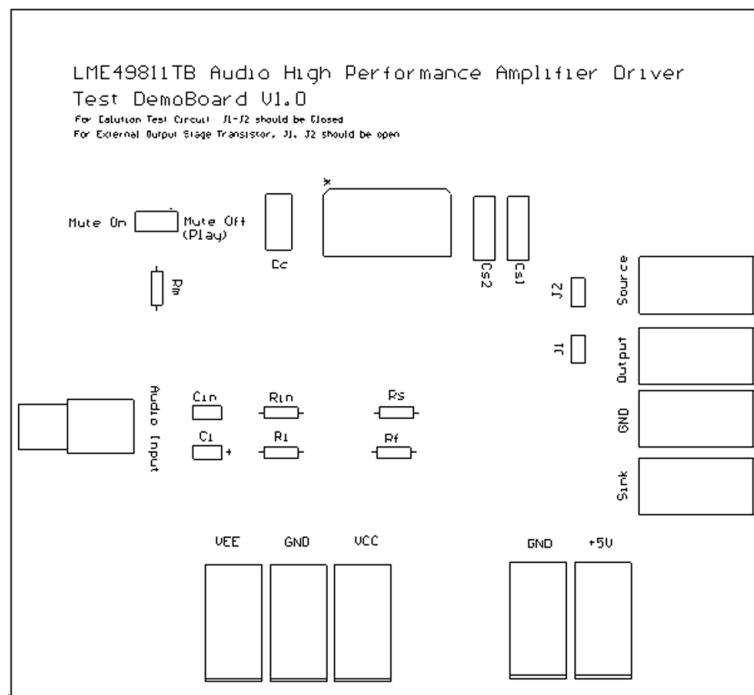


Figure 28. Silkscreen Layer

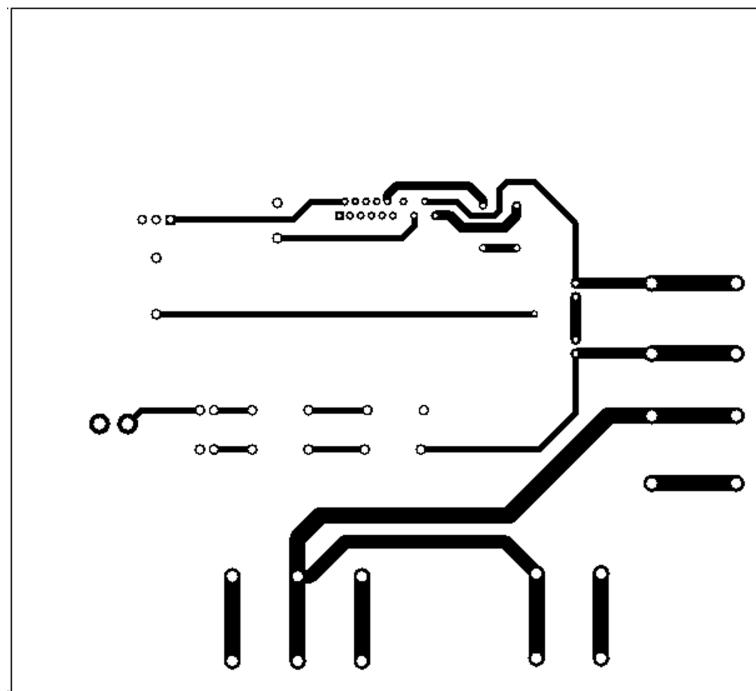


Figure 29. Top Layer

Figure 30. Bottom Layer

REVISION HISTORY

Rev	Date	Description
1.0	12/19/07	Initial release.
1.01	01/04/08	Edited the project title (replaced “Driver” with “Power Amplifier Input Stage”).
1.02	11/11/09	Fixed the spacing between the equations 3, 4, 5, and 6 to the units measures.
C	04/05/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49811TB/NOPB	OBsolete	TO-OTHER	NDN	15		TBD	Call TI	Call TI	-20 to 75	LME49811 TB	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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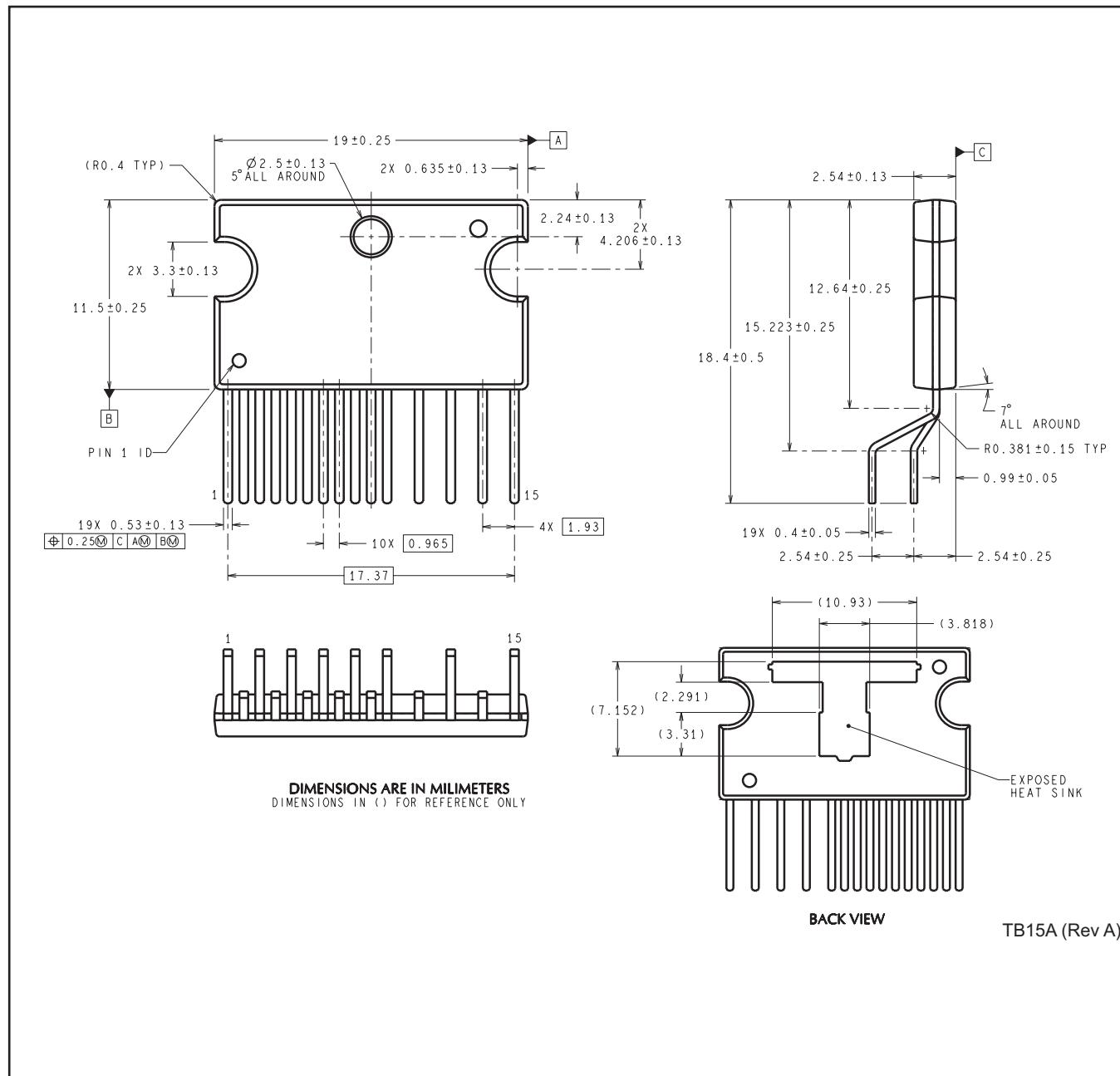
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PACKAGE OPTION ADDENDUM

14-Oct-2016

MECHANICAL DATA

NDN0015A



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