TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# **TC75W60FU, TC75W60FK**

**Dual Operational Amplifier** 

### **Features**

• High slew rate : SR  $(V_{DD} = 3 \text{ V}) = 5.1 \text{ V/}\mu\text{s}$  (typ.)

• Single and dual power Supply operations are possible.

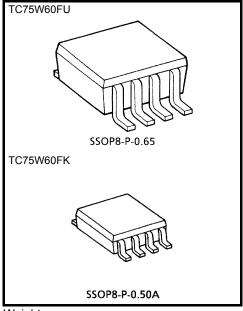
:  $V_{DD} = \pm 0.9$  to 3.5 V or 1.8 to 7 V

Lower supply current than general-purpose bipolar type op amps

:  $I_{DD}$  ( $V_{DD}$  = 3 V) = 660  $\mu$ A (typ.)

• The internally phase compensated operational amplifier.

Small package



Weight

SSOP8-P-0.65 : 0.021 g (typ.) SSOP8-P-0.50A : 0.01 g (typ.)

### **Absolute Maximum Ratings (Ta = 25°C)**

Characteristics		Symbol	Rating	Unit	
Supply voltage		V <sub>DD</sub> , V <sub>SS</sub>	7	V	
Differential input voltage		DV <sub>IN</sub>	± 7	٧	
Input voltage		V <sub>IN</sub>	$V_{DD}$ to $V_{SS}$	<b>V</b>	
Power dissipation	TC75W60FU	D-	250	mW	
	TC75W60FK	P <sub>D</sub>	200	11100	
Operating temperature		T <sub>opr</sub>	-40 to 85	°C	
Storage temperature		T <sub>stg</sub> –55 to 125		°C	

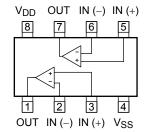
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

# Marking (top view)

# TC75W60FU Type name TC75W60FK 8 7 6 5 Lot No. 5 W 6 0 1 2 3 4

# Pin Connection (top view)



# **Electrical Characteristics**

# DC Characteristics ( $V_{DD} = 3.0 \text{ V}, V_{SS} = GND, Ta = 25^{\circ}\text{C}$ )

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Input offset voltage	V <sub>IO</sub>	_	$R_S = 1 k\Omega$	_	2	7	mV
Input offset current	I <sub>IO</sub>	_	_	_	1	_	pА
Input bias current	lį	_	_	_	1	_	pA
Common mode input voltage	CMV <sub>IN</sub>	_	_	0.0	_	2.1	V
Voltage gain (open loop)	G <sub>V</sub>	_	_	60	70	_	dB
Maximum output voltage	V <sub>OH</sub>	_	$R_L = 100 \text{ k}\Omega$	2.9	_	_	V
	V <sub>OL</sub>	_	$R_L = 100 \text{ k}\Omega$	_	_	0.1	V
Common mode rejection ratio	CMRR	_	V <sub>IN</sub> = 0.0 to 2.1 V	54	70	_	dB
Suuply voltage rejection ratio	SVRR	_	V <sub>DD</sub> = 1.8 to 7.0 V	60	70	_	dB
Supply current	I <sub>DD</sub>	_	_	_	660	1000	μА
Source current	I <sub>source</sub>	_	_	330	700	_	μА
Sink current	I <sub>sink</sub>	_	_	600	1250	_	μΑ

# DC Characteristics (V<sub>DD</sub> = 1.8 V, V<sub>SS</sub> = GND, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Input offset voltage	V <sub>IO</sub>	_	$R_S = 1 k\Omega$	_	2	7	mV
Input offset current	I <sub>IO</sub>	_	_	_	1	_	pA
Input bias current	lı	_	_	_	1	_	pA
Common mode input voltage	CMV <sub>IN</sub>	_	_	0.3	_	0.9	V
Voltage gain (open loop)	G <sub>V</sub>	_	_	_	70	_	dB
maximum output voltage	V <sub>OH</sub>	_	$R_L = 100 \text{ k}\Omega$	1.7	_	_	V
	V <sub>OL</sub>	_	$R_L = 100 \text{ k}\Omega$	_	_	0.1	
Common mode rejection ratio	CMRR	_	V <sub>IN</sub> = 0.3 to 0.9 V	50	60	_	dB
Supply current	I <sub>DD</sub>	_	_	_	600	900	μΑ
Source current	I <sub>source</sub>		_	300	700	_	μА
Sink current	I <sub>sink</sub>		_	550	1150	_	μА

# AC Characteristics ( $V_{DD} = 3.0 \text{ V}, V_{SS} = \text{GND}, Ta = 25^{\circ}\text{C}$ )

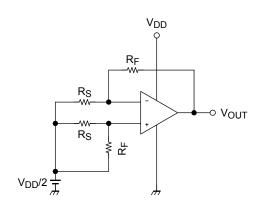
Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Slew rate	SR	_	_	_	5.1	_	V/μs
Unity gain cross frequency	f <sub>T</sub>	_	_	_	3.7	_	MHz

# AC Characteristics ( $V_{DD} = 1.8 \text{ V}, V_{SS} = GND, Ta = 25^{\circ}\text{C}$ )

Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Slew rate	SR	_	_	_	4.0	_	V/μs
Unity gain cross frequency	f <sub>T</sub>	_	_		3.0	_	MHz

## **TEST CIRCUIT**

### (1) SVRR, VIO



SVRR

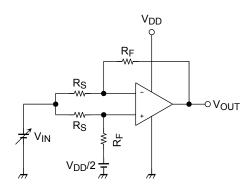
$$V_{DD} = 1.5 \text{ V}$$
 :  $V_{DD} = V_{DD}1$ ,  $V_{OUT} = V_{OUT}1$   
 $V_{DD} = 7.0 \text{ V}$  :  $V_{DD} = V_{DD}2$ ,  $V_{OUT} = V_{OUT}2$ 

$$SVRR = 20 \ log \left( \left| \frac{V_OUT^{1-}V_{OUT}^{2}}{V_{DD}^{1-}V_{DD}^{2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

• V<sub>IO</sub>

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

### (2) CMRR, CMVIN



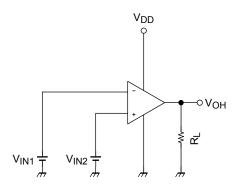
CMRR

$$V_{IN} = 0.0 \text{ V}$$
 :  $V_{IN} = V_{DD}1$ ,  $V_{OUT} = V_{OUT}1$   
 $V_{IN} = 2.5 \text{ V}$  :  $V_{IN} = V_{DD}2$ ,  $V_{OUT} = V_{OUT}2$ 

$$CMRR = 20 \log \left( \left| \frac{V_{OUT}1 - V_{OUT}2}{V_{IN}1 - V_{IN}2} \right| \times \frac{R_S}{R_F + R_S} \right)$$

CMV<sub>IN</sub>

# (3) VOH

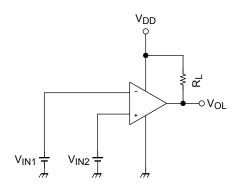


# $V_{\mathsf{OH}}$

$$V_{IN1} = \frac{V_{DD}}{2} - 0.05 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.05 \text{ V}$$

# (4) VOL

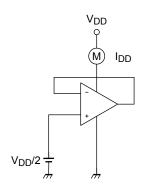


# $V_{\mathsf{OL}}$

$$V_{IN1} = \frac{V_{DD}}{2} + 0.05 \text{ V}$$

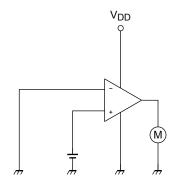
$$V_{IN2} = \frac{V_{DD}}{2} - 0.05 \text{ V}$$

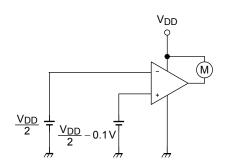
# (5) IDD

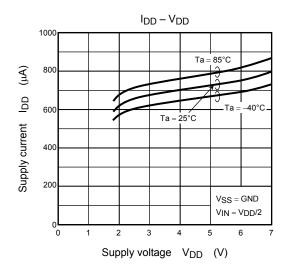


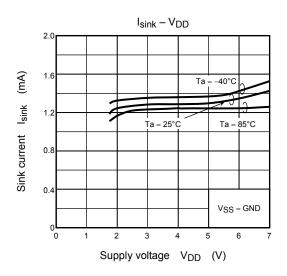


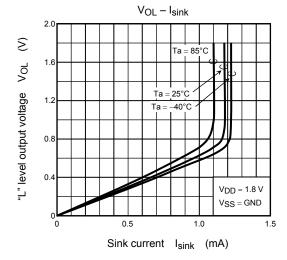


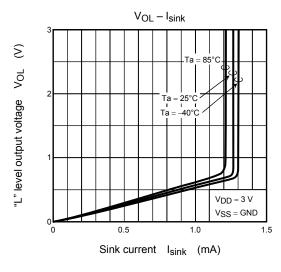


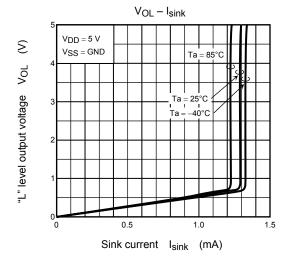


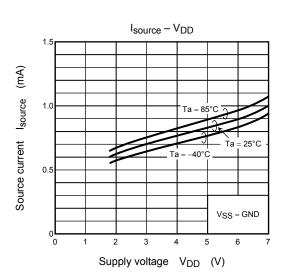




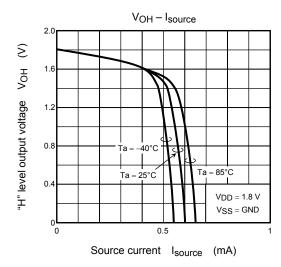


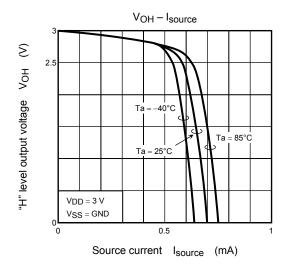


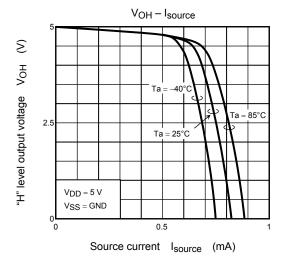


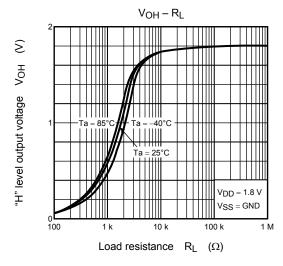


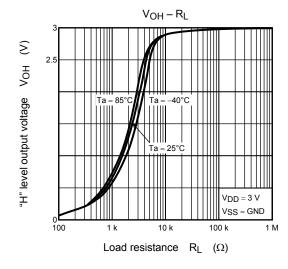
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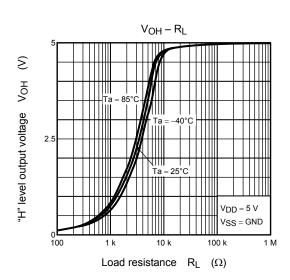


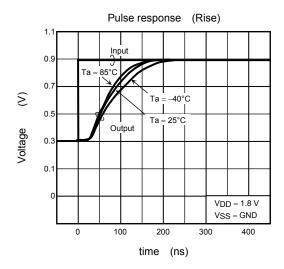


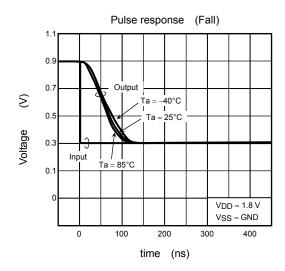


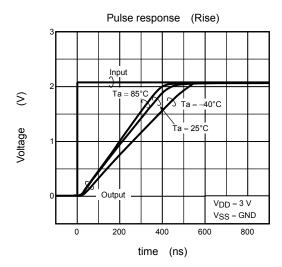


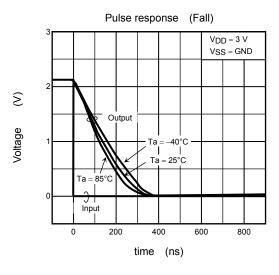


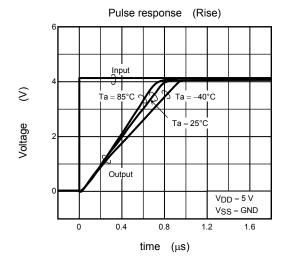


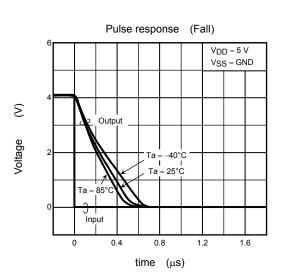


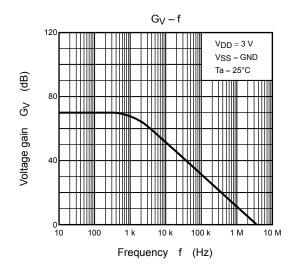


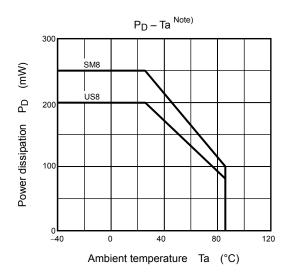












Note):

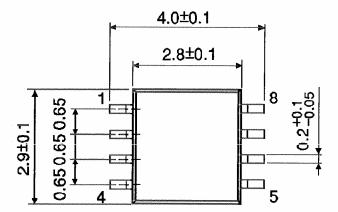
These power dissipation curves are given by measurement of only IC on the air and, in general, it become higher when mounted on PCB.

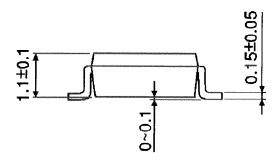
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Since the power dissipation depends on mounted condition, please be sure to design.

# **Package Dimensions**

SSOP8-P-0.65 Unit: mm





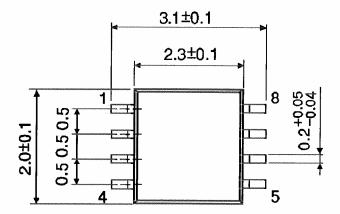
Weight: 0.021 g (typ.)

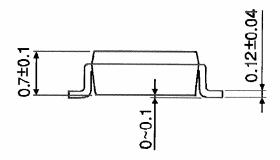
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# **Package Dimensions**

SSOP8-P-0.50A Unit: mm





Weight: 0.01 g (typ.)

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