

CD4051B, CD4052B, CD4053B Types

CMOS Analog Multiplexers/Demultiplexers*

With Logic-Level Conversion

High-Voltage Types (20-Volt Rating)

- CD4051B – Single 8-Channel
- CD4052B – Differential 4-Channel
- CD4053B – Triple 2-Channel

RCA-CD4051B, CD4052B, and CD4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if $V_{DD}-V_{SS} = 3$ V, a $V_{DD}-V_{EE}$ of up to 13 V can be controlled; for $V_{DD}-V_{EE}$ level differences above 13 V, a $V_{DD}-V_{SS}$ of at least 4.5 V is required). For example, if $V_{DD} = +4.5$ V, $V_{SS} = 0$, and $V_{EE} = -13.5$ V, analog signals from -13.5 V to $+4.5$ V can be controlled by digital inputs of 0 to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

The CD4051B is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

The CD4051B, CD4052B, and CD4053B are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

* When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating

Features:

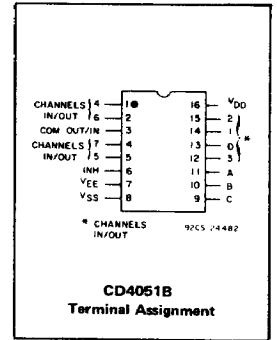
- Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 V_{p-p}
- Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for $V_{DD}-V_{EE} = 15$ V
- High OFF resistance: channel leakage of ± 100 pA (typ.) @ $V_{DD}-V_{EE} = 18$ V
- Logic-level conversion for digital addressing signals of 3 to 20 V ($V_{DD}-V_{SS} = 3$ to 20 V) to switch analog signals to 20 V p-p ($V_{DD}-V_{EE} = 20$ V); see introductory text
- Matched switch characteristics: $R_{ON} = 5 \Omega$ (typ.) for $V_{DD}-V_{EE} = 15$ V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μ W (typ.) @ $V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10$ V
- Binary address decoding on chip
- 5-, 10-, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Break-before-make switching eliminates channel overlap

RECOMMENDED OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$ (Unless Otherwise Specified)

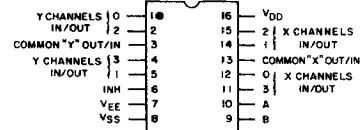
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

CHARACTERISTIC	V_{DD}	Min.	Max.	Units
Supply-Voltage Range ($T_A = \text{Full Package-Temp. Range}$)	—	3	18	V
Multiplexer Switch Input Current Capability*	—	—	25	mA
Output Load Resistance	—	100	—	Ω

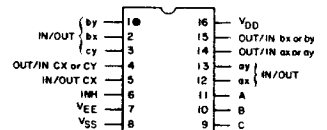
* In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 3 on the CD4051; terminals 3 and 13 on the CD4052; terminals 4, 14, and 15 on the CD4053.



CD4051B
Terminal Assignment



CD4052B
Terminal Assignment



CD4053B
Terminal Assignment

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MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} or V_{EE} , whichever is more negative)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

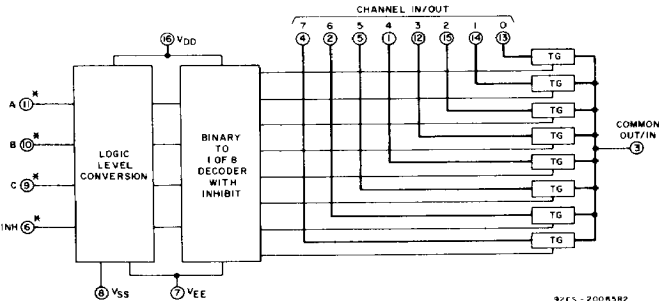


Fig. 1 - Functional diagram of CD4051B.

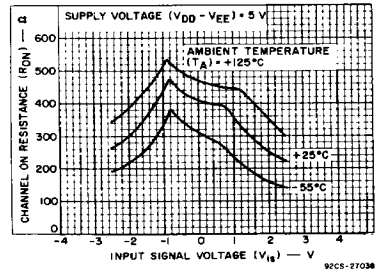


Fig. 4 - Typical channel ON resistance vs input signal voltage (all types).

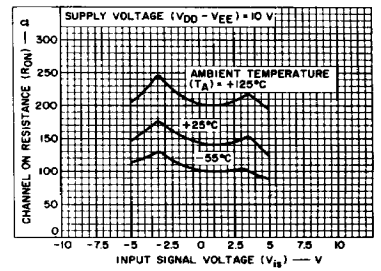


Fig. 5 - Typical channel ON resistance vs. input signal voltage (all types).

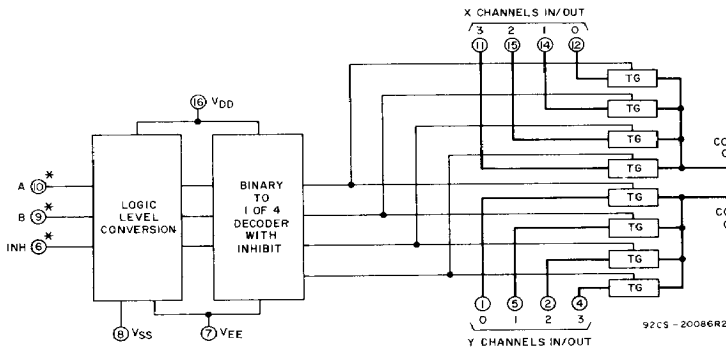


Fig. 2 - Functional diagram of CD4052B.

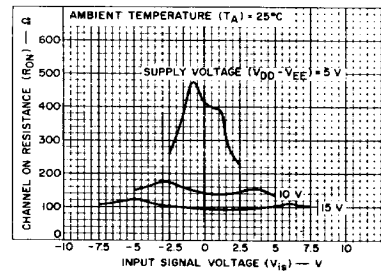


Fig. 6 - Typical channel ON resistance vs. input signal voltage (all types).

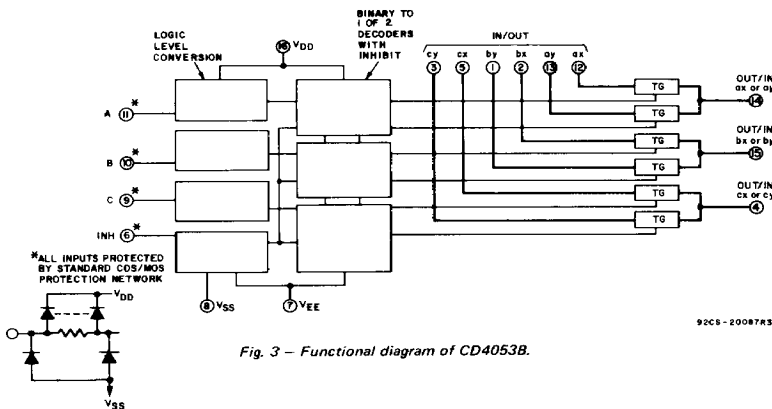


Fig. 3 - Functional diagram of CD4053B.

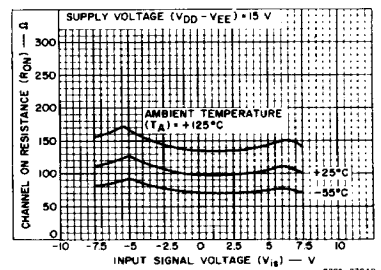


Fig. 7 - Typical channel ON resistance vs. input signal voltage (all types).

CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS				LIMITS at Indicated Temperature (°C)						Units	
	V_{is}	V_{EE}	V_{SS}	V_{DD}	Values at -55, +25, +125 Apply to D, F, K, H Pkgs. Values at -40, +25, +85 apply to E pkgs.							
	(V)	(V)	(V)	(V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.		
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{Os})												
Quiescent Device Current, I_{DD} Max.				5	5	5	150	150	-	0.04	5	μA
				10	10	10	300	300	-	0.04	10	
				15	20	20	600	600	-	0.04	20	
On-State Resistance $0 \leq V_{is} \leq V_{DD}$ r_{on} Max.				5	800	850	1200	1300	-	470	1050	Ω
				10	310	330	520	550	-	180	400	
				15	200	210	300	320	-	125	240	
Change in On-State Resistance (Between Any Two Channels) Δr_{on}				5	-	-	-	-	-	15	-	Ω
				10	-	-	-	-	-	10	-	
				15	-	-	-	-	-	5	-	
OFF Channel Leakage Current: Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max.				18	$\pm 100^*$		$\pm 1000^*$			± 0.01	$\pm 100^*$	nA
Capacitance: Input, C_{is} Output, C_{os} CD4051 CD4052 CD4053 Feedthrough, C_{ios}				5	-	-	-	-	-	5	-	pF
			5	-	-	-	-	-	30	-		
			5	-	-	-	-	-	18	-		
			5	-	-	-	-	-	9	-		
Propagation Delay Time (Signal Input to Output)	V_{DD}	$R_1 = 200 k\Omega$ $C_L = 50 pF$ $t_r, t_f = 20 ns$		5	-	-	-	-	-	30	60	ns
				10	-	-	-	-	-	15	30	
				15	-	-	-	-	-	10	20	

* Determined by minimum feasible leakage measurement for automatic testing.

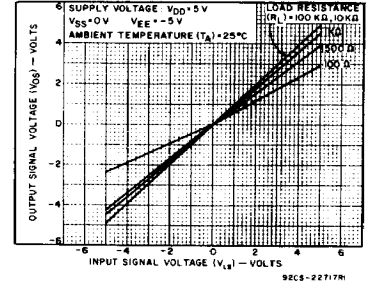


Fig.8 - Typical ON characteristics for 1 of 8 channels (CD4051B).

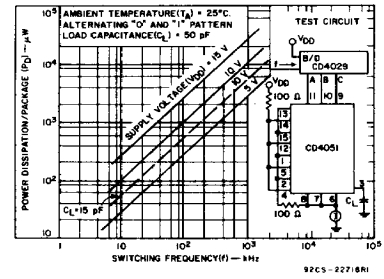


Fig.9 - Typical dynamic power dissipation vs. switching frequency (CD4051B).

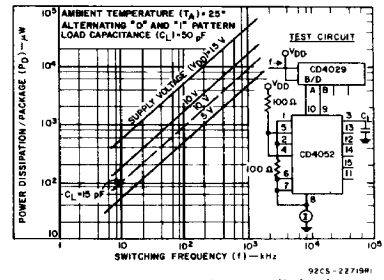


Fig.10 - Typical dynamic power dissipation vs. switching frequency (CD4052B).

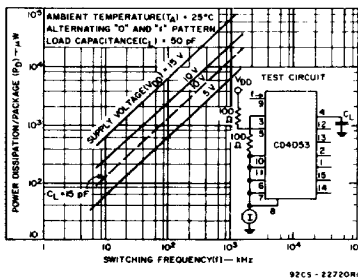
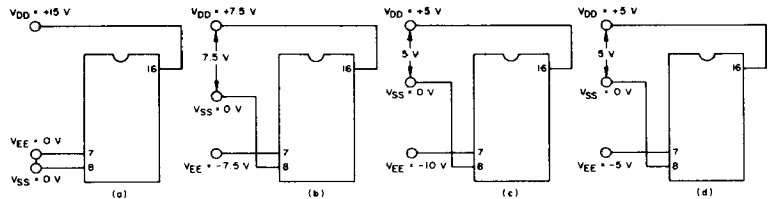


Fig.11 - Typical dynamic power dissipation vs. switching frequency (CD4053B).



The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD} . The analog signal (through the TG) may swing from V_{EE} to V_{DD} .

Fig.12 - Typical bias voltages.

CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS				LIMITS at Indicated Temperature (°C)							Units	
	V _{is} (V)	V _{EE} (V)	V _{SS} (V)	V _{DD} (V)	Values at -55, +25, +125 Apply to D, F, K, H, Pkg Values at -40, +25, +85, apply to E pkg								
					-55	-40	+85	+125	+25				
											Min.	Typ.	Max.
CONTROL (ADDRESS or INHIBIT) V_C													
Input Low Voltage, V _{IL} Max.	=V _{DD} thru 1 kΩ	V _{EE} =V _{SS} R _L =1 kΩ to V _{SS} I _{IS} < 2 μA on all OFF Channels	5	1.5				--	--	1.5		V	
			10	3				--	--	3			
			15	4				--	--	4			
Input High Voltage, V _{IH} Min.			5	3.5				3.5		--	--		
			10	7				7		--	--		
			15	11				11		--	--		
Input Current, I _{IN} Max.	V _{IN} = 0, 18		18	±0.1	±0.1	±1	±1	--	±10 ⁻⁵	±0.1	μA		
Propagation Delay Time: Address-to-Signal OUT (Channels ON or OFF) See Figs. 14, 15, 18	t _r , t _f = 20 ns, C _L = 50 pF R _L = 1 kΩ												
	0	0	5	--	--	--	--	--	450	720	ns		
	0	0	10	--	--	--	--	--	160	320			
	0	0	15	--	--	--	--	--	120	240			
	-5	0	5	--	--	--	--	--	225	450			
Inhibit-to-Signal OUT (Channel turning ON) See Fig. 14	R _L = 1 kΩ, C _L = 50 pF t _r , t _f = 20 ns												
	0	0	5	--	--	--	--	--	400	720	ns		
	0	0	10	--	--	--	--	--	160	320			
	0	0	15	--	--	--	--	--	120	240			
	-10	0	5	--	--	--	--	--	200	400			
Inhibit-to-Signal OUT (Channel turning OFF) See Fig. 15	R _L = 1 kΩ, C _L = 50 pF t _r , t _f = 20 ns												
	0	0	5	--	--	--	--	--	200	450	ns		
	0	0	10	--	--	--	--	--	90	210			
	0	0	15	--	--	--	--	--	70	160			
	-10	0	5	--	--	--	--	--	130	300			
Input Capacitance, C _{IN} (Any Address or Inhibit Input)			--	--	--	--	--	--	5	7.5	pF		

INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE
CD4052B				
INHIBIT	B	A		
0	0	0	0x, 0y	
0	0	1	1x, 1y	
0	1	0	2x, 2y	
0	1	1	3x, 3y	
1	X	X	NONE	
CD4053B				
INHIBIT	A or B or C			
0	0	ax or bx or cx		
0	1	ay or by or cy		
1	X	NONE		

X = Don't care

Fig. 13 - Truth tables.

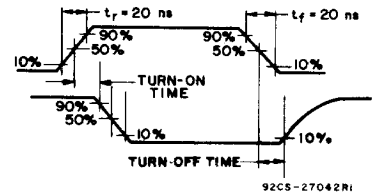


Fig. 14 - Waveforms, channel being turned ON (R_L = 1 kΩ).

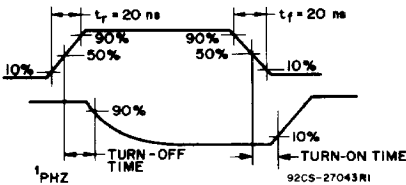


Fig. 15 - Waveforms, channel being turned OFF (R_L = 1 kΩ).

TEST CIRCUITS

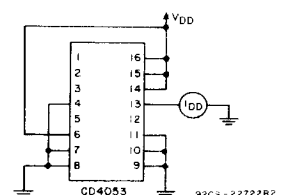
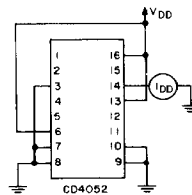
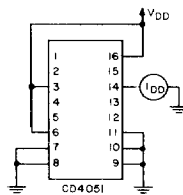


Fig. 16 - OFF channel leakage current - any channel OFF.

CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
	V _{is} (V)	V _{DD} (V)	R _L (kΩ)	TYPICAL VALUE		
Cutoff (-3-dB) Frequency Channel ON (Sine Wave Input)	5*	10	1	CD4053	30	MHz
	V _{EE} = V _{SS} .			CD4052	25	
	20 log $\frac{V_{os}}{V_{is}} = -3\text{dB}$			CD4051	20	
	V _{os} at Any Channel				60	
Total Harmonic Distortion, THD	2*	5	10		0.3	%
	3*	10			0.2	
	5*	15			0.12	
	V _{EE} = V _{SS} , f _{is} = 1 kHz sine wave					
-40-dB Feedthrough Frequency (All Channels OFF)	5*	10	1	CD4053	8	MHz
	V _{EE} = V _{SS} .			CD4052	10	
	20 log $\frac{V_{os}}{V_{is}} = -40\text{dB}$			CD4051	12	
	V _{os} at Any Channel				8	
-40-dB Signal Crosstalk Frequency	5*	10	1	Between Any 2 Channels		MHz
				Measured on Common	3	
	V _{EE} = V _{SS} .			Measured on Any Channel	6	
	20 log $\frac{V_{os}}{V_{is}} = -40\text{dB}$			Between Any 2 Sections CD4052 Only	10	
				Between Any 2 Sections CD4053 Only	In Pin 2, Out Pin 14: 2.5 In Pin 15, Out Pin 14: 6	
Address-or-Inhibit-to Signal Crosstalk	-	10	10#		65	mV (Peak)
V _{EE} =0, V _{SS} =0, t _r , t _f = 20 ns, V _C = V _{DD} - V _{SS} (Square Wave)						

* Peak-to-peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$

2

Both ends of channel

TEST CIRCUITS (Cont'd)

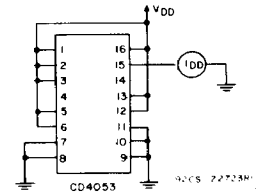
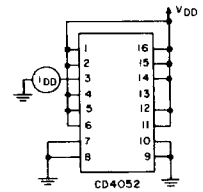
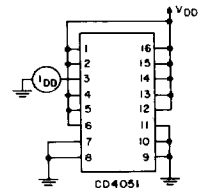


Fig. 17 - OFF channel leakage current - all channels OFF.

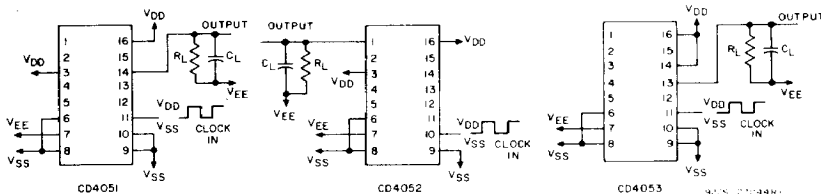


Fig. 18 - Propagation delay - address input to signal output.

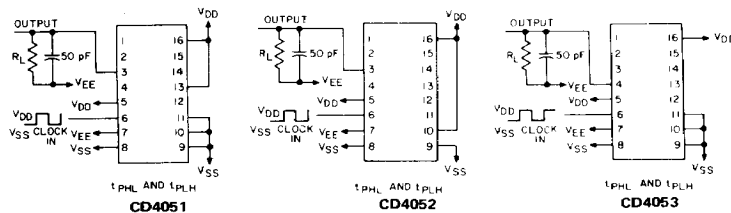


Fig. 19 - Propagation delay - inhibit input to signal output.

CD4051B, CD4052B, CD4053B Types

TEST CIRCUITS (Cont'd)

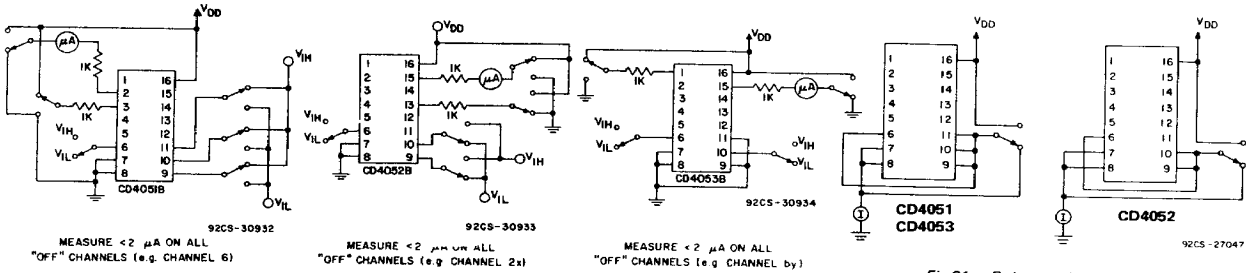


Fig. 20 - Input voltage test circuits (noise immunity).

Fig. 21 - Quiescent device current.

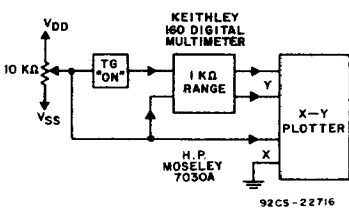


Fig. 22 - Channel ON resistance measurement circuit.

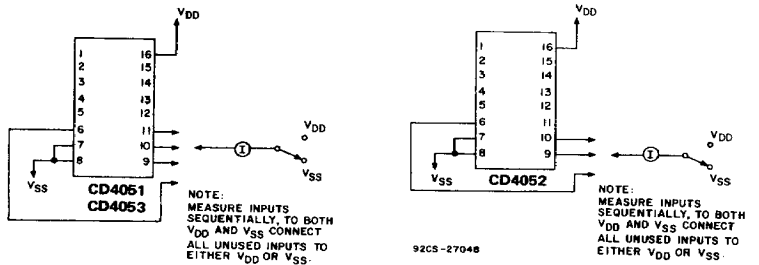


Fig. 23 - Input current.

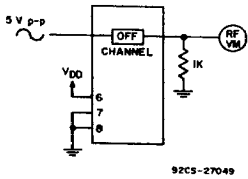


Fig. 24 - Feedthrough (all types).

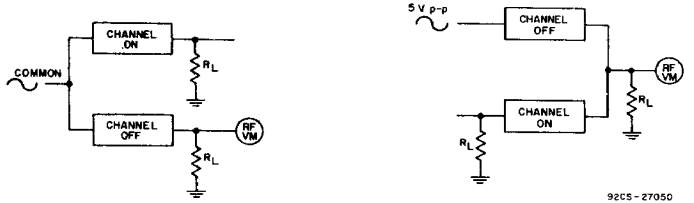


Fig. 25 - Crosstalk between any two channels (all types).

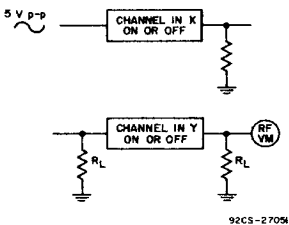


Fig. 26 - Crosstalk between duals or triplets (CD4052B, CD4053B).

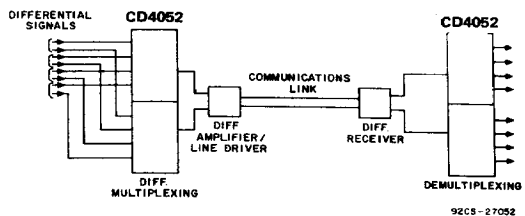
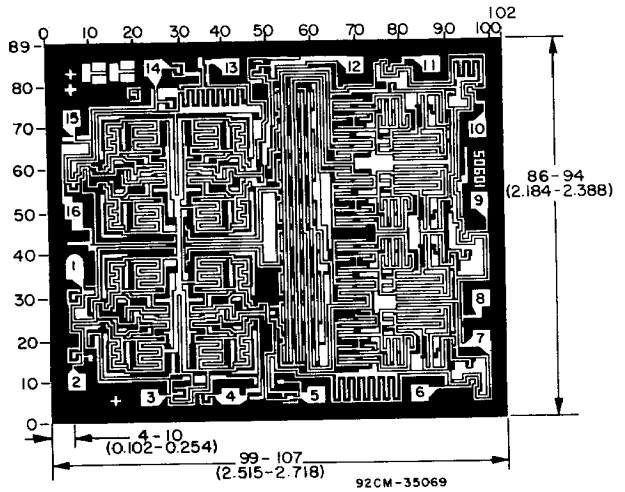


Fig. 27 - Typical time-division application of the CD4052B.

CD4051B, CD4052B, CD4053B Types

SPECIAL CONSIDERATIONS

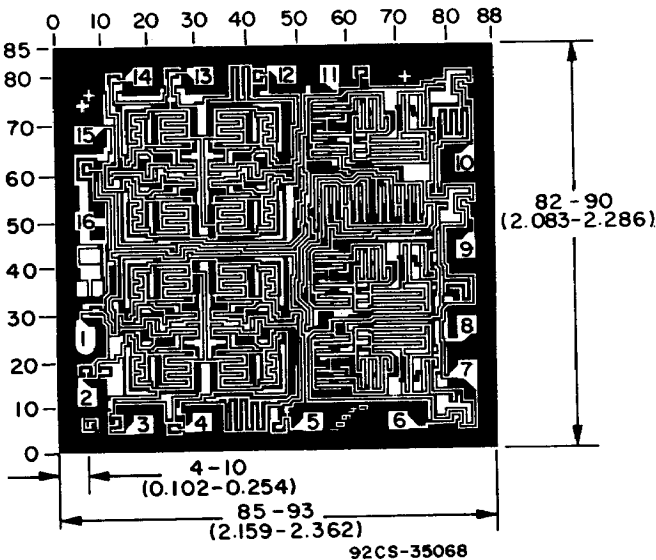
In applications where separate power sources are used to drive VDD and the signal inputs, the VDD current capability should exceed VDD/RL (RL = effective external load). This provision avoids permanent current flow or clamping action on the VDD supply when power is applied or removed from the CD4051B, CD4052B, or CD4053B.



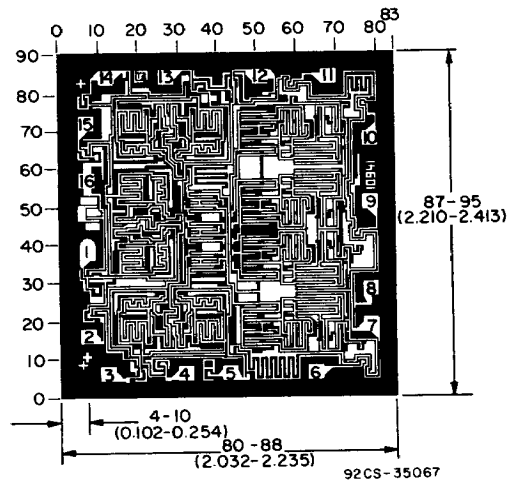
Dimensions and pad layout for CD4051BH.

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations are in Mils (10^{-3} inch).



Dimensions and pad layout for CD4052BH.



Dimensions and pad layout for CD4053BH.