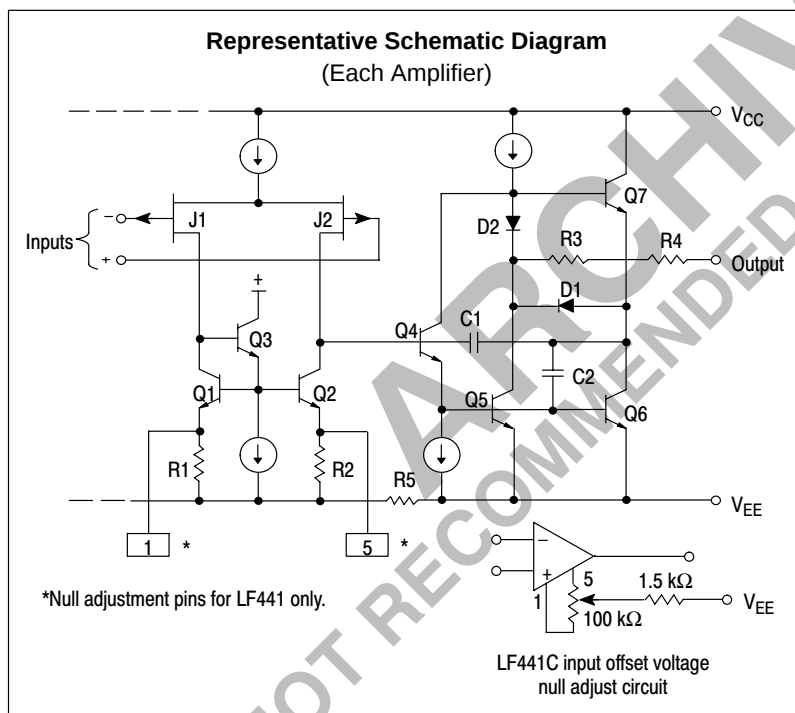


Low Power JFET Input Operational Amplifiers

These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing. The LF441C device provides for the external null adjustment of input offset voltage.

These devices are specified over the commercial temperature range. All are available in plastic dual in-line and SOIC packages.

- Low Supply Current: 200 μ A/Amplifier
- Low Input Bias Current: 5.0 pA
- High Gain Bandwidth: 2.0 MHz
- High Slew Rate: 6.0 V/ μ s
- High Input Impedance: $10^{12} \Omega$
- Large Output Voltage Swing: ± 14 V
- Output Short Circuit Protection



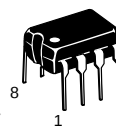
ORDERING INFORMATION

Device	Function	Operating Temperature Range	Package
LF441CD LF441CN	Single	$T_A = 0^\circ \text{ to } +70^\circ \text{C}$	SO-8 Plastic DIP
LF442CD LF442CN	Dual		SO-8 Plastic DIP
LF444CD LF444CN	Quad		SO-14 Plastic DIP

LF441C LF442C LF444C

LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

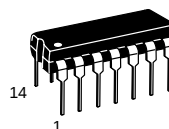
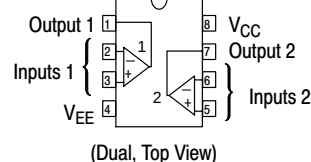
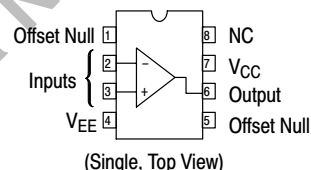


N SUFFIX
PLASTIC PACKAGE
CASE 626

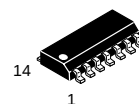


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

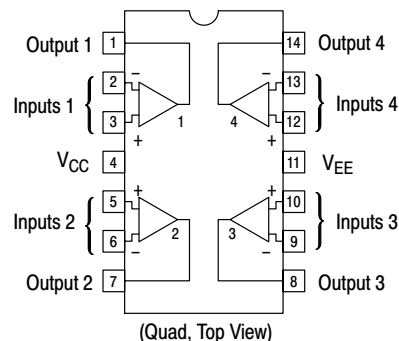


N SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



LF441C LF442C LF444C

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	± 30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	± 15	V
Output Short Circuit Duration (Note 3)	t_{SC}	Indefinite	sec
Operating Junction Temperature (Note 3)	T_J	+150	°C
Storage Temperature Range	T_{stg}	-60 to +150	°C

- NOTES:** 1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 V, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = 0^\circ$ to 70° C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10$ k Ω , $V_O = 0$ V) Single: $T_A = +25^\circ$ C $T_A = 0^\circ$ to $+70^\circ$ C Dual: $T_A = +25^\circ$ C $T_A = 0^\circ$ to $+70^\circ$ C Quad: $T_A = +25^\circ$ C $T_A = 0^\circ$ to $+70^\circ$ C	V_{IO}	— — — — — —	3.0 — 3.0 — 3.0 —	5.0 7.5 5.0 7.5 10 12	mV
Average Temperature Coefficient of Offset Voltage ($R_S = 10$ k Ω , $V_O = 0$ V)	$\Delta V_{IO}/\Delta T$	—	10	—	μ V/°C
Input Offset Current ($V_{CM} = 0$ V, $V_O = 0$ V) $T_A = +25^\circ$ C $T_A = 0^\circ$ to $+70^\circ$ C	I_{IO}	— —	0.5 —	50 1.5	pA nA
Input Bias Current ($V_{CM} = 0$ V, $V_O = 0$ V) $T_A = +25^\circ$ C $T_A = 0^\circ$ to $+70^\circ$ C	I_{IB}	— —	3.0 —	100 3.0	pA nA
Common Mode Input Voltage Range ($T_A = +25^\circ$ C)	V_{ICR}	— -11	+14.5 -12	+11 —	V
Large Signal Voltage Gain ($V_O = \pm 10$ V, $R_L = 10$ k Ω) $T_A = +25^\circ$ C $T_A = 0^\circ$ to $+70^\circ$ C	A_{VOL}	25 15	60 —	— —	V/mV
Output Voltage Swing ($R_L = 10$ k Ω)	$V_O +$ $V_O -$	+12 —	+14 -14	— -12	V
Common Mode Rejection ($R_S \leq 10$ k Ω , $V_{CM} = V_{ICR}$, $V_O = 0$ V)	CMR	70	86	—	dB
Power Supply Rejection ($R_S = 100$ Ω , $V_{CM} = 0$ V, $V_O = 0$ V)	PSR	70	84	—	dB
Power Supply Current (No Load, $V_O = 0$ V) Single Dual Quad	I_D	— — —	200 400 800	250 500 1000	μ A

LF441C LF442C LF444C

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V to }+10\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$, $A_V = +1.0$)	SR	0.6	6.0	—	V/ μs
Settling Time ($A_V = -1.0$, $R_L = 10\text{ k}\Omega$, $V_O = 0\text{ V to }+10\text{ V}$)	t_s	—	1.6 2.2	—	μs
Gain Bandwidth Product ($f = 200\text{ kHz}$)	GBW	0.6	2.0	—	MHz
Equivalent Input Noise Voltage ($R_S = 100\text{ }\Omega$, $f = 1.0\text{ kHz}$)	e_n	—	47	—	nV/ $\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	i_n	—	0.01	—	pA/ $\sqrt{\text{Hz}}$
Input Resistance	R_i	—	10^{12}	—	Ω
Channel Separation ($f = 1.0\text{ Hz to }20\text{ kHz}$)	CS	—	120	—	dB

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

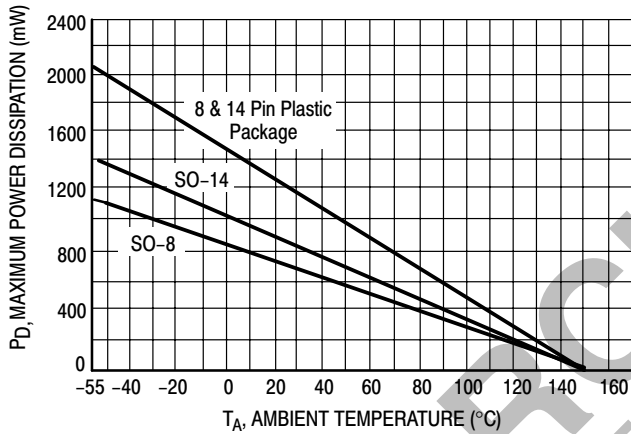


Figure 2. Input Bias Current versus Input Common Mode Voltage

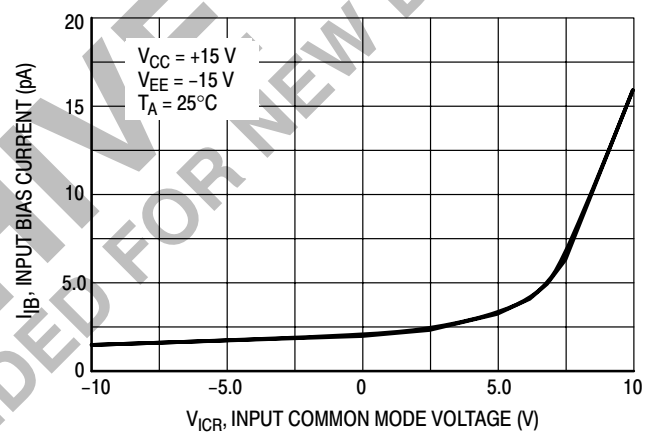


Figure 3. Input Bias Current versus Temperature

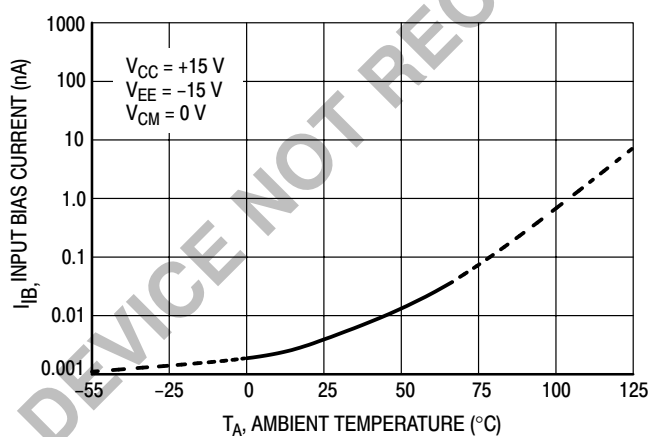


Figure 4. Supply Current versus Supply Voltage

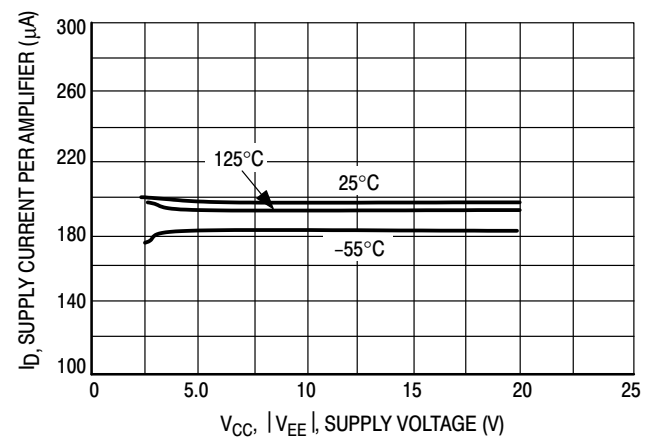


Figure 5. Positive Input Common Mode Voltage Range versus Positive Supply Voltage

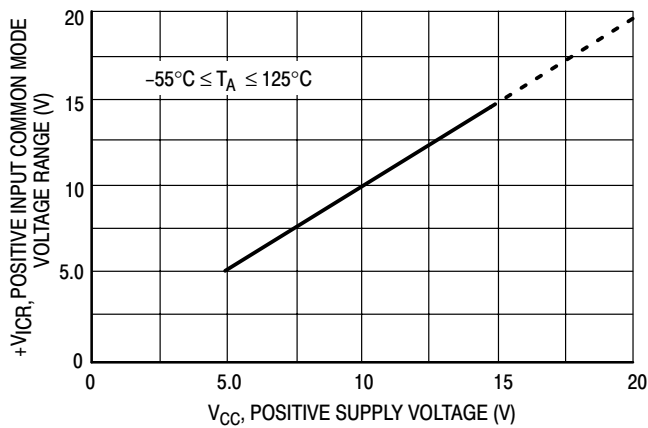


Figure 6. Negative Input Common Mode Voltage Range versus Negative Supply Voltage

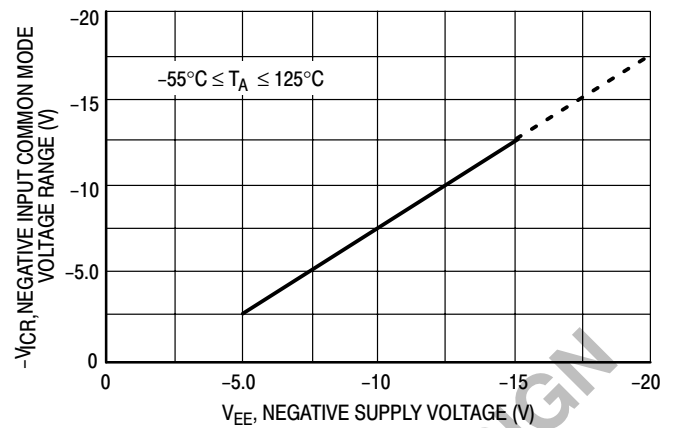


Figure 7. Output Voltage versus Output Source Current

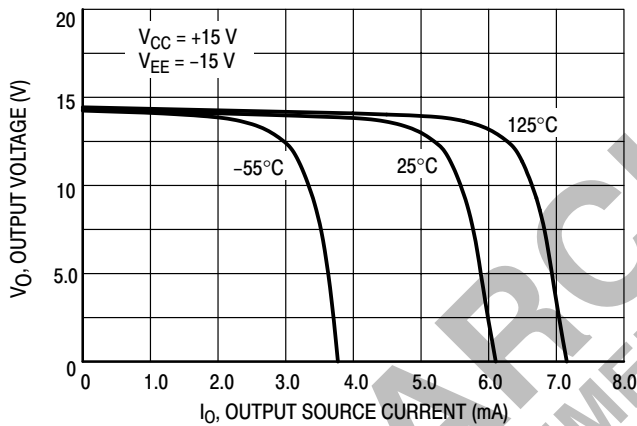


Figure 8. Output Voltage versus Output Sink Current

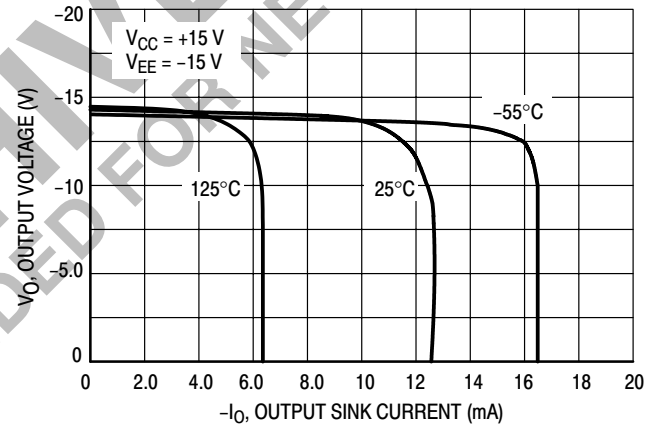


Figure 9. Output Voltage Swing versus Supply Voltage

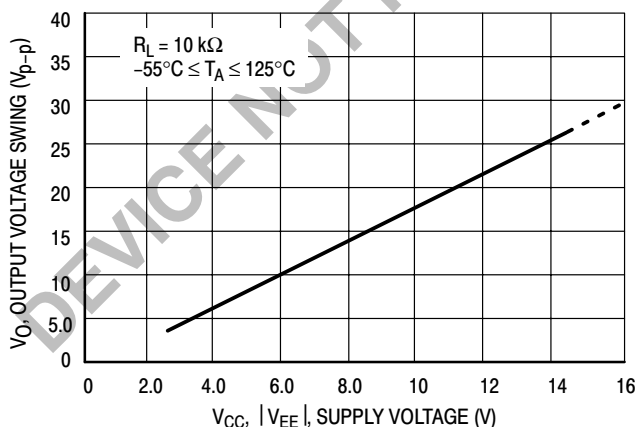


Figure 10. Output Voltage Swing versus Load Resistance

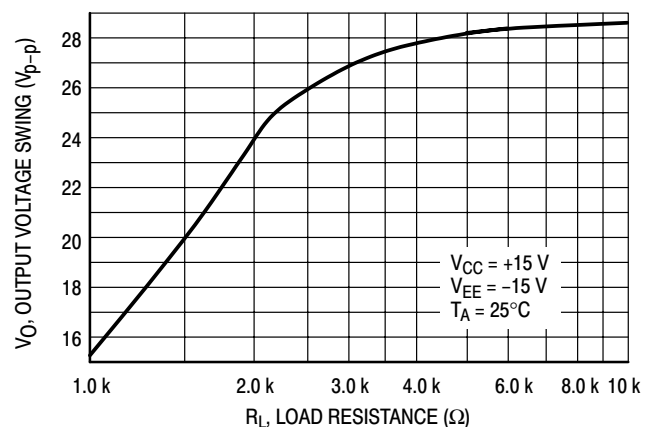


Figure 11. Normalized Gain Bandwidth Product versus Temperature

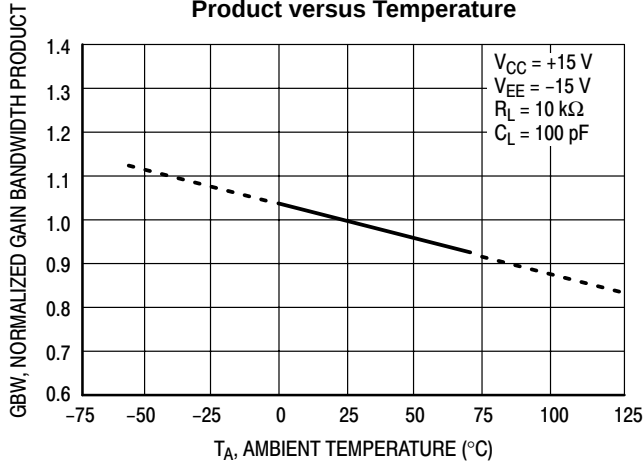


Figure 12. Open Loop Voltage Gain and Phase versus Frequency

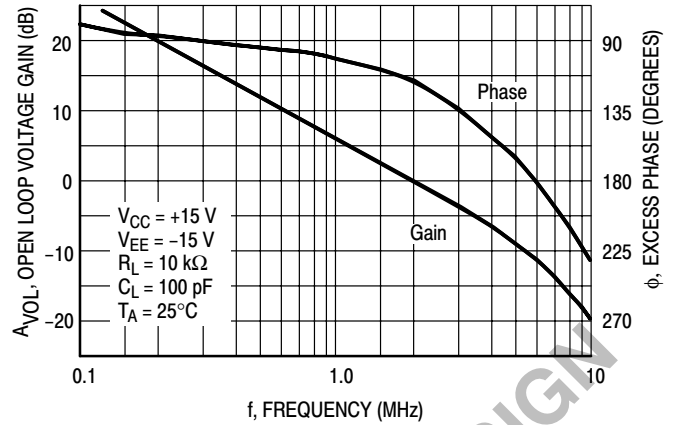


Figure 13. Slew Rate versus Temperature

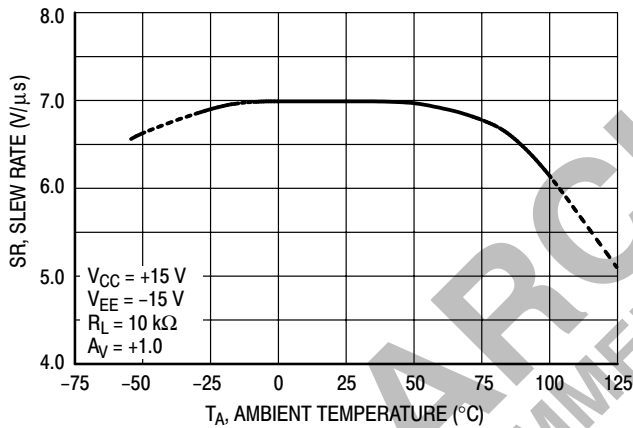


Figure 14. Total Output Distortion versus Frequency

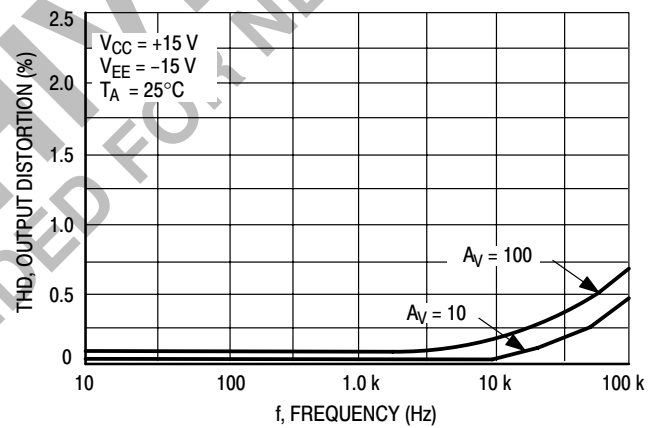


Figure 15. Output Voltage Swing versus Frequency

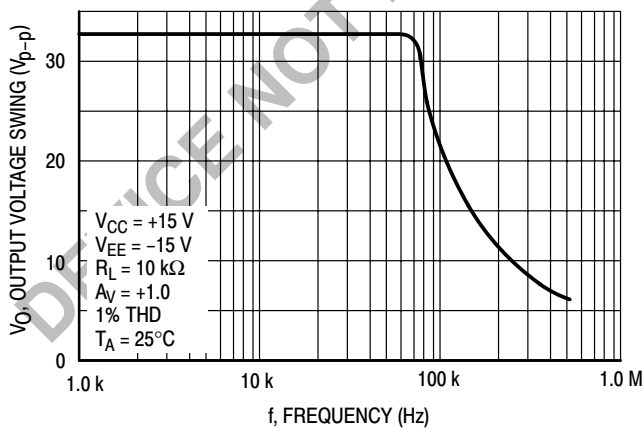


Figure 16. Open Loop Voltage Gain versus Frequency

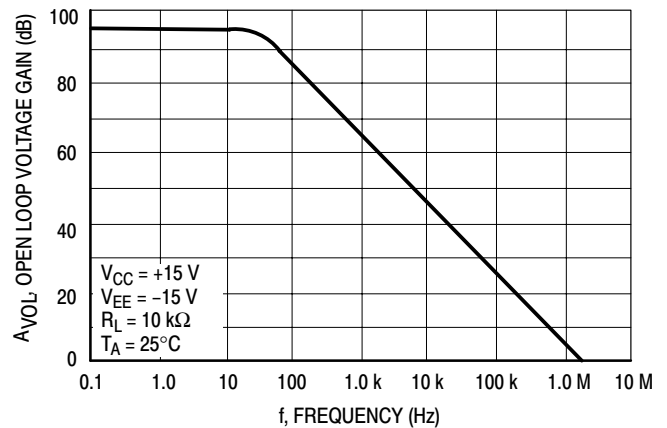


Figure 17. Common Mode Rejection versus Frequency

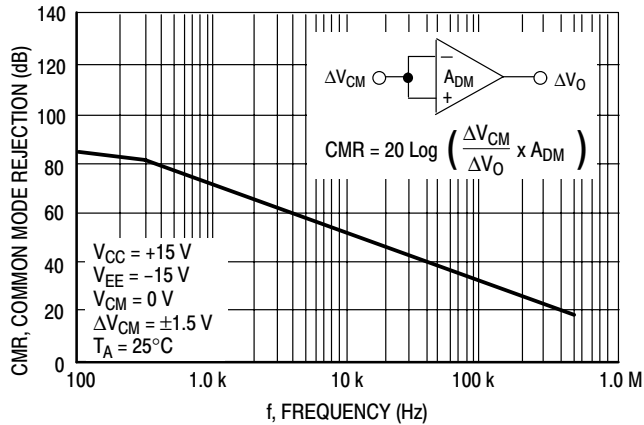


Figure 18. Power Supply Rejection versus Frequency

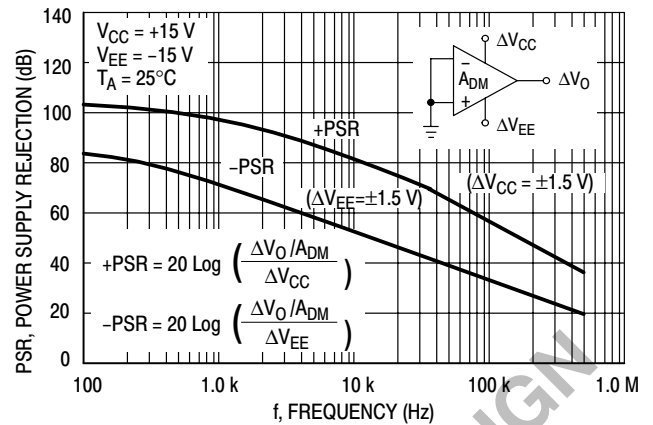


Figure 19. Input Noise Voltage versus Frequency

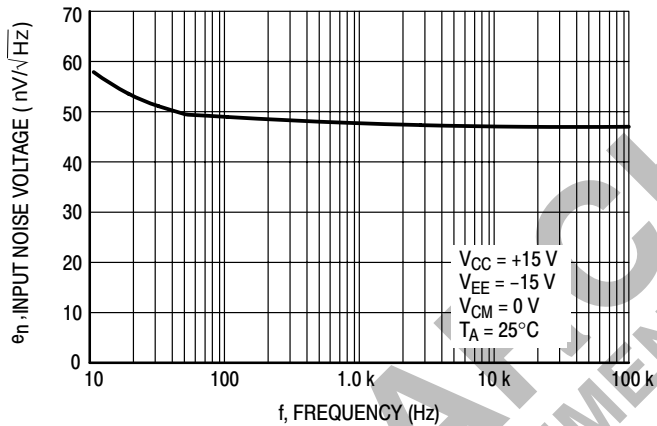


Figure 20. Open Loop Voltage Gain versus Supply Voltage

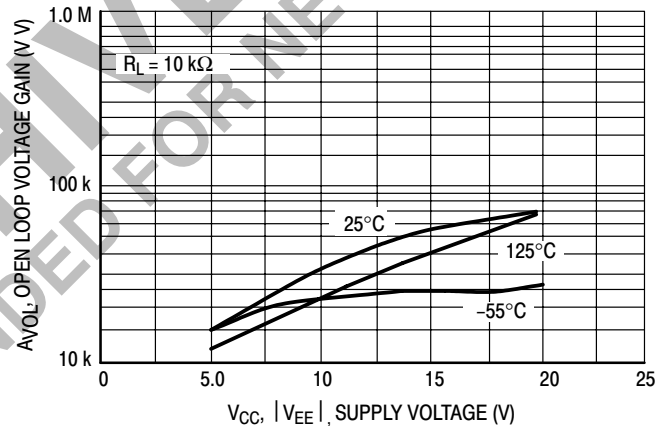


Figure 21. Output Impedance versus Frequency

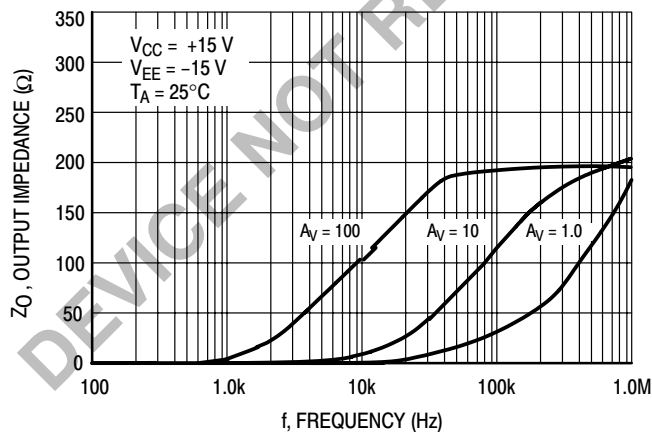
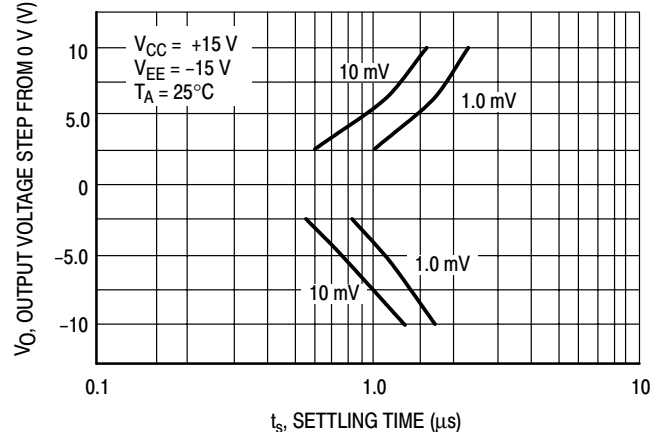


Figure 22. Inverter Settling Time



SMALL SIGNAL RESPONSE

Figure 23. Inverting

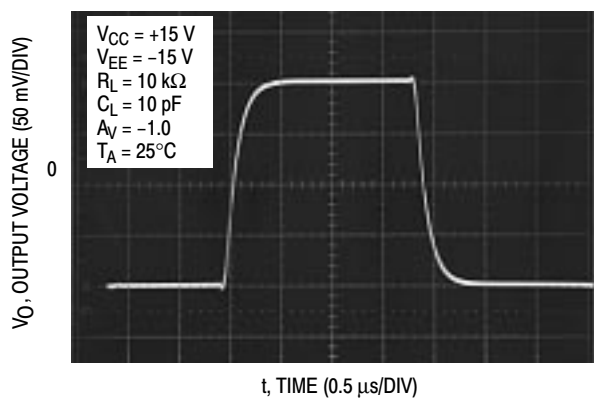
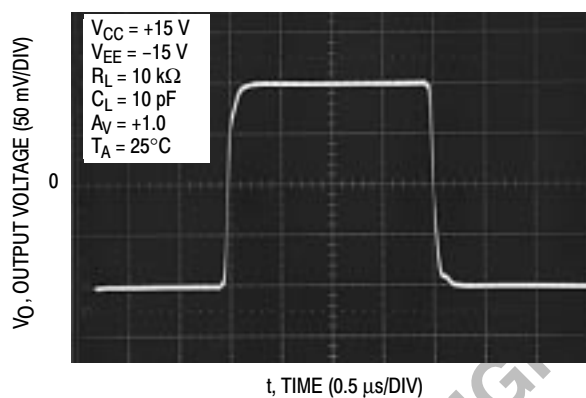


Figure 24. Noninverting



LARGE SIGNAL RESPONSE

Figure 25. Inverting

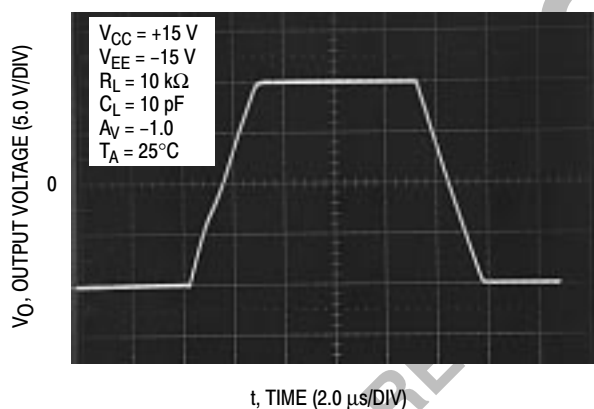
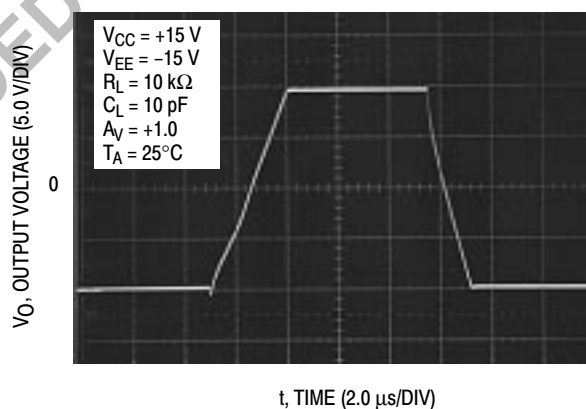


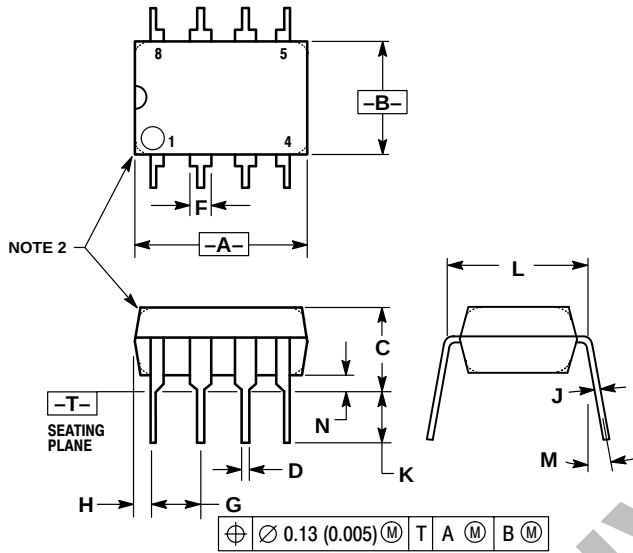
Figure 26. Noninverting



LF441C LF442C LF444C

OUTLINE DIMENSIONS

N SUFFIX PLASTIC PACKAGE CASE 626-05 ISSUE K

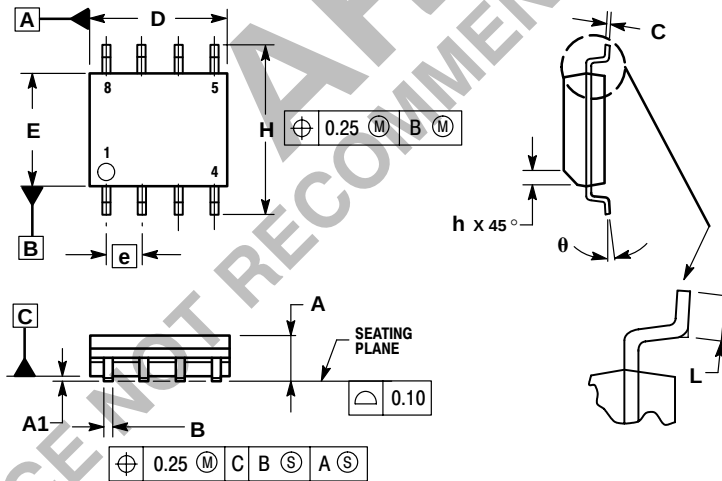


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	10°		10°	
N	0.76	1.01	0.030	0.040

D SUFFIX PLASTIC PACKAGE CASE 751-05 (SO-8) ISSUE R



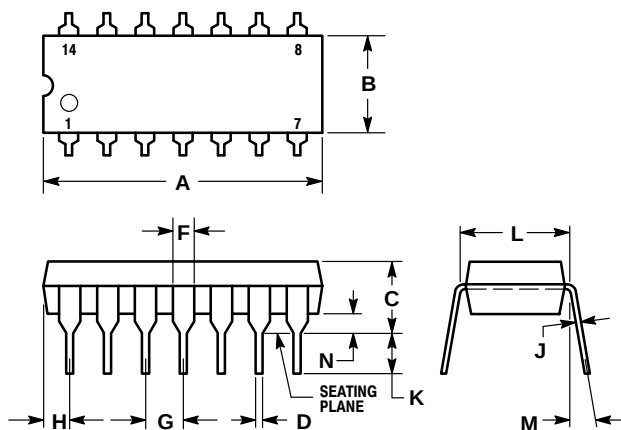
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

OUTLINE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 646-06
ISSUE L

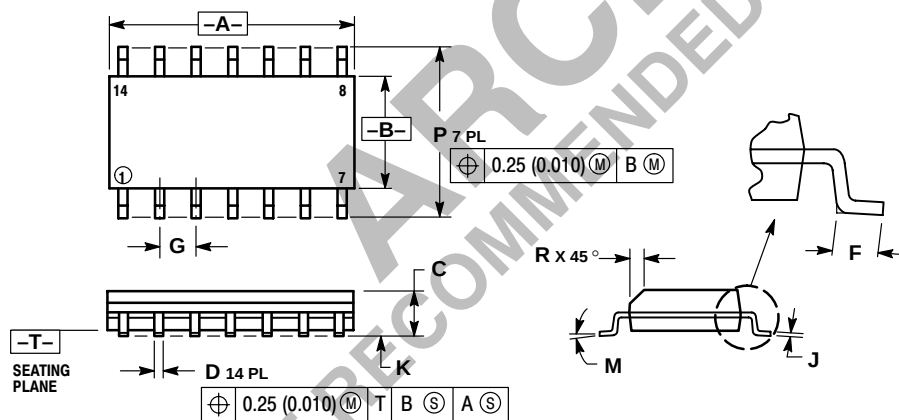


NOTES:

1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC PACKAGE
CASE 751A-03
(SO-14)
ISSUE F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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