Intel® 80960RN I/O Processor

- *Complies with PCI Local Bus Specification, Revision 2.2*
- *Universal (5 V and 3.3 V) PCI Signalling Environment (C-stepping only)*

Data Sheet

Product Features

- High Performance Intel® 80960JT Core
  - Sustained One Instruction/Clock Execution
  - 16 Kbyte, Two-Way Set-Associative Instruction Cache
  - 4 Kbyte, Direct-Mapped Data Cache
  - Sixteen 32-Bit Global Registers
  - Sixteen 32-Bit Local Registers
  - 1 Kbyte, Internal Data RAM
  - Local Register Cache (Eight Available Stack Frames)
  - Two 32-Bit On-Chip Timer Units
- PCI-to-PCI Bridge Unit
  - Eight Delayed Read/Write Buffers Holding up to eight Transactions
  - Primary and Secondary 64-bit PCI Interfaces
  - Two Posting Buffers Holding up to 12 Transactions
  - Delayed and Posted Transaction Support
  - Forwards Memory, I/O, Configuration Commands from PCI Bus to PCI Bus
- I_2O Messaging Unit
  - Four Message Registers
  - Two Doorbell Registers
  - Four Circular Queues
  - 1004 Index Registers
- Memory Controller
  - 128 Mbytes of 64-Bit SDRAM or 64 Mbytes of 32-Bit SDRAM
  - ECC Single-Bit error correction, Double-Bit error detection
  - Two Independent Banks for SRAM / ROM / Flash (8 Mbyte/Bank; 8-Bit)
- Two Address Translation Units
  - Connects Internal Bus to 64-bit PCI Buses
  - Inbound/Outbound Address Translation Support
  - Direct Outbound Addressing Support
- DMA Controller
  - Three Independent Channels
  - PCI Memory Controller Interface
  - 64-Bit Internal + PCI Bus Addressing
  - Independent Interface to 64-bit Primary and Secondary PCI Buses
  - 264 Mbyte/sec Burst Transfers to PCI and SDRAM Memory
  - Direct Addressing to/from PCI Buses
  - Unaligned Transfers Supported in Hardware
  - Two Channels Dedicated to Primary PCI Bus
  - One Channel Dedicated to Secondary PCI Bus
- I^2C Bus Interface Unit
  - Serial Bus
  - Master/Slave Capabilities
  - System Management Functions
- Secondary PCI Arbitration Unit
  - Supports Six Secondary PCI Devices
  - Multi-priority Arbitration Algorithm
- Private PCI Device Support
- Perimeter Land Grid Array Package
  - 540-pin
- Application Accelerator
  - Built-in hardware XOR engine
- Performance Monitoring
  - Ninety-eight events monitored on-chip

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Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at http://www.intel.com.

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1.0 About this Document

This is the data sheet for the Intel® 80960RN processor. This data sheet contains a functional overview, mechanical data (package signal locations and simulated thermal characteristics), targeted electrical specifications (simulated), and bus functional waveforms. Detailed functional descriptions other than parametric performance is published in the *i960® RM/RN I/O Processor Developer's Manual*.

1.1 *Intel® Solutions960®* Program

The *Intel® Solutions960®* program features a wide variety of development tools which support the i960® processor family. Many of these tools are developed by partner companies; some are developed by Intel, such as profile-driven optimizing compilers. For more information on these products, contact your local Intel representative.

1.2 Terminology

In this document, the following terms are used:

- *Primary and Secondary PCI buses* are the 80960RN processor's external PCI buses which conform to PCI SIG specifications.
- Intel® 80960 core refers to the Intel® 80960JT processor which is integrated into the 80960RN processor.

1.3 Additional Information Sources

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

Intel Corporation
Literature Sales
P.O. Box 5937
Denver, CO 80217-9808
1-800-548-4725

Table 1. Related Documentation

Document Title	Order / Contact
i960® RM/RN I/O Processor Developer's Manual	Intel Order # 273158
i960® Jx Microprocessor User's Guide	Intel Order # 272483
i960® RM/RN/RS I/O Processor Specification Update	Intel Order # 273164
PCI Local Bus Specification, Revision 2.2	PCI Special Interest Group 1-800-433-5177
PCI-to-PCI Bridge Architecture Specification, Revision 1.1	PCI Special Interest Group 1-800-433-5177
I^{2}C Peripherals for Microcontrollers	Philips Semiconductor

2.0 Functional Overview

As indicated in Figure 1, the 80960RN processor combines many features with the 80960JT to create an intelligent I/O processor. Subsections following the figure briefly describe the main features; for detailed functional descriptions, refer to the *i960® RM/RN I/O Processor Developer's Manual*.

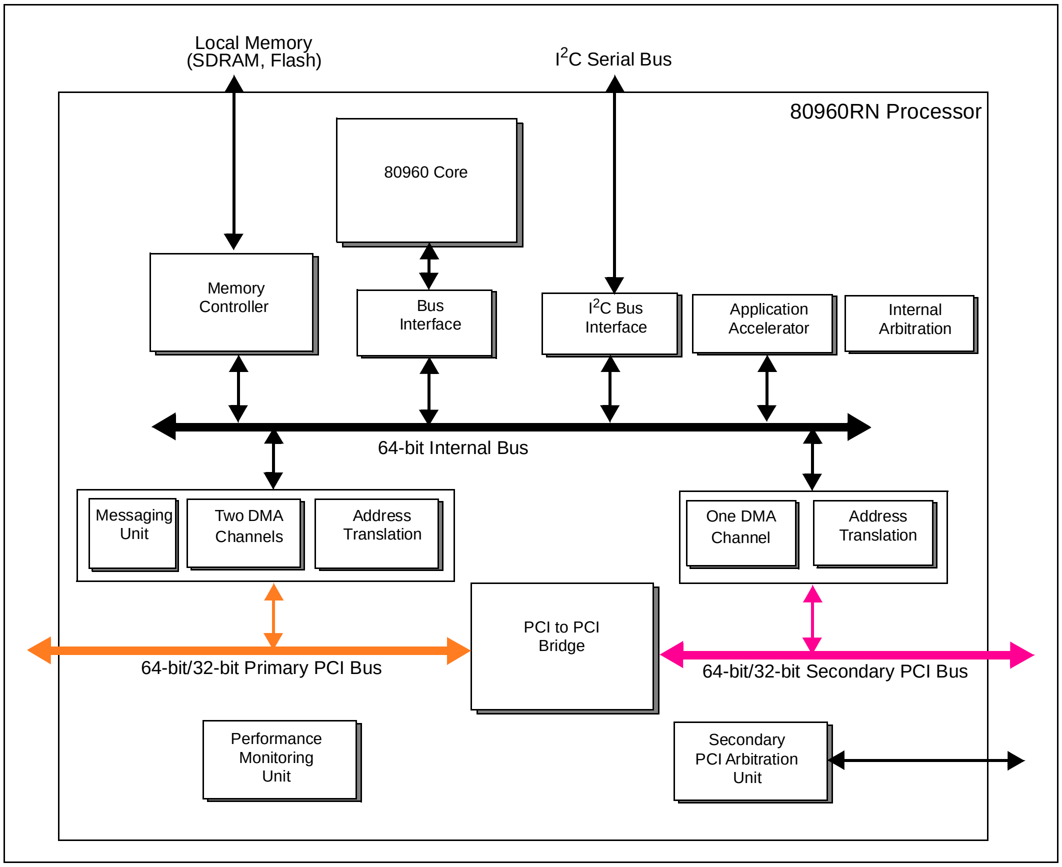
The PCI bus is an industry standard, high performance, low latency system bus that operates up to 264 Mbyte/s. The 80960RN processor, a multi-function PCI device, is fully compliant with the *PCI Local Bus Specification*, Revision 2.2. Function 0 is the PCI-to-PCI bridge unit; Function 1 is the address translation unit.

The PCI-to-PCI bridge unit is the path between two independent 64-bit PCI buses and provides the ability to overcome PCI electrical load limits. The addition of the Intel® i960® core processor brings intelligence to the bridge.

The 80960RN processor, object code compatible with the i960 core processor, is capable of sustained execution at the rate of one instruction per clock.

The internal bus, a 64-bit PCI-like bus, is a high-speed interface to local memory and I/O. Physical and logical memory attributes are programmed via memory-mapped control registers (MMRs); an extension not found on the Intel® i960 Kx, Sx or Cx processors.

Figure 1. Intel® 80960RN Functional Block Diagram



2.1 Key Functional Units

2.1.1 PCI-to-PCI Bridge Unit

The PCI-to-PCI bridge unit (referred to as “bridge”) connects two independent PCI buses. Each PCI bus may be 32 or 64 bits wide. The bridge is fully compliant with the *PCI-to-PCI Bridge Architecture Specification,* Revision 1.1 published by the PCI Special Interest Group. The bridge forwards bus transactions on one PCI bus to the other PCI bus. Dedicated data queues support high performance bandwidth on the PCI buses. The 80960RN supports PCI 64-bit Dual Address Cycle (DAC) addressing.

The bridge has dedicated PCI configuration space accessible through the primary PCI bus.

2.1.2 Private PCI Device Support

The 80960RN processor explicitly supports private PCI devices on the secondary PCI bus. The bridge and Address Translation Unit work together to hide private PCI devices from PCI configuration cycles and allow these hidden devices to use a private PCI address space. The Address Translation Unit issues PCI configuration cycles to configure hidden devices.

2.1.3 DMA Controller

The DMA Controller supports low-latency, high-throughput data transfers between PCI bus agents and local memory. Three separate DMA channels accommodate data transfers: two for primary PCI bus, one for the secondary PCI bus. The DMA Controller supports chaining and unaligned data transfers. The DMA Controller is programmable only through the i960 core processor.

2.1.4 Address Translation Unit

The Address Translation Unit (ATU) allows PCI transactions direct access to local memory. The 80960RN processor has direct access to both PCI buses. The ATU supports transactions between PCI address space and 80960RN processor address space.

Address translation is controlled through programmable registers accessible from both the primary PCI interface and the 80960 core. Dual access to registers allows flexibility in mapping the two address spaces.

2.1.5 Messaging Unit

The Messaging Unit (MU) provides data transfer between the PCI system and the 80960RN processor. The Messaging Unit uses interrupts to notify the PCI system or the 80960RN processor when new data arrives. The MU has four messaging mechanisms: Message Registers, Doorbell Registers, Circular Queues, and Index Registers. Each mechanism allows a host processor or external PCI device and the 80960RN processor to communicate through message passing and interrupt generation.

2.1.6 Memory Controller Unit

The Memory Controller Unit (MCU) allows direct control of a local SDRAM and Flash subsystem. The MCU features programmable chip selects, a wait state generator and Error Correction and Detection. With the ATU configuration registers, local memory can be configured as PCI addressable memory or private processor memory.

2.1.7 I^{2}C Bus Interface Unit

The I^{2}C (Inter-Integrated Circuit) Bus Interface Unit allows the 80960 core to serve as a master and slave device residing on the I^{2}C bus. The I^{2}C bus is a serial bus developed by Philips Semiconductor comprising a two pin interface. The bus allows the 80960RN processor to interface to other I^{2}C peripherals and microcontrollers for system management functions. It requires a minimum of hardware for an economical system to relay status and reliability information on the I/O subsystem to an external device. For more information, see *I^{2}C Peripherals for Microcontrollers* (Philips Semiconductor).

2.1.8 Secondary PCI Arbitration Unit

The Secondary PCI Arbitration Unit provides PCI arbitration for the secondary PCI bus. The arbitration includes a fairness algorithm with programmable priorities and six external PCI Request and Grant signal pairs.

2.1.9 Application Accelerator Unit

The Application Accelerator Unit (AAU) provides hardware acceleration of XOR functions commonly used in RAID algorithms. Additionally, the AAU provides block moves within local memory. The Application Accelerator interfaces the internal bus and operates on data within local memory. The AAU is programmable through the i960 core processor and supports chaining and unaligned data transfers.

2.1.10 Performance Monitor Unit

The Performance Monitor Unit (PMU) allows software to monitor the performance of the different buses: Primary PCI, Secondary PCI, and Internal. Multiple performance characteristics are captured with 14 mode registers and a global time stamp register.

2.1.11 Bus Interface Unit

The Bus Interface Unit (BIU) provides an interface between the 100 MHz 80960JT core and the 66 MHz internal bus. To optimize performance, the BIU implements prefetching and write merging.

2.2 Intel® i960® Core Features (Intel® 80960JT)

The processing power of the 80960RN processor comes from the 100 MHz 80960JT processor core. The 80960JT is a scalar implementation of the 80960 Core Architecture. Figure 2 shows a block diagram of the 80960JT Core processor.

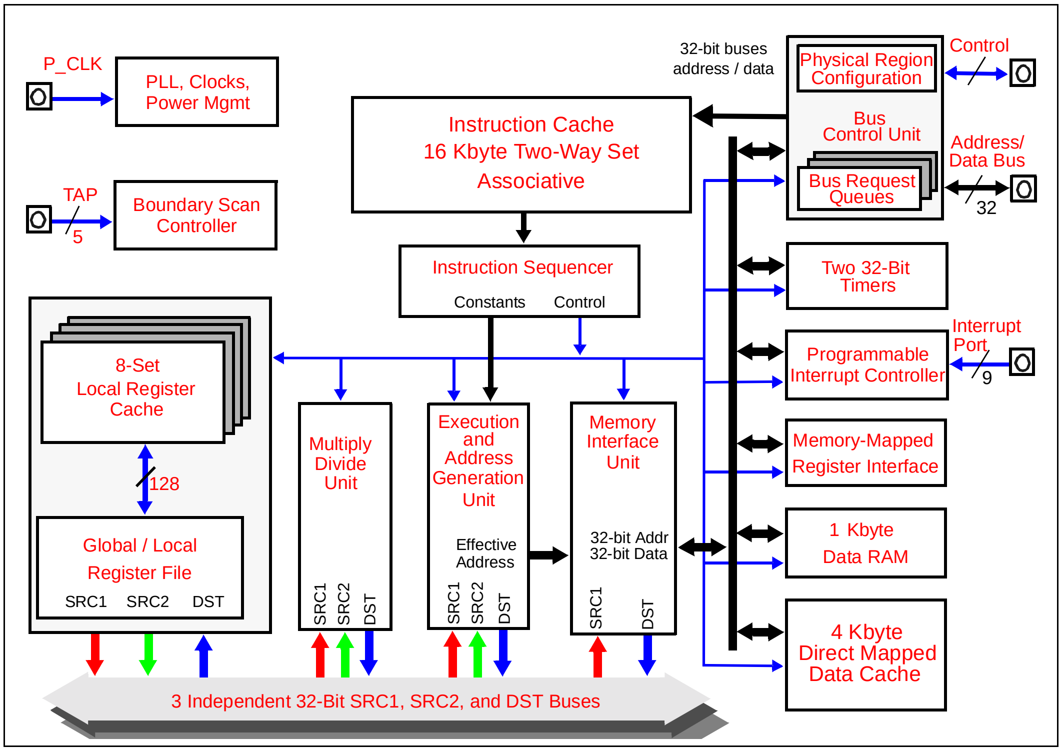
Factors that contribute to the 80960JT core's performance include:

- 100 MHz Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- Efficient instruction pipeline minimizes pipeline break latency
- Register and resource scoreboarding allow overlapped instruction execution
- 128-bit register bus speeds local register caching
- 16 Kbyte two-way set-associative, integrated instruction cache
- 4 Kbyte direct-mapped, integrated data cache
- 1 Kbyte integrated data RAM delivers zero wait state program data

The 80960 core operates out of its own 32-bit address space, which is independent of the PCI address space. Local memory can be:

- Made visible to the PCI address space
- Kept private to the 80960JT core
- Allocated as a combination of the two

Figure 2. Intel® 80960JT Core Block Diagram



2.2.1 Burst Bus

A 32-bit high-performance bus controller interfaces the 80960RN processor to the Bus Interface Unit. The Bus Control Unit fetches instructions and transfers data on the internal bus at the rate of up to four 32-bit words per six clock cycles. The external address/data bus is multiplexed.

Data caching is programmed through a group of logical memory templates and a defaults register. The Bus Control Unit's features include:

- Multiplexed external bus minimizes pin count
- External ready control for address-to-data, data-to-data and data-to-next-address wait state types
- Little endian byte ordering
- Unaligned bus accesses performed transparently
- Three-deep load/store queue decouples the bus from the 80960 core

Upon reset, the 80960JT conducts an internal self test. Before executing its first instruction, it performs an external bus confidence test by performing a checksum on the first words of the Initialization Boot Record.

2.2.2 Timer Unit

The timer unit (TU) contains two independent 32-bit timers that are capable of counting at several clock rates and generating interrupts. Each is programmed through the Timer Unit registers. These memory-mapped registers are addressable on 32-bit boundaries. Timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the 80960JT's interrupt controller. The TU can generate a fault when unauthorized writes from user mode are detected.

2.2.3 Priority Interrupt Controller

Low interrupt latency is critical to many embedded applications. As part of its highly flexible interrupt mechanism, the 80960JT exploits several techniques to minimize latency:

- Interrupt vectors and interrupt handler routines can be reserved on-chip
- Register frames for high-priority interrupt handlers can be cached on-chip
- The interrupt stack can be placed in cacheable memory space

2.2.4 Faults and Debugging

The 80960JT employs a comprehensive fault model. The processor responds to faults by making implicit calls to a fault handling routine. Specific information collected for each fault allows the fault handler to diagnose exceptions and recover appropriately.

The processor also has built-in debug capabilities. With software, the 80960JT may be configured to detect as many as seven different trace event types. Alternatively, **mark** and **fmark** instructions can generate trace events explicitly in the instruction stream. Hardware breakpoint registers are also available to trap on execution and data addresses.

2.2.5 On-Chip Cache and Data RAM

Memory subsystems often impose substantial wait state penalties. The 80960JT integrates considerable storage resources on-chip to decouple CPU execution from the external bus. The 80960JT includes a 16 Kbyte instruction cache, a 4 Kbyte data cache and 1 Kbyte data RAM.

2.2.6 Local Register Cache

The 80960JT rapidly allocates and deallocates local register sets during context switches. The processor needs to flush a register set to the stack only when it saves more than seven sets to its local register cache.

2.2.7 Test Features

The 80960RN processor incorporates numerous features that enhance the user's ability to test both the processor and the system to which it is attached. These features include ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG).

The 80960JT provides testability features compatible with IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std. 1149.1).

One of the boundary scan instructions, HIGHZ, forces the processor to float all its output pins (ONCE mode). ONCE mode can also be initiated at reset without using the boundary scan mechanism.

ONCE mode is useful for board-level testing. This feature allows a mounted 80960RN processor to electrically "remove" itself from a circuit board allowing system-level testing where a remote tester can exercise the processor system.

The test logic does not interfere with component or system behavior and ensures that components function correctly and the connections between various components are correct.

The JTAG Boundary Scan feature is an alternative to conventional "bed-of-nails" testing. Boundary Scan can examine connections that might otherwise be inaccessible to a test system.

2.2.8 Memory-Mapped Control Registers

The 80960JT is compliant with 80960 family architecture. Each memory-mapped, 32-bit register is accessed via memory-format instructions. The processor ensures that these accesses do not generate external bus cycles.

2.2.9 Instructions, Data Types and Memory Addressing Modes

As with all 80960 family processors, the instruction set supports several different data types and formats:

- Bit
- Bit fields
- Integer (8-, 16-, 32-, 64-bit)
- Ordinal (8-, 16-, 32-, 64-bit unsigned integers)
- Triple word (96 bits)
- Quad word (128 bits)

The 80960JT provides a full set of addressing modes for C and assembly:

- Two Absolute modes
- Five Register Indirect modes
- Index with displacement mode
- IP with displacement mode

Table 2 shows the available 80960JT instructions.

Table 2. Instruction Set

Data Movement	Arithmetic	Logical	Bit, Bit Field and Byte
Load Store Move Conditional Select Load Address	Add Subtract Multiply Divide Remainder Modulo Shift Extended Shift Extended Multiply Extended Divide Add with Carry Subtract with Carry Conditional Add Conditional Subtract Rotate	And Not And And Not Or Exclusive Or Not Or Or Not Nor Exclusive Nor Not Nand	Set Bit Clear Bit Not Bit Alter Bit Scan For Bit Span Over Bit Extract Modify Scan Byte for Equal Byte Swap
Comparison	**Branch**	**Call/Return**	**Fault**
Compare Conditional Compare Compare and Increment Compare and Decrement Test Condition Code Check Bit	Unconditional Branch Conditional Branch Compare and Branch	Call Call Extended Call System Return Branch and Link	Conditional Fault Synchronize Faults
Debug	**Processor Management**	**Atomic**	
Modify Trace Controls Mark Force Mark	Flush Local Registers Modify Arithmetic Controls Modify Process Controls Halt System Control Cache Control Interrupt Control	Atomic Add Atomic Modify	

3.0 Package Information

3.1 Package Introduction

The 80960RN processor is offered in a Perimeter Land Grid Array (PBGA) package. This is a perimeter array package with five rows of ball connections in the outer area of the package. See Figure 4 “540L H-PBGA Package Diagram (Bottom View)” on page 27.

3.1.1 Functional Signal Definitions

This section defines the pins and signals in the following tables:

- Table 3 “Pin Description Nomenclature” on page 16
- Table 4 “Memory Controller Signals” on page 17
- Table 5 “Primary PCI Bus Signals” on page 20
- Table 6 “Secondary PCI Arbiter Signals” on page 21
- Table 8 “Intel® 80960Jx Core Signals and Configuration Straps” on page 24
- Table 9 “I^{2}C, JTAG, Core Signals” on page 25

3.1.1.1 Signal Pin Descriptions

Table 3. Pin Description Nomenclature

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or output
OD	Open Drain pin
-	Pin must be connected as described
N/C	NO CONNECT. Do not make electrical connections to these balls.
5V	Input pin is 5 volt tolerant
Sync(...)	Synchronous. Inputs meet setup and hold times relative to an input clock. Sync(P) Synchronous to **P_CLK** Sync(D) Synchronous to **DCLKIN** Sync(T) Synchronous to **TCK**
Async	Asynchronous. Inputs may be asynchronous relative to **P_CLK**, **DCLKIN**, or **TCK**. All asynchronous signals are level-sensitive.
Prst(...)	While the **P_RST#** pin is asserted, the pin: Prst(1) Is driven to Vcc Prst(0) Is driven to Vss Prst(X) Is driven to unknown state Prst(H) Is pulled up to Vcc Prst(L) Is pulled down to Vss Prst(Z) Floats Prst(Q) Is a valid output Since **P_RST#** is asynchronous, these are asynchronous events.
Srst(...)	While the **S_RST#** pin is asserted, the pin: Srst(1) Is driven to Vcc Srst(0) Is driven to Vss Srst(X) Is driven to unknown state Srst(H) Is pulled up to Vcc Srst(L) Is pulled down to Vss Srst(Z) Floats Srst(Q) Is a valid output Note that **S_RST#** is asserted when **P_RST#** is asserted or BCR[6] is set with software.
Irst(...)	While the **I_RST#** pin is asserted, the pin: Irst(1) Is driven to Vcc Irst(0) Is driven to Vss Irst(X) Is driven to unknown state Irst(H) Is pulled up to Vcc Irst(L) Is pulled down to Vss Irst(Z) Floats Irst(Q) Is a valid output Note that **I_RST#** is asserted when **P_RST#** is asserted or EBCR[5] is set with software.
P32(...)	While the Primary PCI Bus is configured as a 32-bit PCI bus by the Primary central resource: P32(H) is pulled up internally to Vcc P32(L) is pulled down internally to Vss
S32(...)	While the Secondary PCI Bus is configured as a 32-bit PCI bus with **32BITPCI_EN#**: S32(H) is pulled up internally to Vcc S32(L) is pulled down internally to Vss

Table 4. Memory Controller Signals (Sheet 1 of 3)

Name	Count	Type	Description
DCLKOUT	1	O Irst(Q)	**SDRAM OUTPUT CLOCK** dedicated for SDRAM memory subsystem.
DCLKIN	1	I	**SDRAM INPUT CLOCK** dedicated for SDRAM memory subsystem. Used to skew DCLKOUT appropriately to accommodate flight time and clock buffer delays.
SA[11:0]	12	O Irst(Q)	**SDRAM MULTIPLEXED ADDRESS BUS** carries the multiplexed row and column addresses to the SDRAM memory banks. For **SA[10]**, see note 1.
SBA[1:0]	2	O Irst(Q)	**SDRAM INTERNAL BANK SELECT** indicates which of the SDRAM internal banks are read or written during the current transaction.
SRAS#	1	O Irst(1)	**SDRAM ROW ADDRESS STROBE** indicates the presence of a valid row address on the Multiplexed Address Bus **SA[11:0]**. See note 1.
SCAS#	1	O Irst(1)	**SDRAM COLUMN ADDRESS STROBE** indicates the presence of a valid column address on the Multiplexed Address Bus **SA[11:0]**. See note 1.
SDQM[7:0]	8	O Irst(1)	**SDRAM DATA MASK** controls which of the eight bytes on the data bus should be written or read. When **SDQM[7:0]** asserted, the SDRAM devices do not accept/drive valid data from/to the byte lanes. When **SDQM[7:0]** deasserted, the SDRAM devices accept/drive valid data from/to the byte lanes. By convention, SDQM[1] masks two x8 SDRAM devices. Functionally, all **SDQM[7:0]** signals are equivalent.
SWE#	1	O Irst(1)	**SDRAM WRITE ENABLE** indicates that the current memory transaction is a write operation. See note 1.
SCE[1:0]#	2	O Irst(1)	**SDRAM CHIP ENABLE** enables the SDRAM devices for a memory access (1 per bank supported). See note 1.
SCKE[1:0]	2	O Irst(Q)	**SCKE[1:0]** are the clock enables for the SDRAM memory. Deasserting will place the SDRAM in self-refresh mode. See note 1.
DQ[63:0]	64	I/O Irst(1) Sync(D)	**DATA BUS** carries 64-bit data to and from memory. During a data (T_d) cycle, read or write data is present on one or more contiguous bytes, comprising DQ[63:56], DQ[55:48], DQ[47:40], DQ[39:32], DQ[31:24], DQ[23:16], DQ[15:8] and DQ[7:0]. During write operations, unused pins are driven to determinate values.
SCB[7:0]	8	I/O Irst(1) Sync(D)	**ERROR CORRECTION CODE** carries the 8-bit ECC code to and from memory during data cycles.
ROE#	1	O Irst(1)	**ROM OUTPUT ENABLE** specifies, during a T_a cycle, whether the operation is a write (1) or read (0) to the ROM interface. It remains valid during T_d cycles. When **ROE#** is asserted, the data is transferred from the memory on **RAD[16:9]**.
RWE#	1	O Irst(1)	**ROM WRITE ENABLE** indicates the direction data is to be transferred to/from ROM and controls the WE input on the ROM device. When **RWE#** is asserted, the data is transferred to the memory on DQ[7:0].
RCE[1:0]#	2	O Irst(1)	**FLASH CHIP ENABLE** enables Flash devices for a memory access.
RALE	1	O Irst(0)	**ROM ADDRESS LATCH ENABLE** indicates the cycle in which the address on RAD[16:3] should be externally latched for the Flash subsystem.

Table 4. Memory Controller Signals (Sheet 2 of 3)

Name	Count	Type	Description
RAD[16:9]	8	I/O 5V Irst(X) Sync(D)	**FLASH ADDRESS/DATA BUS**: During an address (T_a) cycle, bits 16:9 contain a physical word address. During a data cycle (Td), bits 16:9 carry data bits 16:9 of the Flash data byte.
RAD[8]	1	O Prst(H)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 8 contain a physical word address. **RAD[8]**. multiplexes physical address bits [22] with [8]. Refer to the MCU chapter of the *i960® RM/RN I/O Processor Developer's Manual* for details.
RAD[7]	1	O Prst(H)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 7 contain a physical word address. **RAD[7]**. multiplexes physical address bits [21] with [7]. Refer to the MCU chapter of the *i960® RM/RN I/O Processor Developer's Manual* for details.
RAD[6]/ **RST_MODE#** (Config. Pin)	1	I/O 5V Prst(H)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 6 contain a physical word address. **RAD[6]**. multiplexes physical address bits [20] with [6]. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *i960® RM/RN I/O Processor Developer's Manual* for details. **RESET MODE** is sampled at Primary PCI bus reset to determine if the 80960RN processor is to be held in reset. If asserted, the 80960RN processor will be held in reset until the 80960 Processor Reset bit is cleared in the Extended Bridge Control Register.
RAD[5]	1	O Prst(H)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 5 contain a physical word address. **RAD[5]**. multiplexes physical address bits [19] with [5]. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *i960® RM/RN I/O Processor Developer's Manual* for details.
RAD[4]/ **STEST** (Config. Pin)	1	I/O 5V Prst(H)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 4 contain a physical word address. **RAD[4]**. multiplexes physical address bits [18] with [4]. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *i960® RM/RN I/O Processor Developer's Manual* for details. **SELF TEST** enables or disables the processor's internal self-test feature at initialization. **STEST** is examined at the end of **P_RST#**. When **STEST** is asserted, the processor performs its internal self-test and the external bus confidence test. When **STEST** is deasserted, the processor performs only the external bus confidence test. 0 = Self Test Disabled 1 = Self Test Enabled
RAD[3]/ **RETRY** (Config. Pin)	1	I/O 5V Prst(H)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 3 contain a physical word address. **RAD[3]**. multiplexes physical address bits [17] with [3]. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *i960® RM/RN I/O Processor Developer's Manual* for details. **RETRY** is sampled at Primary PCI bus reset to determine if the Primary PCI interface will be disabled. If high, the Primary PCI interface will disable PCI configuration cycles by signaling a Retry until the Configuration Cycle Retry bit is cleared in the Extended Bridge Control Register. If low, the Primary PCI interface allow configuration cycles to occur.

Table 4. Memory Controller Signals (Sheet 3 of 3)

Name	Count	Type	Description
RAD[2]/ **32BITMEM_EN#** (Config. Pin)	1	I/O 5V Prst(H)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 2 contains a physical word address. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *i960® RM/RN I/O Processor Developer's Manual* for details. **32-BIT Memory Enable** The **32BITMEM_EN#** signal is sampled at Primary PCI Reset to notify the memory controller if 32-bit wide SDRAM memories are connected to the memory controller. If **32BITMEM_EN#** is high, the memory controller supports the 64-bit SDRAM protocol for accesses to SDRAM memories. If **32BITMEM_EN#** is low, the memory controller supports the 32-bit SDRAM protocol for accesses to SDRAM memories.
RAD[1]/ **32BITPCI_EN#** (Config. Pin)	1	I/O 5V Prst(H)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 1 contains a physical word address. Within four clocks after the deassertion of **P_RST#**, this pin is an output only. Refer to the MCU chapter of the *i960® RM/RN I/O Processor Developer's Manual* for details. **32-BIT Secondary PCI Enable** The **32BITPCI_EN#** signal is sampled at Primary PCI Reset to notify the secondary PCI arbiter NOT to generate the 64-bit protocol of the rising edge of the secondary reset for the secondary PCI bus. If **32BITPCI_EN#** is high, the secondary PCI arbiter asserts **S_REQ64#** during **S_RST#**, indicating the secondary PCI bus is a 64-bit bus. If **32BITPCI_EN#** is low, the secondary PCI arbiter does not assert **S_REQ64#** during **S_RST#**, indicating the secondary PCI bus is NOT a 64-bit bus.
RAD[0]	1	O Prst(H)	**FLASH ADDRESS BUS**: During an address (T_a) cycle, bit 0 contains a physical word address. Refer to the MCU chapter of the *i960® RM/RN I/O Processor Developer's Manual* for details.

NOTE:

1. These pins remain functional for 20 **DCLKIN** periods after **I_RST#** is asserted for a warm boot. The designated Irst() state applies after 20 **DCLKIN** periods after **I_RST#** is asserted. For more details, refer to the MCU Chapter of the *i960® RM/RN I/O Processor Developer's Manual*.

Table 5. Primary PCI Bus Signals (Sheet 1 of 2)

Name	Count	Type	Description
P_AD[31:0]	32	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI ADDRESS/DATA** is the multiplexed PCI address and bottom 32 bits of the data bus.
P_AD[63:32]	32	I/O 5V Sync(P) Prst(Z) P32(H)	**PRIMARY PCI DATA** is the upper 32 bits of the primary PCI data bus driven during the data phase.
P_PAR	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS PARITY** is even parity across **P_AD[31:0]** and **P_C/BE[3:0]#**.
P_PAR64	1	I/O 5V Sync(P) Prst(Z) P32(H)	**PRIMARY PCI BUS UPPER DWORD PARITY** is even parity across **P_AD[63:32]** and **P_C/BE[7:4]#**.
P_C/BE[3:0]#	4	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS COMMAND and BYTE ENABLES** are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables for **P_AD[31:0]**.
P_C/BE[7:4]#	4	I/O 5V Sync(P) Prst(Z) P32(H)	**PRIMARY PCI BUS BYTE ENABLES** are as byte enables for **P_AD[63:32]** during the data phase.
P_REQ#	1	O Prst(Z)	**PRIMARY PCI BUS REQUEST** indicates to the primary PCI bus arbiter that the 80960RN processor desires use of the PCI bus.
P_REQ64#	1	I/O 5V Sync(P) Prst(Z) P32(Z)	**PRIMARY PCI BUS REQUEST 64-BIT TRANSFER** indicates the attempt of a 64-bit transaction on the primary PCI bus. If the target is 64-bit capable, the target acknowledges the attempt with the assertion of **P_ACK64#**.
P_GNT#	1	I 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS GRANT** indicates that access to the primary PCI bus has been granted.
P_ACK64#	1	I/O 5V Sync(P) Prst(Z) P32(Z)	**PRIMARY PCI BUS ACKNOWLEDGE 64-BIT TRANSFER** indicates that the device has positively decoded its address as the target of the current access and the target is willing to transfer data using the full 64-bit data bus.
P_FRAME#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS CYCLE FRAME** is asserted to indicate the beginning and duration of an access.
P_IRDY#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS INITIATOR READY** indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the Address/Data bus. During a read, it indicates the processor is ready to accept the data.
P_TRDY#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS TARGET READY** indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the Address/Data bus. During a write, it indicates the target is ready to accept the data.

Table 5. Primary PCI Bus Signals (Sheet 2 of 2)

Name	Count	Type	Description
P_STOP#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS STOP** indicates a request to stop the current transaction on the primary PCI bus.
P_DEVSEL#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS DEVICE SELECT** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
P_SERR#	1	I/O 5V OD Sync(P) Prst(Z)	**PRIMARY PCI BUS SYSTEM ERROR** is driven for address parity errors on the primary PCI bus.
P_CLK	1	I 5V	**PRIMARY PCI BUS INPUT CLOCK** provides the timing for all primary PCI transactions and is the clock source for all internal 80960RN units.
P_RST#	1	I 5V Async	**PRIMARY RESET** brings PCI-specific registers, sequencers, and signals to a consistent state. When **P_RST#** is asserted: PCI output signals are driven to a known consistent state. PCI bus interface output signals are three-stated. open drain signals such as **P_SERR#** are floated. **P_RST#** may be asynchronous to **P_CLK** when asserted or deasserted. Although asynchronous, deassertion must be guaranteed to be a clean, bounce-free edge.
P_PERR#	1	I/O 5V Sync(P) Prst(Z)	**PRIMARY PCI BUS PARITY ERROR** is asserted when a data parity error occurs during a primary PCI bus transaction.
P_LOCK#	1	I 5V Sync(P)	**PRIMARY PCI BUS LOCK** indicates the need to perform an atomic operation on the primary PCI bus.
P_IDSEL	1	I 5V Sync(P)	**PRIMARY PCI BUS INITIALIZATION DEVICE SELECT** is used to select the 80960RN during a Configuration Read or Write command on the primary PCI bus.
P_INT[A:D]#	4	O OD Prst(Z)	**PRIMARY PCI BUS INTERRUPT** requests an interrupt. The assertion and deassertion of **P_INT[A:D]#** is asynchronous to **P_CLK**. A device asserts its **P_INT[A:D]#** line when requesting attention from its device driver. Once the **P_INT[A:D]#** signal is asserted, it remains asserted until the device driver clears the pending request. **P_INT[A:D]#** Interrupts are level sensitive.

Table 6. Secondary PCI Arbiter Signals

Name	Count	Type	Description
S_REQ[5:0]#	6	I 5V Sync(P)	**SECONDARY PCI BUS REQUESTS** are the request signals from devices 0 through 5 on the secondary PCI bus.
S_GNT[5:0]#	6	O Srst(Z)	**SECONDARY PCI BUS GRANT** are grant signals sent to devices 5-0 on the secondary PCI bus

Table 7. Secondary PCI Bus Signals (Sheet 1 of 2)

Name	Count	Type	Description
S_AD[31:0]	32	I/O 5V Sync(P) Srst(0)	**SECONDARY PCI ADDRESS/DATA** is the multiplexed secondary PCI address and lower 32 bits of the data bus.
S_AD[63:32]	32	I/O 5V Sync(P) Srst(Z) S32(H)	**SECONDARY PCI DATA** is the upper 32 bits of the secondary PCI data bus.
S_PAR	1	I/O Sync(P) Srst(0)	**SECONDARY PCI BUS PARITY** is even parity across **S_AD[31:0]** and **S_C/BE[3:0]#**.
S_PAR64	1	I/O 5V Sync(P) Srst(Z) S32(H)	**SECONDARY PCI BUS UPPER DWORD PARITY** is even parity across **S_AD[63:32]** and **S_C/BE[7:4]#**.
S_C/BE[3:0]#	4	I/O 5V Sync(P) Srst(0)	**SECONDARY PCI BUS COMMAND and BYTE ENABLES** are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as the byte enables for **S_AD[31:0]**.
S_C/BE[7:4]#	4	I/O 5V Sync(P) Srst(Z) S32(H)	**SECONDARY PCI BYTE ENABLES** are used as byte enables for **S_AD[63:32]** during secondary PCI data phases.
S_REQ64#	1	I/O 5V Sync(P) Srst(Q) S32(Z)	**SECONDARY PCI BUS REQUEST 64-BIT TRANSFER** indicates the attempt of a 64-bit transaction on the secondary PCI bus. If the target is 64-bit capable, the target acknowledges the attempt with the assertion of **S_ACK64#**.
S_ACK64#	1	I/O 5V Sync(P) Srst(Z) S32(Z)	**SECONDARY PCI BUS ACKNOWLEDGE 64-BIT TRANSFER** indicates that the device has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64 bits.
S_FRAME#	1	I/O 5V Sync(P) Srst(Z)	**SECONDARY PCI BUS CYCLE FRAME** is asserted to indicate the beginning and duration of an access.
S_IRDY#	1	I/O 5V Sync(P) Srst(Z)	**SECONDARY PCI BUS INITIATOR READY** indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the secondary Address/Data bus. During a read, it indicates the processor is ready to accept the data.
S_TRDY#	1	I/O 5V Sync(P) Srst(Z)	**SECONDARY PCI BUS TARGET READY** indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the secondary Address/Data bus. During a write, it indicates the target is ready to accept the data.
S_STOP#	1	I/O 5V Sync(P) Srst(Z)	**SECONDARY PCI BUS STOP** indicates a request to stop the current transaction on the secondary PCI bus.

Table 7. Secondary PCI Bus Signals (Sheet 2 of 2)

Name	Count	Type	Description
S_DEVSEL#	1	I/O 5V Sync(P) Srst(Z)	**SECONDARY PCI BUS DEVICE SELECT** is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
S_SERR#	1	I/O 5V OD Sync(P) Srst(Z)	**SECONDARY PCI BUS SYSTEM ERROR** is driven for address parity errors on the secondary PCI bus.
S_RST#	1	**O** Async	**SECONDARY PCI BUS RESET** is an output based on **P_RST#**. It brings PCI-specific registers, sequencers, and signals to a consistent state. When **P_RST#** is asserted or BCR[6] is set, it causes **S_RST#** to assert and: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • open drain signals such as **S_SERR#** are floated **S_RST#** may be asynchronous to **S_CLKIN** when asserted or deasserted. Although asynchronous, deassertion must be guaranteed to be a clean, bounce-free edge.
S_PERR#	1	**I/O** 5V Sync(P) Srst(Z)	**SECONDARY PCI BUS PARITY ERROR** is asserted when a data parity error during a secondary PCI bus transaction.
S_LOCK#	1	**I/O** 5V Sync(P) Srst(Z)	**SECONDARY PCI BUS LOCK** indicates the need to perform an atomic operation on the secondary PCI bus.

Table 8. Intel® 80960Jx Core Signals and Configuration Straps

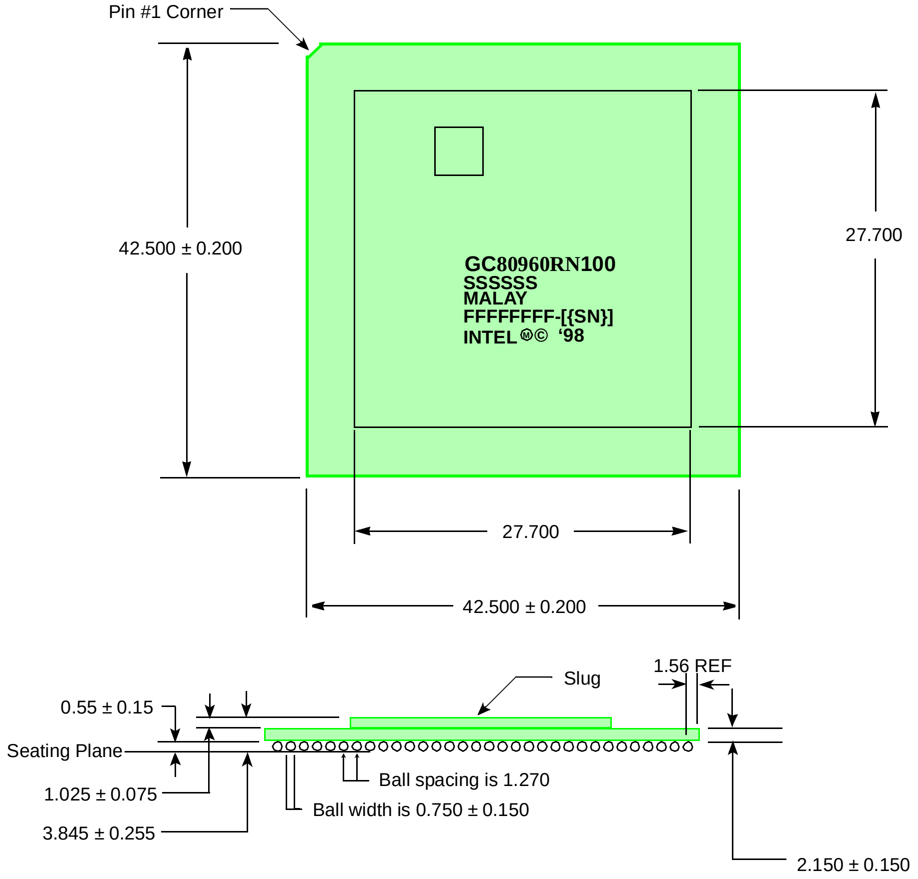
Name	Count	Type	Description
XINT[3:0]#/ **S_INT[D:A]#**	4	I 5V Async	**SECONDARY PCI BUS INTERRUPT REQUESTS. S_INT[D:A]#** assertion and deassertion is asynchronous to **P_CLK**. As device asserts **S_INT[D:A]#** when requesting attention from it device driver. When **S_INT[D:A]#** is asserted, it remains asserted until the device driver clears the pending request. **S_INT[D:A]#** interrupts are level low sensitive. **EXTERNAL INTERRUPT**. External devices use this signal to request an interrupt service. These signals operate in dedicated mode, where each signal is assigned a dedicated interrupt level. The **S_INT[D:A]#/XINT[3:0]#** signals can be directed as follows: **Sec. PCIPrimary PCI**i960 core processor S_INTA#⇒P_INTA# or XINT0# S_INTB#⇒P_INTB# or XINT1# S_INTC#⇒P_INTC# or XINT2# S_INTD#⇒P_INTD# or XINT3#
XINT[5:4]#	2	I 5V Async	**EXTERNAL INTERRUPT** pins are used to request 80960RN interrupt service.
NMI#	1	I 5V Async	**NON-MASKABLE INTERRUPT** causes an i960 core processor non-maskable interrupt event to occur. **NMI#** is the highest priority interrupt source.
V_{CC5REF}	1	-	**INPUT REFERENCE VOLTAGE** is strapped to 5 V. This reference voltage allows the 80960RN input pins to be 5 V tolerant.
V_{CCPLL}	3	-	**PLL POWER** is a separate V_{CC} supply pin for the phase lock loop clock generator. It is intended for external connection to the V_{CC} board plane. In noisy environments, add a simple bypass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships.
FAIL#	1	O Irst(0)	**FAIL** indicates a failure of the processor's built-in self-test performed during initialization. **FAIL#** is asserted immediately upon reset and toggles during self-test to indicate the status of individual tests: When self-test passes, the processor deasserts **FAIL#** and commences operation from user code. When self-test fails, the processor asserts **FAIL#** and then stops executing. Self-test failing does not cause the bridge to stop execution. 0 = Self Test Failed 1 = Self Test Passed

Table 9. I^2C, JTAG, Core Signals

Name	Count	Type	Description
TCK	1	I 5V	**TEST CLOCK** is an input which provides the clocking function for the IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the component on the rising edge and data is clocked out of the component on the falling edge.
TDI	1	I 5V Sync(T)	**TEST DATA INPUT** is the serial input pin for the JTAG feature. TDI is sampled on the rising edge of **TCK**, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pull-up to ensure proper operation when this signal is unconnected.
TDO	1	O	**TEST DATA OUTPUT** is the serial output pin for the JTAG feature. **TDO** is driven on the falling edge of **TCK** during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, **TDO** floats.
TRST#	1	I 5V Async	**TEST RESET** asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan Testing (JTAG). This signal has a weak internal pull-up to ensure proper operation when this signal is unconnected.
TMS	1	I 5V Sync(T)	**TEST MODE SELECT** is sampled at the rising edge of **TCK** to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing. This signal has a weak internal pull-up to ensure proper operation when this signal is unconnected.
SDA	1	I/O 5V OD Irst(Z)	**I^2C DATA** is used for data transfer and arbitration on the I^2C bus.
SCL	1	I/O 5V OD Irst(Z)	**I^2C CLOCK** provides synchronous operation of the I^2C bus.
LCDINIT#	1	I Sync(I)	**LCD INITIALIZATION** is a static signal used to initialize the internal logic for the LCD960 debugger. This signal has an internal pull-up for normal operation.
I_RST#	1	**O** Async	**INTERNAL BUS RESET** indicates when the internal bus has been reset with **P_RST#** or a software reset.
ONCE# (Config. Pin)	1	I 5V	**ONCE MODE**: The processor samples this pin during reset. If it is asserted LOW at the end of reset, the processor enters **ONCE** Mode. In ONCE Mode, the processor stops all clocks and floats all output pins except the **TDO** and RAD[8:0] pins. The pin has a weak internal pull-up which is active during reset to ensure normal operation if the pin is left unconnected.

3.1.2 540-Lead H-PBGA Package

Figure 3. 540L H-PBGA Package Diagram (Top and Side View)



NOTES:

1. All dimensions and tolerances conform to ANSI Y14.5M 1982.
2. Dimensions are measured at the maximum solder ball diameter parallel to primary datum.
3. Primary datum and seating plane are defined by the spherical crowns of the solder balls.
4. All dimensions are in millimeters.
5. S spec numbers are only printed on the C-X steppings.

Figure 4. 540L H-PBGA Package Diagram (Bottom View)

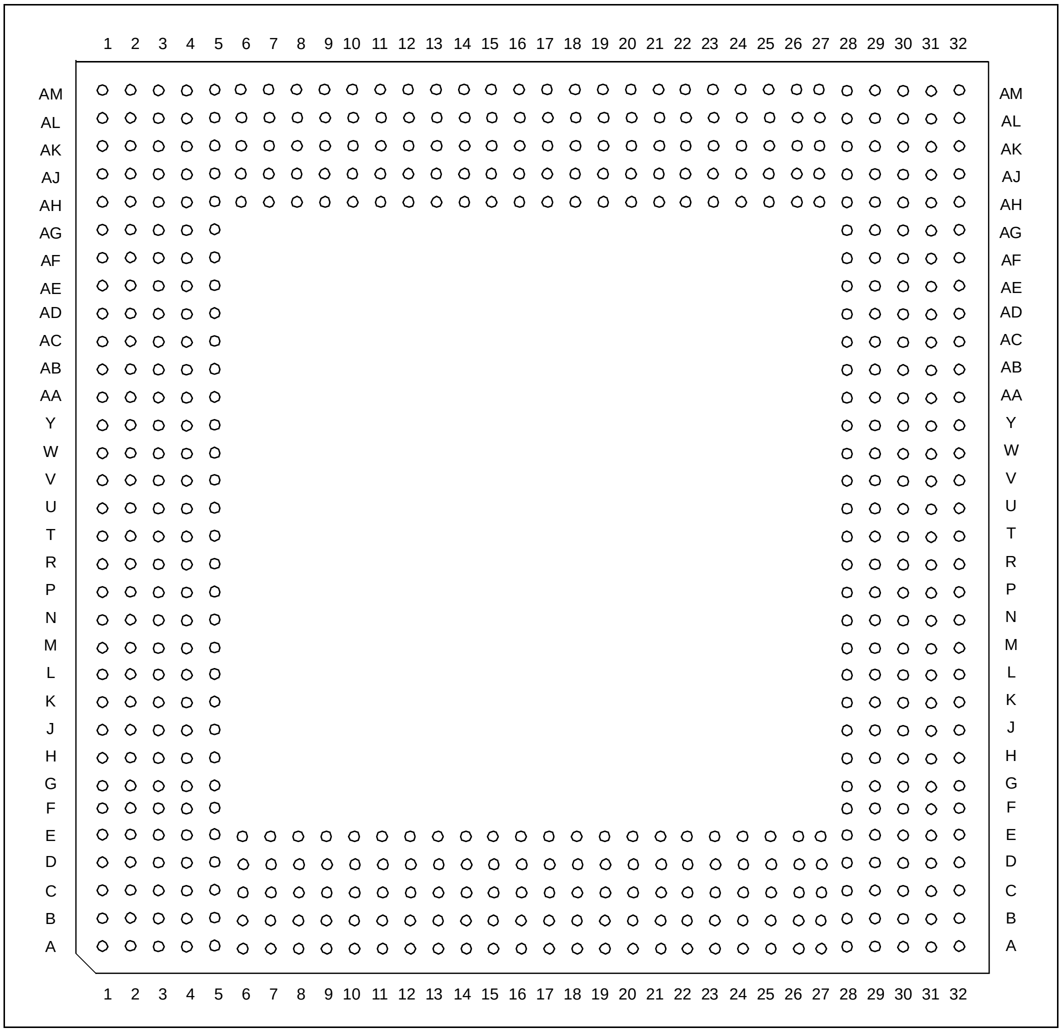


Table 10. 540-Lead H-PBGA Package — Signal Name Order (Sheet 1 of 5)

Signal	Ball #	Signal	Ball #	Signal	Ball #
DCLKIN	E21	DQ35	C24	N/C	AG1
DCLKOUT	A22	DQ36	E24	N/C	AL16
DQ00	D22	DQ37	B25	P_ACK64#	V5
DQ01	A23	DQ38	E25	P_AD00	U1
DQ02	C23	DQ39	C26	P_AD01	U2
DQ03	A24	DQ40	A27	P_AD02	U3
DQ04	D24	DQ41	C27	P_AD03	T1
DQ05	A25	DQ42	A28	P_AD04	T3
DQ06	C25	DQ43	G32	P_AD05	T4
DQ07	A26	DQ44	H31	P_AD06	T5
DQ08	E26	DQ45	H28	P_AD07	R1
DQ09	B27	DQ46	J30	P_AD08	R3
DQ10	E27	DQ47	J28	P_AD09	R5
DQ11	C28	DQ48	W28	P_AD10	P1
DQ12	H32	DQ49	Y31	P_AD11	P3
DQ13	H30	DQ50	Y28	P_AD12	P4
DQ14	J32	DQ51	AA30	P_AD13	P5
DQ15	J29	DQ52	AA28	P_AD14	N1
DQ16	W29	DQ53	AB31	P_AD15	N2
DQ17	Y32	DQ54	AB28	P_AD16	K3
DQ18	Y30	DQ55	AC30	P_AD17	K4
DQ19	AA32	DQ56	AC28	P_AD18	K5
DQ20	AA29	DQ57	AD31	P_AD19	J1
DQ21	AB32	DQ58	AD28	P_AD20	J2
DQ22	AB30	DQ59	AE30	P_AD21	J3
DQ23	AC32	DQ60	AE28	P_AD22	J5
DQ24	AC29	DQ61	AF31	P_AD23	H1
DQ25	AD32	DQ62	AF28	P_AD24	H5
DQ26	AD30	DQ63	AH32	P_AD25	G1
DQ27	AE32	FAIL#	E12	P_AD26	G2
DQ28	AE29	LCDINIT#	A21	P_AD27	G3
DQ29	AF32	I_RST#	A11	P_AD28	E5
DQ30	AF30	ONCE#	C21	P_AD29	A6
DQ31	AG32	NMI#	A9	P_AD30	C6
DQ32	E22	N/C	A16	P_AD31	D6
DQ33	B23	N/C	G5	P_AD32	AG2
DQ34	E23	N/C	V28	P_AD33	AG3

Table 10. 540-Lead H-PBGA Package — Signal Name Order (Sheet 2 of 5)

Signal	Ball #	Signal	Ball #	Signal	Ball #
P_AD34	AF1	P_C/BE6#	V3	RALE	B19
P_AD35	AF3	P_C/BE7#	V4	RCE0#	C19
P_AD36	AF4	P_FRAME#	L5	RCE1#	E19
P_AD37	AF5	P_DEVSEL#	L1	P_IDSEL	H3
P_AD38	AE1	P_GNT#	A7	ROE#	D20
P_AD39	AE2	P_INTA#	E8	RWE#	A20
P_AD40	AE3	P_INTB#	D8	SA00	N30
P_AD41	AE5	P_INTC#	E7	SA01	N29
P_AD42	AD1	P_INTD#	C7	SA02	N28
P_AD43	AD3	P_IRDY#	L3	SA03	P32
P_AD44	AD4	P_LOCK#	M4	SA04	P31
P_AD45	AD5	P_PAR	N3	SA05	P30
P_AD46	AC1	P_PAR64	W3	SA06	P28
P_AD47	AC2	P_PERR#	M3	SA07	R32
P_AD48	AC3	P_SERR#	M1	SA08	R30
P_AD49	AC5	P_STOP#	M5	SA09	R29
P_AD50	AB1	P_REQ#	E6	SA10	R28
P_AD51	AB3	P_REQ64#	U5	SA11	T32
P_AD52	AB4	P_RST#	B7	SBA0	T31
P_AD53	AB5	P_TRDY#	L2	SBA1	T30
P_AD54	AA1	RAD00	A13	SCAS#	L30
P_AD55	AA2	RAD01	B13	SCB0	K32
P_AD56	AA3	RAD02	C13	SCB1	K30
P_AD57	AA5	RAD03	E13	SCB2	V31
P_AD58	Y1	RAD04	A14	SCB3	W32
P_AD59	Y3	RAD05	C14	SCB4	K31
P_AD60	Y4	RAD06	D14	SCB5	K28
P_AD61	Y5	RAD07	E14	SCB6	V30
P_AD62	W1	RAD08	A15	SCB7	W30
P_AD63	W2	RAD09	C15	SCE0#	M30
P_CLK	C20	RAD10	E15	SCE1#	M28
P_C/BE0#	R2	RAD11	E17	SCKE0	T28
P_C/BE1#	N5	RAD12	A18	SCKE1	U32
P_C/BE2#	K1	RAD13	C18	SCL	A8
P_C/BE3#	H4	RAD14	D18	SDA	C8
P_C/BE4#	W5	RAD15	E18	SDQM0	L29
P_C/BE5#	V1	RAD16	A19	SDQM1	M32

Table 10. 540-Lead H-PBGA Package — Signal Name Order (Sheet 3 of 5)

Signal	Ball #	Signal	Ball #	Signal	Ball #
SDQM2	U30	S_AD28	AJ25	S_C/BE1#	AJ19
SDQM3	U28	S_AD29	AK25	S_C/BE2#	AM21
SDQM4	L28	S_AD30	AM25	S_C/BE3#	AH24
SDQM5	M31	S_AD31	AH26	S_C/BE4#	AL12
SDQM6	U29	S_AD32	AH1	S_C/BE5#	AM12
SDQM7	V32	S_AD33	AH3	S_C/BE6#	AH13
SRAS#	N32	S_AD34	AH4	S_C/BE7#	AJ13
SWE#	L32	S_AD35	AJ2	S_DEVSEL#	AM20
S_ACK64#	AM13	S_AD36	AJ5	S_FRAME#	AK21
S_AD00	AH14	S_AD37	AK5	S_GNT0#	AM26
S_AD01	AK14	S_AD38	AM5	S_GNT1#	AJ27
S_AD02	AL14	S_AD39	AH6	S_GNT2#	AM27
S_AD03	AM14	S_AD40	AK6	S_GNT3#	AK28
S_AD04	AH15	S_AD41	AL6	S_GNT4#	AM28
S_AD05	AJ15	S_AD42	AM6	S_GNT5#	AK29
S_AD06	AK15	S_AD43	AH7	S_IRDY#	AJ21
S_AD07	AM15	S_AD44	AJ7	S_LOCK#	AK20
S_AD08	AJ17	S_AD45	AK7	S_PAR	AK19
S_AD09	AK17	S_AD46	AM7	S_PAR64	AK12
S_AD10	AM17	S_AD47	AH8	S_PERR#	AH20
S_AD11	AH18	S_AD48	AK8	S_REQ0#	AL26
S_AD12	AK18	S_AD49	AL8	S_REQ1#	AH27
S_AD13	AL18	S_AD50	AM8	S_REQ2#	AK27
S_AD14	AM18	S_AD51	AH9	S_REQ3#	AH28
S_AD15	AH19	S_AD52	AJ9	S_REQ4#	AL28
S_AD16	AH22	S_AD53	AK9	S_REQ5#	AJ29
S_AD17	AK22	S_AD54	AM9	S_REQ64#	AK13
S_AD18	AL22	S_AD55	AH10	S_RST#	AK26
S_AD19	AM22	S_AD56	AK10	S_SERR#	AM19
S_AD20	AH23	S_AD57	AL10	S_STOP#	AL20
S_AD21	AJ23	S_AD58	AM10	S_TRDY#	AH21
S_AD22	AK23	S_AD59	AH11	TCK	C12
S_AD23	AM23	S_AD60	AJ11	TDI	A12
S_AD24	AK24	S_AD61	AK11	TDO	E11
S_AD25	AL24	S_AD62	AM11	TMS	B11
S_AD26	AM24	S_AD63	AH12	TRST#	C11
S_AD27	AH25	S_C/BE0#	AH17	V_{CC}	A17

Table 10. 540-Lead H-PBGA Package — Signal Name Order (Sheet 4 of 5)

Signal	Ball #	Signal	Ball #	Signal	Ball #
V_{CC}	A29	V_{CC}	F2	V_{CC}	AL3
V_{CC}	B2	V_{CC}	F3	V_{CC}	AL4
V_{CC}	B3	V_{CC}	F4	V_{CC}	AL5
V_{CC}	B4	V_{CC}	G30	V_{CC}	AL7
V_{CC}	B5	V_{CC}	G31	V_{CC}	AL9
V_{CC}	B6	V_{CC}	H2	V_{CC}	AL11
V_{CC}	B8	V_{CC}	J31	V_{CC}	AL13
V_{CC}	B10	V_{CC}	K2	V_{CC}	AL15
V_{CC}	B12	V_{CC}	L31	V_{CC}	AL17
V_{CC}	B14	V_{CC}	M2	V_{CC}	AL19
V_{CC}	B16	V_{CC}	N31	V_{CC}	AL21
V_{CC}	B17	V_{CC}	P2	V_{CC}	AL23
V_{CC}	B18	V_{CC}	R31	V_{CC}	AL25
V_{CC}	B20	V_{CC}	T2	V_{CC}	AL27
V_{CC}	B22	V_{CC}	U31	V_{CC}	AL29
V_{CC}	B24	V_{CC}	V2	V_{CC}	AL30
V_{CC}	B26	V_{CC}	W31	V_{CC}	AL31
V_{CC}	B28	V_{CC}	Y2	V_{CC}	AM4
V_{CC}	B29	V_{CC}	AA31	V_{CC}	AM16
V_{CC}	B30	V_{CC}	AB2	V_{CC5REF}	E20
V_{CC}	B31	V_{CC}	AC31	V_{CCPLL1}	C22
V_{CC}	C2	V_{CC}	AD2	V_{CCPLL2}	B15
V_{CC}	C3	V_{CC}	AE31	V_{CCPLL3}	D26
V_{CC}	C5	V_{CC}	AF2	V_{SS}	A1
V_{CC}	C16	V_{CC}	AG30	V_{SS}	A2
V_{CC}	C29	V_{CC}	AG31	V_{SS}	A3
V_{CC}	C30	V_{CC}	AH2	V_{SS}	A4
V_{CC}	C31	V_{CC}	AH30	V_{SS}	A5
V_{CC}	D2	V_{CC}	AH31	V_{SS}	A30
V_{CC}	D12	V_{CC}	AJ1	V_{SS}	A31
V_{CC}	D30	V_{CC}	AJ30	V_{SS}	A32
V_{CC}	D31	V_{CC}	AJ31	V_{SS}	B1
V_{CC}	D32	V_{CC}	AK2	V_{SS}	B21
V_{CC}	E2	V_{CC}	AK3	V_{SS}	B32
V_{CC}	E3	V_{CC}	AK30	V_{SS}	C1
V_{CC}	E10	V_{CC}	AK31	V_{SS}	C4
V_{CC}	E31	V_{CC}	AL2	V_{SS}	C17

Table 10. 540-Lead H-PBGA Package — Signal Name Order (Sheet 5 of 5)

Signal	Ball #	Signal	Ball #	Signal	Ball #
V_{SS}	C32	V_{SS}	F32	V_{SS}	AJ6
V_{SS}	D1	V_{SS}	G4	V_{SS}	AJ8
V_{SS}	D3	V_{SS}	G28	V_{SS}	AJ10
V_{SS}	D4	V_{SS}	G29	V_{SS}	AJ12
V_{SS}	D5	V_{SS}	H29	V_{SS}	AJ14
V_{SS}	D7	V_{SS}	J4	V_{SS}	AJ16
V_{SS}	D9	V_{SS}	K29	V_{SS}	AJ18
V_{SS}	D11	V_{SS}	L4	V_{SS}	AJ20
V_{SS}	D13	V_{SS}	M29	V_{SS}	AJ22
V_{SS}	D15	V_{SS}	N4	V_{SS}	AJ24
V_{SS}	D16	V_{SS}	P29	V_{SS}	AJ26
V_{SS}	D17	V_{SS}	R4	V_{SS}	AJ28
V_{SS}	D19	V_{SS}	T29	V_{SS}	AJ32
V_{SS}	D21	V_{SS}	U4	V_{SS}	AK1
V_{SS}	D23	V_{SS}	V29	V_{SS}	AK4
V_{SS}	D25	V_{SS}	W4	V_{SS}	AK16
V_{SS}	D27	V_{SS}	Y29	V_{SS}	AK32
V_{SS}	D28	V_{SS}	AA4	V_{SS}	AL1
V_{SS}	D29	V_{SS}	AB29	V_{SS}	AL32
V_{SS}	E1	V_{SS}	AC4	V_{SS}	AM1
V_{SS}	E4	V_{SS}	AD29	V_{SS}	AM2
V_{SS}	E16	V_{SS}	AE4	V_{SS}	AM3
V_{SS}	E28	V_{SS}	AF29	V_{SS}	AM29
V_{SS}	E29	V_{SS}	AG4	V_{SS}	AM30
V_{SS}	E30	V_{SS}	AG5	V_{SS}	AM31
V_{SS}	E32	V_{SS}	AG28	V_{SS}	AM32
V_{SS}	F1	V_{SS}	AG29	XINT0#	B9
V_{SS}	F5	V_{SS}	AH5	XINT1#	C9
V_{SS}	F28	V_{SS}	AH16	XINT2#	E9
V_{SS}	F29	V_{SS}	AH29	XINT3#	A10
V_{SS}	F30	V_{SS}	AJ3	XINT4#	C10
V_{SS}	F31	V_{SS}	AJ4	XINT5#	D10

Table 11. 540-Lead H-PBGA Pinout — Ballpad Number Order (Sheet 1 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	V_{SS}	B6	V_{CC}	C11	TRST#
A2	V_{SS}	B7	P_RST#	C12	TCK
A3	V_{SS}	B8	V_{CC}	C13	RAD02
A4	V_{SS}	B9	XINT0#	C14	RAD05
A5	V_{SS}	B10	V_{CC}	C15	RAD09
A6	P_AD29	B11	TMS	C16	V_{CC}
A7	P_GNT#	B12	V_{CC}	C17	V_{SS}
A8	SCL	B13	RAD01	C18	RAD13
A9	NMI#	B14	V_{CC}	C19	RCE0#
A10	XINT3#	B15	V_{CCPLL2}	C20	P_CLK
A11	I_RST#	B16	V_{CC}	C21	ONCE#
A12	TDI	B17	V_{CC}	C22	V_{CCPLL1}
A13	RAD00	B18	V_{CC}	C23	DQ02
A14	RAD04	B19	RALE	C24	DQ35
A15	RAD08	B20	V_{CC}	C25	DQ06
A16	N/C	B21	V_{SS}	C26	DQ39
A17	V_{CC}	B22	V_{CC}	C27	DQ41
A18	RAD12	B23	DQ33	C28	DQ11
A19	RAD16	B24	V_{CC}	C29	V_{CC}
A20	RWE#	B25	DQ37	C30	V_{CC}
A21	LCDINIT#	B26	V_{CC}	C31	V_{CC}
A22	DCLKOUT	B27	DQ09	C32	V_{SS}
A23	DQ01	B28	V_{CC}	D1	V_{SS}
A24	DQ03	B29	V_{CC}	D2	V_{CC}
A25	DQ05	B30	V_{CC}	D3	V_{SS}
A26	DQ07	B31	V_{CC}	D4	V_{SS}
A27	DQ40	B32	V_{SS}	D5	V_{SS}
A28	DQ42	C1	V_{SS}	D6	P_AD31
A29	V_{CC}	C2	V_{CC}	D7	V_{SS}
A30	V_{SS}	C3	V_{CC}	D8	P_INTB#
A31	V_{SS}	C4	V_{SS}	D9	V_{SS}
A32	V_{SS}	C5	V_{CC}	D10	XINT5#
B1	V_{SS}	C6	P_AD30	D11	V_{SS}
B2	V_{CC}	C7	P_INTD#	D12	V_{CC}
B3	V_{CC}	C8	SDA	D13	V_{SS}
B4	V_{CC}	C9	XINT1#	D14	RAD06
B5	V_{CC}	C10	XINT4#	D15	V_{SS}

Table 11. 540-Lead H-PBGA Pinout — Ballpad Number Order (Sheet 2 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
D16	V_{SS}	E21	DCLKIN	H28	DQ45
D17	V_{SS}	E22	DQ32	H29	V_{SS}
D18	RAD14	E23	DQ34	H30	DQ13
D19	V_{SS}	E24	DQ36	H31	DQ44
D20	ROE#	E25	DQ38	H32	DQ12
D21	V_{SS}	E26	DQ08	J1	P_AD19
D22	DQ00	E27	DQ10	J2	P_AD20
D23	V_{SS}	E28	V_{SS}	J3	P_AD21
D24	DQ04	E29	V_{SS}	J4	V_{SS}
D25	V_{SS}	E30	V_{SS}	J5	P_AD22
D26	V_{CCPLL3}	E31	V_{CC}	J28	DQ47
D27	V_{SS}	E32	V_{SS}	J29	DQ15
D28	V_{SS}	F1	V_{SS}	J30	DQ46
D29	V_{SS}	F2	V_{CC}	J31	V_{CC}
D30	V_{CC}	F3	V_{CC}	J32	DQ14
D31	V_{CC}	F4	V_{CC}	K1	P_C/BE2#
D32	V_{CC}	F5	V_{SS}	K2	V_{CC}
E1	V_{SS}	F28	V_{SS}	K3	P_AD16
E2	V_{CC}	F29	V_{SS}	K4	P_AD17
E3	V_{CC}	F30	V_{SS}	K5	P_AD18
E4	V_{SS}	F31	V_{SS}	K28	SCB5
E5	P_AD28	F32	V_{SS}	K29	V_{SS}
E6	P_REQ#	G1	P_AD25	K30	SCB1
E7	P_INTC#	G2	P_AD26	K31	SCB4
E8	P_INTA#	G3	P_AD27	K32	SCB0
E9	XINT2#	G4	V_{SS}	L1	P_DEVSEL#
E10	V_{CC}	G5	N/C	L2	P_TRDY#
E11	TDO	G28	V_{SS}	L3	P_IRDY#
E12	FAIL#	G29	V_{SS}	L4	V_{SS}
E13	RAD03	G30	V_{CC}	L5	P_FRAME#
E14	RAD07	G31	V_{CC}	L28	SDQM4
E15	RAD10	G32	DQ43	L29	SDQM0
E16	V_{SS}	H1	P_AD23	L30	SCAS#
E17	RAD11	H2	V_{CC}	L31	V_{CC}
E18	RAD15	H3	P_IDSEL	L32	SWE#
E19	RCE1#	H4	P_C/BE3#	M1	P_SERR#
E20	V_{CC5REF}	H5	P_AD24	M2	V_{CC}

Table 11. 540-Lead H-PBGA Pinout — Ballpad Number Order (Sheet 3 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
M3	P_PERR#	R32	SA07	W29	DQ16
M4	P_LOCK#	T1	P_AD03	W30	SCB7
M5	P_STOP#	T2	V_{CC}	W31	V_{CC}
M28	SCE1#	T3	P_AD04	W32	SCB3
M29	V_{SS}	T4	P_AD05	Y1	P_AD58
M30	SCE0#	T5	P_AD06	Y2	V_{CC}
M31	SDQM5	T28	SCKE0	Y3	P_AD59
M32	SDQM1	T29	V_{SS}	Y4	P_AD60
N1	P_AD14	T30	SBA1	Y5	P_AD61
N2	P_AD15	T31	SBA0	Y28	DQ50
N3	P_PAR	T32	SA11	Y29	V_{SS}
N4	V_{SS}	U1	P_AD00	Y30	DQ18
N5	P_C/BE1#	U2	P_AD01	Y31	DQ49
N28	SA02	U3	P_AD02	Y32	DQ17
N29	SA01	U4	V_{SS}	AA1	P_AD54
N30	SA00	U5	P_REQ64#	AA2	P_AD55
N31	V_{CC}	U28	SDQM3	AA3	P_AD56
N32	SRAS#	U29	SDQM6	AA4	V_{SS}
P1	P_AD10	U30	SDQM2	AA5	P_AD57
P2	V_{CC}	U31	V_{CC}	AA28	DQ52
P3	P_AD11	U32	SCKE1	AA29	DQ20
P4	P_AD12	V1	P_C/BE5#	AA30	DQ51
P5	P_AD13	V2	V_{CC}	AA31	V_{CC}
P28	SA06	V3	P_C/BE6#	AA32	DQ19
P29	V_{SS}	V4	P_C/BE7#	AB1	P_AD50
P30	SA05	V5	P_ACK64#	AB2	V_{CC}
P31	SA04	V28	N/C	AB3	P_AD51
P32	SA03	V29	V_{SS}	AB4	P_AD52
R1	P_AD07	V30	SCB6	AB5	P_AD53
R2	P_C/BE0#	V31	SCB2	AB28	DQ54
R3	P_AD08	V32	SDQM7	AB29	V_{SS}
R4	V_{SS}	W1	P_AD62	AB30	DQ22
R5	P_AD09	W2	P_AD63	AB31	DQ53
R28	SA10	W3	P_PAR64	AB32	DQ21
R29	SA09	W4	V_{SS}	AC1	P_AD46
R30	SA08	W5	P_C/BE4#	AC2	P_AD47
R31	V_{CC}	W28	DQ48	AC3	P_AD48

Table 11. 540-Lead H-PBGA Pinout — Ballpad Number Order (Sheet 4 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
AC4	V_{SS}	AG1	N/C	AH28	S_REQ3#
AC5	P_AD49	AG2	P_AD32	AH29	V_{SS}
AC28	DQ56	AG3	P_AD33	AH30	V_{CC}
AC29	DQ24	AG4	V_{SS}	AH31	V_{CC}
AC30	DQ55	AG5	V_{SS}	AH32	DQ63
AC31	V_{CC}	AG28	V_{SS}	AJ1	V_{CC}
AC32	DQ23	AG29	V_{SS}	AJ2	S_AD35
AD1	P_AD42	AG30	V_{CC}	AJ3	V_{SS}
AD2	V_{CC}	AG31	V_{CC}	AJ4	V_{SS}
AD3	P_AD43	AG32	DQ31	AJ5	S_AD36
AD4	P_AD44	AH1	S_AD32	AJ6	V_{SS}
AD5	P_AD45	AH2	V_{CC}	AJ7	S_AD44
AD28	DQ58	AH3	S_AD33	AJ8	V_{SS}
AD29	V_{SS}	AH4	S_AD34	AJ9	S_AD52
AD30	DQ26	AH5	V_{SS}	AJ10	V_{SS}
AD31	DQ57	AH6	S_AD39	AJ11	S_AD60
AD32	DQ25	AH7	S_AD43	AJ12	V_{SS}
AE1	P_AD38	AH8	S_AD47	AJ13	S_C/BE7#
AE2	P_AD39	AH9	S_AD51	AJ14	V_{SS}
AE3	P_AD40	AH10	S_AD55	AJ15	S_AD05
AE4	V_{SS}	AH11	S_AD59	AJ16	V_{SS}
AE5	P_AD41	AH12	S_AD63	AJ17	S_AD08
AE28	DQ60	AH13	S_C/BE6#	AJ18	V_{SS}
AE29	DQ28	AH14	S_AD00	AJ19	S_C/BE1#
AE30	DQ59	AH15	S_AD04	AJ20	V_{SS}
AE31	V_{CC}	AH16	V_{SS}	AJ21	S_IRDY#
AE32	DQ27	AH17	S_C/BE0#	AJ22	V_{SS}
AF1	P_AD34	AH18	S_AD11	AJ23	S_AD21
AF2	V_{CC}	AH19	S_AD15	AJ24	V_{SS}
AF3	P_AD35	AH20	S_PERR#	AJ25	S_AD28
AF4	P_AD36	AH21	S_TRDY#	AJ26	V_{SS}
AF5	P_AD37	AH22	S_AD16	AJ27	S_GNT1#
AF28	DQ62	AH23	S_AD20	AJ28	V_{SS}
AF29	V_{SS}	AH24	S_C/BE3#	AJ29	S_REQ5#
AF30	DQ30	AH25	S_AD27	AJ30	V_{CC}
AF31	DQ61	AH26	S_AD31	AJ31	V_{CC}
AF32	DQ29	AH27	S_REQ1#	AJ32	V_{SS}

Table 11. 540-Lead H-PBGA Pinout — Ballpad Number Order (Sheet 5 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
AK1	V_{SS}	AL1	V_{SS}	AM1	V_{SS}
AK2	V_{CC}	AL2	V_{CC}	AM2	V_{SS}
AK3	V_{CC}	AL3	V_{CC}	AM3	V_{SS}
AK4	V_{SS}	AL4	V_{CC}	AM4	V_{CC}
AK5	S_AD37	AL5	V_{CC}	AM5	S_AD38
AK6	S_AD40	AL6	S_AD41	AM6	S_AD42
AK7	S_AD45	AL7	V_{CC}	AM7	S_AD46
AK8	S_AD48	AL8	S_AD49	AM8	S_AD50
AK9	S_AD53	AL9	V_{CC}	AM9	S_AD54
AK10	S_AD56	AL10	S_AD57	AM10	S_AD58
AK11	S_AD61	AL11	V_{CC}	AM11	S_AD62
AK12	S_PAR64	AL12	S_C/BE4#	AM12	S_C/BE5#
AK13	S_REQ64#	AL13	V_{CC}	AM13	S_ACK64#
AK14	S_AD01	AL14	S_AD02	AM14	S_AD03
AK15	S_AD06	AL15	V_{CC}	AM15	S_AD07
AK16	V_{SS}	AL16	N/C	AM16	V_{CC}
AK17	S_AD09	AL17	V_{CC}	AM17	S_AD10
AK18	S_AD12	AL18	S_AD13	AM18	S_AD14
AK19	S_PAR	AL19	V_{CC}	AM19	S_SERR#
AK20	S_LOCK#	AL20	S_STOP#	AM20	S_DEVSEL#
AK21	S_FRAME#	AL21	V_{CC}	AM21	S_C/BE2#
AK22	S_AD17	AL22	S_AD18	AM22	S_AD19
AK23	S_AD22	AL23	V_{CC}	AM23	S_AD23
AK24	S_AD24	AL24	S_AD25	AM24	S_AD26
AK25	S_AD29	AL25	V_{CC}	AM25	S_AD30
AK26	S_RST#	AL26	S_REQ0#	AM26	S_GNT0#
AK27	S_REQ2#	AL27	V_{CC}	AM27	S_GNT2#
AK28	S_GNT3#	AL28	S_REQ4#	AM28	S_GNT4#
AK29	S_GNT5#	AL29	V_{CC}	AM29	V_{SS}
AK30	V_{CC}	AL30	V_{CC}	AM30	V_{SS}
AK31	V_{CC}	AL31	V_{CC}	AM31	V_{SS}
AK32	V_{SS}	AL32	V_{SS}	AM32	V_{SS}

3.2 Package Thermal Specifications

The device is specified for operation when T_C (case temperature) is within the range of 0°C to 85°C, depending on operating conditions. Refer to the "*Thermal Data for the 540-lead PBGA package*" application note for more information regarding maximum case temperatures on the 540-lead PBGA package. Case temperature may be measured in any environment to determine whether the processor is within specified operating range. Measure the case temperature at the center of the top surface, opposite the ballpad.

3.2.1 Thermal Specifications

This section defines the terms used for thermal analysis.

3.2.1.1 Ambient Temperature

Ambient temperature, T_A, is the temperature of the ambient air surrounding the package. In a system environment, ambient temperature is the temperature of the air upstream from the package.

3.2.1.2 Case Temperature

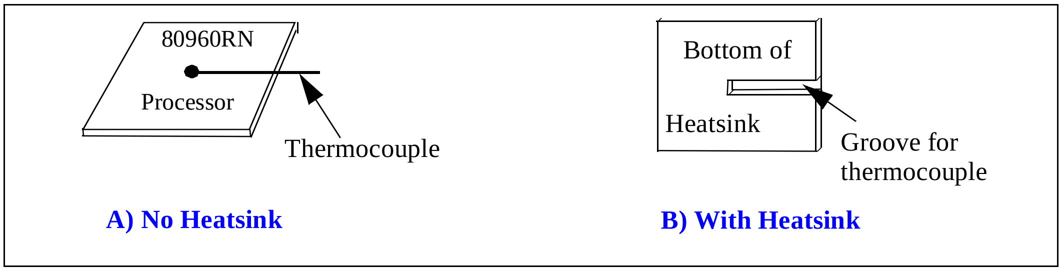
To ensure functionality and reliability, the device is specified for proper operation when the case temperature, T_C, is within the specified range as indicated in Table 12 "540-Lead H-PBGA Package Thermal Characteristics" on page 39.

When measuring case temperature, attention to detail is required to ensure accuracy. If a thermocouple is used, calibrate it before taking measurements. Errors may result when the measured surface temperature is affected by the surrounding ambient air temperature. Such errors may be due to a poor thermal contact between thermocouple junction and the surface, heat loss by radiation, or conduction through thermocouple leads.

To minimize measurement errors:

- Use a 35 gauge K-type thermocouple or equivalent.
- Attach the thermocouple bead or junction to the package top surface at a location corresponding to the center of the die (Figure 5A). The center of the die gives a more accurate measurement and less variation as the boundary condition changes.
- Attach the thermocouple bead at a 0° angle with respect to the package as shown in Figure 5A, when no heatsink is attached.
- When a passive heat sink is attached, a groove is made on the bottom surface of the heatsink and the thermocouple is attached at a 0° angle, as shown in Figure 5B.

Figure 5. Thermocouple Attachment - A) No Heatsink / B) With Heatsink



A) No Heatsink

B) With Heatsink

3.2.1.3 Thermal Resistance

The thermal resistance value for the case-to-ambient, θ_{CA}, is used as a measure of the cooling solution's thermal performance.

3.2.2 Thermal Analysis

Table 12 lists the case-to-ambient thermal resistances of the 80960RN for different air flow rates with and without a heat sink.

To calculate T_A, the maximum ambient temperature to conform to a particular case temperature:

$$T_A = T_C - P(\theta_{CA})$$

Compute P by multiplying I_{CC} and V_{CC}. Values for θ_{JC} and θ_{CA} are given in Table 12.

Junction temperature (T_J) is commonly used in reliability calculations. T_J can be calculated from θ_{JC} (thermal resistance from junction to case) using the following equation:

$$T_J = T_C + P(\theta_{JC})$$

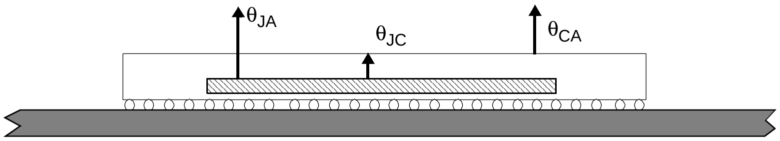
Similarly, when T_A is known, the corresponding case temperature (T_C) can be calculated as follows:

$$T_C = T_A + P(\theta_{CA})$$

The θ_{JA} (Junction to Ambient) for this package is currently estimated at 13.10° C/Watt with no airflow and no heatsink. The θ_{JA} (Junction to Ambient) for this package is currently estimated at 8.30° C/Watt with no airflow and a passive heatsink:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

Table 12. 540-Lead H-PBGA Package Thermal Characteristics

Thermal Resistance — °C/Watt								
Parameter	Airflow — ft./min (m/sec)							
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	300 (1.52)	400 (2.03)	600 (3.04)	800 (4.06)
θ_{JC} (Junction-to-Case)	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
θ_{CA} (Case-to-Ambient) Without Heatsink	12.66	11.61	10.66	9.26	8.26	7.61	6.57	5.78
θ_{CA} (Case-to-Ambient) With Passive 0.25 in. Heatsink[2,3]	9.0	8.2	7.5	6.1	5.1	4.7	3.8	3.2
θ_{CA} (Case-to-Ambient) With Passive 0.35 in. Heatsink[2]	7.86	6.96	6.06	4.56	3.66	3.16	2.56	2.16
								

3.3 Heat Sink Information

Under normal circumstances, a heat sink is not required for the 80960RN.

Table 13 provides a list of suggested sources for heat sinks. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

Table 13. Heat Sink Vendors and Contacts

Company	Factory Representative	Phone #	Fax #	Heatsink Part #
				Passive
AAVID Thermalloy, Inc 80 Commercial Street Concord, NH 03301 USA info@aavid.com http://www.aavidthermalloy.com/atp/atp.html	Attention: Sales	(603) 224-9988	(603) 223-1790	21933B withoou thermal grease (uses pins) 21935B withoou thermal grease (uses pins)

3.4 Vendor Information

Table 14 through Table 18 provide vendor details for socket-headers, burn-in sockets, shipping trays, logic analyzer interposers and JTAG emulators for the Intel® 80960RN. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

3.4.1 Socket-Header Vendor

Table 14. Socket-Header Vendor

Company	Factory Representative	Phone/Fax #	Part #	
			BGA 540 Pin Header	BGA 540 Pin Socket Carrier
Adapter Technologies, Inc. 214-218 South 4th St. Perkasie, PA 18944	John Miller	215-258-5750/ 215-258-5760	BGAH-540-0-01-3201-0277-1	BGA-540-0-02-3201-0275P-130

3.4.2 Burn-in Socket Vendor

Table 15. Burn-in Socket Vendor

Company	Factory Representative	Phone #	Burn-in Socket Part #
Texas Instruments 111 Forbes Blvd. Mansfield, MA 02048	W. Ray Johnson	508-236-5375	ULGA540-005

3.4.3 Shipping Tray Vendor

Table 16. Shipping Tray Vendor

Company	Factory Representative	Phone #	Shipping Tray Part #
3M	Ron Goth	602-465-5381	7-0000-21001-184-167

3.4.4 Logic Analyzer Interposer Vendor

Table 17. Logic Analyzer Interposer Vendor

Company	Factory Representative	Phone/Fax #	Part #
Packard-Hughes Interconnect 17150 Von Karman Ave Irvine, CA 92614-0968	Karen May	949-660-5773 949-660-5825	1126898

3.4.5 JTAG Emulator Vendor

3.5

Table 18. JTAG Emulator Vendor

Company	Factory Representative	Phone/ Fax #	Part #
Spectrum Digital, Inc.	Jeff Bond	281-494-4500/ 281-494-5310	701500

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–55°C to + 125°C
Case Temperature Under Bias	0°C to + 85°C
Supply Voltage wrt. V_{SS}	–0.5 V to + 4.6 V
Supply Voltage wrt. V_{SS} on $\mathbf{V_{CC5}}$	–0.5 V to + 6.5 V
Voltage on Any Ball wrt. V_{SS}	–0.5 V to V_{CC} + 0.5 V

NOTICE: This data sheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.

†**WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 19. Operating Conditions

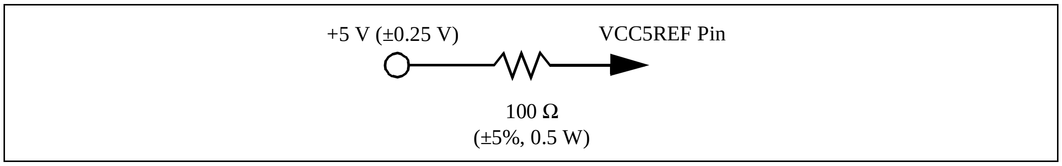
Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.6	V	
V_{CC5}	Input Protection Bias	V_{CC}	V_{CC}+2.5	V	
F_{P_CLK}	Input Clock Frequency	16	33.33	MHz	
T_C	Case Temperature Under Bias GC (540L PBGA)	0	85	°C	

4.2 V_{CC5REF} Pin Requirements (V_{DIFF})

In mixed voltage systems that drive 80960RN processor inputs in excess of 3.3 V, the $\mathbf{V_{CC5REF}}$ pin must be connected to the system's 5 V supply. To limit current flow into the $\mathbf{V_{CC5REF}}$ pin, there is a limit to the voltage differential between the $\mathbf{V_{CC5REF}}$ pin and the other V_{CC} pins. The voltage differential between the $\mathbf{V_{CC5REF}}$ pin and its 3.3 V V_{CC} pins should never exceed 2.25 V. This limit applies to power-up, power-down, and steady-state operation. Table 20 outlines this requirement.

If the voltage difference requirements cannot be met due to system design limitations, an alternate solution may be employed. As shown in Figure 6, a minimum of 100 Ω series resistor may be used to limit the current into the $\mathbf{V_{CC5REF}}$ pin. This resistor ensures that current drawn by the $\mathbf{V_{CC5REF}}$ pin does not exceed the maximum rating for this pin.

Figure 6. V_{CC5REF} Current-Limiting Resistor



This resistor is not necessary in systems that can guarantee the V_{DIFF} specification.

In 3.3 V-only systems (only applies to 80960RN C-x steppings) and systems that drive pins from 3.3 V logic, connect the $\mathbf{V_{CC5REF}}$ pin directly to the 3.3 V V_{CC} plane.

Table 20. V_{DIFF} Specification for Dual Power Supply Requirements (3.3 V, 5 V)

Symbol	Parameter	Min	Max	Units	Notes
V_{DIFF}	V_{CC5}-V_{CC} Difference		2.25	V	(1)

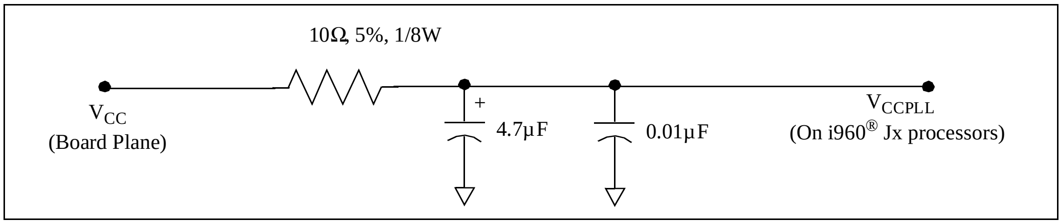
NOTE:

1. $\mathbf{V_{CC5REF}}$ input should not exceed V_{CC} by more than 2.25 V during power-up and power-down, or during steady-state operation.

4.3 V_{CCPLL} Pin Requirements

To reduce clock skew on the i960 Jx processor, the V_{CCPLL} pin for the Phase Lock Loop (PLL) circuit is isolated on the pinout. The lowpass filter, as shown in Figure 7, reduces noise induced clock jitter and its effects on timing relationships in system designs. The trace lengths between the 4.7 µF capacitor, the 0.01 µF capacitor, and V_{CCPLL} must be as short as possible.

Figure 7. V_{CCPLL} Lowpass Filter



4.4 Targeted DC Specifications

Table 21. DC Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL5}	Input Low Voltage 5 Volt PCI	-0.5	0.8	V	(1,4)
V_{IH5}	Input High Voltage 5 Volt PCI	2	V_{CC} + 0.5	V	(1,4)
$V_{IL3.3}$	Input Low Voltage 3.3 Volt PCI	-0.5	0.3V_{CC}	V	(1,4,5)
$V_{IH3.3}$	Input High Voltage 3.3 Volt PCI	0.5V_{CC}	V_{CC} + 0.5	V	(1,4,5)
V_{OL1}	Output Low Voltage Processor signals		0.4	V	I_{OL} = 6 mA (3)
V_{OH1}	Output High Voltage Processor signals	2.4 V_{CC} - 0.5		V	I_{OH} = -2 mA (3) I_{OH} = -200 µA (3, 6)
V_{OL2}	Output Low Voltage 5 V PCI / Flash signals		0.4	V	I_{OL} = 6 mA (1)
V_{OH2}	Output High Voltage 5 V PCI / Flash signals	2.4		V	I_{OH} = -2 mA (1)
V_{OL3}	Output Low Voltage SDRAM signals	-2.0	0.4	V	I_{OL} = 3 mA (4)
V_{OH3}	Output High Voltage SDRAM signals	2.4	V_{CC} + 2.0	V	I_{OH} = -2 mA (4)
V_{OL4}	Output Low Voltage 3.3 V PCI signals		0.1V_{CC}	V	I_{OL} = 1500 µA (1,5)
V_{OH4}	Output Low Voltage 3.3 V PCI signals	0.9V_{CC}		V	I_{OH} = -500 µA (1,5)
C_{IN}	Input Capacitance - PBGA		10	pF	$F_{S\_CLK} = T_F$ Min (1, 2)
C_{OUT}	I/O or Output Capacitance - PBGA		10	pF	$F_{S\_CLK} = T_F$ Min (1, 2)
C_{CLK}	S_CLK Capacitance - PBGA	5	10	pF	$F_{S\_CLK} = T_F$ Min (1, 2)
C_{IDSEL}	IDSEL Ball Capacitance		8	pF	(1,2)
L_{PIN}	Ball Inductance		25	nH	(1,2)

NOTES:

1. As required by the *PCI Local Bus Specification*, Revision 2.2.
2. Not tested.
3. Processor signals include **RALE**, **RCE[1:0]#**, **ROE#**, **RWE#**, **XINT[5:4]#**, **NMI#**, **FAIL#**, **TDI**, **TDO**, **TMS**, **TRST#**, **SDA**, and **SCL**.
4. SDRAM signals include **SA[11:0]**, **SBA[1:0]**, **SCAS#**, **SCE[1:0]#**, **SCKE[1:0]**, **SDQM[7:0]**, **SRAS#**, **SWE#**, **DCLKIN**, **DCLKOUT**, **DQ[63:0]**, and **SCB[7:0]**.
5. 3.3 V PCI signalling only supported on C-x steppings on the 80960RN processor
6. Guaranteed by characterization

Table 22. I_{CC} Characteristics

Symbol	Parameter	Typ	Max	Units	Notes
I_{LI1}	Input Leakage Current for each signal except **TMS**, **TRST#**, **TDI**, **ONCE#**, RAD[8:0] and **LCDINIT#**.		± 5	µA	$0 \le V_{IN} \le V_{CC}$
I_{LI2}	Input Leakage Current for **TMS**, **TRST#**, **TDI**, **ONCE#**, RAD[8:0] and **LCDINIT#**.	-140	-250	µA	$V_{IN} = 0.45$ V (1)
I_{LO}	Output Leakage Current		± 5	µA	$0.4 \le V_{OUT} \le V_{CC}$
I_{CC} Active (Power Supply)	Power Supply Current		1.65	A	(1,2)
I_{CC} Active (Thermal)	Thermal Current	1.2		A	(1,3)
I_{CC} Active (Power Modes)	Reset Mode ONCE Mode		0.95 0.02	A	(4) (4)

NOTES:

1. Measured with device operating and outputs loaded to the test condition in Figure 13.
2. I_{CC} Active (Power Supply) value is provided for selecting your system's power supply. It is measured using one of the worst case instruction mixes with V_{CC} = 3.6 V and ambient temperature = 55°C.
3. I_{CC} Active (Thermal) value is provided for your system's thermal management. Typical I_{CC} is measured with V_{CC} = 3.3 V and ambient temperature = 55°C.
4. I_{CC} Test (Power modes) refers to the I_{CC} values that are tested when the device is in Reset mode or ONCE mode with V_{CC} = 3.6 V and ambient temperature = 55°C.

4.5 Targeted AC Specifications

4.5.1 Clock Signal Timings

Table 23. Input Clock Timings

Symbol	Parameter	Min	Max	Units	Notes
T_F	**P_CLK** Frequency	16	33.33	MHz	
T_C	**P_CLK** Period	30	62.5	ns	(1)
T_{CS}	**P_CLK** Period Stability		±250	ps	Adjacent Clocks (2)
TCH	**P_CLK** High Time	12		ns	Measured at 1.5 V (2)
T_{CL}	**P_CLK** Low Time	12		ns	Measured at 1.5 V (2)
T_{CR}	**P_CLK** Rise Time	1	4	V/ns	0.4 V to 2.4 V (2)
T_{CF}	**P_CLK** Fall Time	1	4	V/ns	2.4 V to 0.4 V (2)
T_{DICS}	**DCLKIN** Period Stability		±250	ps	Adjacent Clocks (2)
T_{DICH}	**DCLKIN** High Time	5		ns	Measured at 1.5 V (2)
T_{DICL}	**DCLKIN** Low Time	5		ns	Measured at 1.5 V (2)

NOTES:

1. See Figure 8 “P_CLK, TCK, DCLKIN, DCLKOUT Waveform” on page 51.
2. Not tested.

Table 24. SDRAM Output Clock Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{DOF}	**DCLKOUT** Frequency	$2T_F$		MHz	
T_{DOC}	**DCLKOUT** Period	$T_C / 2$		ns	(1)
T_{DOCS}	**DCLKOUT** Period Stability		±250	ps	Adjacent Clocks
TDOCH	**DCLKOUT** High Time	5		ns	Measured at 1.5 V
T_{DOCL}	**DCLKOUT** Low Time	5		ns	Measured at 1.5 V

NOTE:

1. See Figure 8 “P_CLK, TCK, DCLKIN, DCLKOUT Waveform” on page 51.

4.5.2 PCI Interface Signal Timings

Table 25. PCI Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{OV1}	Output Valid Delay from **P_CLK** - PCI Signals Except **P_REQ#**, **P_INT[A:D]#**, and **S_GNT[5:0]#**	2	11	ns	(1,2)
T_{OV2}	Output Valid Delay from **P_CLK** - **P_INT[A:D]#**	0	25	ns	(1,2,6)
T_{OV3}	Output Valid Delay from **P_CLK** - **S_REQ64#**	0		ns	(1,2,8)
T_{OV4}	Output Valid Delay from **P_CLK** - **P_REQ#** and **S_GNT[5:0]#**	2	12	ns	(1,2)
T_{OF}	Output Float Delay from **P_CLK**		28	ns	(1,4,5,6)
T_{IS1}	Input Setup to **P_CLK** - PCI Signals Except **P_GNT#** and **S_REQ[5:0]#**	7		ns	(1,3)
T_{IS2}	Input Setup to **P_CLK** - **P_GNT#**	10		ns	(1,3)
T_{IS3}	Input Setup to **P_CLK** - **S_REQ[5:0]#**	12		ns	(1,3)
T_{IH1}	Input Hold from **P_CLK** - PCI Signals	0		ns	(1,3)
T_{IS4}	Input Setup to **P_CLK** - **S_INT[A:D]#**	25		ns	(1,3,7,9)
T_{IH2}	Input Hold to **P_CLK** - **S_INT[A:D]#**	2		ns	(1,3,7,9)
T_{IS5}	Input Setup to **P_CLK** - **P_RST#**	6		ns	(1,3,7)
T_{IH3}	Input Hold to **P_CLK** - **P_RST#**	2		ns	(1,3,7)
T_{IS6}	Input Setup to **P_RST#** - **P_REQ64#**	$10T_c$		ns	(1,3)
T_{IH4}	Input Hold to **P_RST#** - **P_REQ64#**	0	50	ns	(1,3)

NOTES:

1. The *PCI Local Bus Specification*, Revision 2.2 requires that all of the PCI signal AC timings use 0 pF for minimum timings and 50 pF for maximum timings.
2. See Figure 9 “T_{OV} Output Delay Waveform” on page 51.
3. See Figure 11 “T_{IS} and T_{IH} Input Setup and Hold Waveform” on page 52.
4. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested. See Figure 10 “T_{OF} Output Float Waveform” on page 52.
5. See Figure 10 “T_{OF} Output Float Waveform” on page 52.
6. Outputs precharged to V_{CC5}.
7. **P_RST#**, **S_INT[A:D]#** may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge.
8. **S_REQ64#** is asserted asynchronously with respect to **P_RST#**. **S_REQ64#** is deasserted one **P_CLK** after the deassertion of **S_RST#**.
9. **S_INT[A:D]#** must be asserted for a minimum of two **P_CLK** periods to guarantee recognition.

4.5.3 Intel® 80960JN Core Interface Timings

Table 26. Intel® 80960JN Core Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{OV5}	Output Valid Delay from **P_CLK** - **FAIL#**	2	TBD	ns	(1,5)
T_{IS7}	Input Setup to **P_CLK** - **NMI#**, **XINT[5:4]#**	25		ns	(2,3)
T_{IH5}	Input Hold from **P_CLK** - **NMI#**, **XINT[5:4]#**	2		ns	(2,3)

NOTES:

1. See Figure 9 “T_{OV} Output Delay Waveform” on page 51.
2. See Figure 11 “T_{IS} and T_{IH} Input Setup and Hold Waveform” on page 52.
3. Setup and hold times must be met for proper processor operation. **NMI#** and **XINT[5:4]#** may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge. For asynchronous operation, **NMI#** and **XINT[5:4]#** must be asserted for a minimum of two **P_CLK** periods to guarantee recognition.
4. Core signals include: **XINT[5:4]#**, **NMI#**, **FAIL#** .
5. The processor asserts **FAIL#** during built-in self-test. If self-test passes, **FAIL#** is deasserted. The processor asserts **FAIL#** during the bus confidence test. If the test passes, **FAIL#** is deasserted and user program execution begins.

4.5.4 SDRAM/Flash Interface Signal Timings

Table 27. SDRAM / Flash Signal Timings

Sym	Parameter	Min	Max	Units	Notes
T_{OV6}	Output Valid Delay from **DCLKIN** - **SA[11:0]**, **SBA[1:0]**, **SCAS#**, **SRAS#**, and **SWE#**.	1.62	6.60	ns	(1,5)
T_{OV7}	Output Valid Delay from **DCLKIN** - **DQ[63:0]**, and **SCB[7:0]**.	2.03	7.14	ns	(1,5)
T_{OV8}	Output Valid Delay from **DCLKIN** - **SDQM[7:0]**	2.57	6.85	ns	(1,5)
T_{OV9}	Output Valid Delay from **DCLKIN** - **SCKE[1:0]**	1.74	5.50	ns	(1,5)
T_{OV10}	Output Valid Delay from **DCLKIN** - **SCE[1:0]#**	1.65	5.25	ns	(1,5)
T_{IS8}	Input Setup to **DCLKIN** - **DQ[63:0]**, and **SCB[7:0]**	3.00		ns	(2)
T_{IH6}	Input Hold from **DCLKIN** - **DQ[63:0]**, and **SCB[7:0]**	1.5		ns	(2)
T_{OV11}	Output Valid Delay from **DCLKIN** - RAD[16:0], **RALE**, **RCE[1:0]#**, **ROE#**, and **RWE#**.	1.4	11.0	ns	(1,5)
T_{IS9}	Input Setup to **DCLKIN** - RAD[16:0]	5		ns	(2)
T_{IH7}	Input Hold from **DCLKIN** - RAD[16:0]	1.4		ns	(2)

NOTES:

1. See Figure 9 “T_{OV} Output Delay Waveform” on page 51.
2. See Figure 11 “T_{IS} and T_{IH} Input Setup and Hold Waveform” on page 52.
3. SDRAM signals include **SA[11:0]**, **SBA[1:0]**, **SCAS#**, **SCE[1:0]#**, **SCKE[1:0]**, **SDQM[7:0]**, **SRAS#**, **SWE#**, **DQ[63:0]**, and **SCB[7:0]**. Timings are for 3.3 V signalling environment.
4. Flash signals include RAD[16:0], **RALE**, **RCE[1:0]#**, **ROE#**, and **RWE#**. Timings are for 5V signalling environment.
5. These output valid times are specified with a 0 pF loading.

4.5.5 Boundary Scan Test Signal Timings

Table 28. Boundary Scan Test Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{BSF}	**TCK** Frequency	0	$0.5T_F$	MHz	
T_{BSCH}	**TCK** High Time	15		ns	Measured at 1.5 V (1)
T_{BSCL}	**TCK** Low Time	15		ns	Measured at 1.5 V (1)
T_{BSCR}	**TCK** Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{BSCF}	**TCK** Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to **TCK** — **TDI**, **TMS**	4		ns	(4)
T_{BSIH1}	Input Hold from **TCK** — **TDI**, **TMS**	6		ns	(4)
T_{BSIS2}	Input Setup to **TCK** — **TRST#**	25		ns	(4)
T_{BSIH2}	Input Hold from **TCK** — **TRST#**	3		ns	(4)
T_{BSOV1}	**TDO** Valid Delay	3	30	ns	Relative to falling edge of **TCK** (2,3)
T_{OF1}	**TDO** Float Delay	3	30	ns	Relative to falling edge of **TCK** (2,5)
T_{OV12}	All Outputs (Non-Test) Valid Delay	3	30	ns	Relative to falling edge of **TCK** (2,3)
T_{OF2}	All Outputs (Non-Test) Float Delay	3	30	ns	Relative to falling edge of **TCK** (2,5)
T_{IS10}	Input Setup to **TCK** — All Inputs (Non-Test)	4		ns	(4)
T_{IH8}	Input Hold from **TCK** — All Inputs (Non-Test)	6		ns	(4)

NOTES:

1. Not tested.
2. Outputs precharged to V_{CC5}.
3. See Figure 9 “T_{OV} Output Delay Waveform” on page 51.
4. See Figure 11 “T_{IS} and T_{IH} Input Setup and Hold Waveform” on page 52.
5. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested. See Figure 10 “T_{OF} Output Float Waveform” on page 52.

4.5.6 I²C Interface Signal Timings

Table 29. I²C Interface Signal Timings

Symbol	Parameter	Std. Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCL}	**SCL** Clock Frequency	0	100	0	400	KHz	
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7		1.3		µs	(1)
T_{HDSTA}	Hold Time (repeated) START Condition	4		0.6		µs	(1,3)
T_{LOW}	**SCL** Clock Low Time	4.7		1.3		µs	(1,2)
T_{HIGH}	**SCL** Clock High Time	4		0.6		µs	(1,2)
T_{SUSTA}	Setup Time for a Repeated START Condition	4.7		0.6		µs	(1)
T_{HDDAT}	Data Hold Time	0		0	0.9	µs	(1)
T_{SUDAT}	Data Setup Time	250		100		ns	(1)
T_{SR}	**SCL** and **SDA** Rise Time		1000	$20+0.1C_b$	300	ns	(1,4)
T_{SF}	**SCL** and **SDA** Fall Time		300	$20+0.1C_b$	300	ns	(1,4)
T_{SUSTO}	Setup Time for STOP Condition	4		0.6		µs	(1)

NOTES:

1. See Figure 12 “I²C Interface Signal Timings” on page 52.
2. Not tested.
3. After this period, the first clock pulse is generated.
4. C_b = the total capacitance of one bus line, in pF.

4.6 AC Timing Waveforms

Figure 8. P_CLK, TCK, DCLKIN, DCLKOUT Waveform

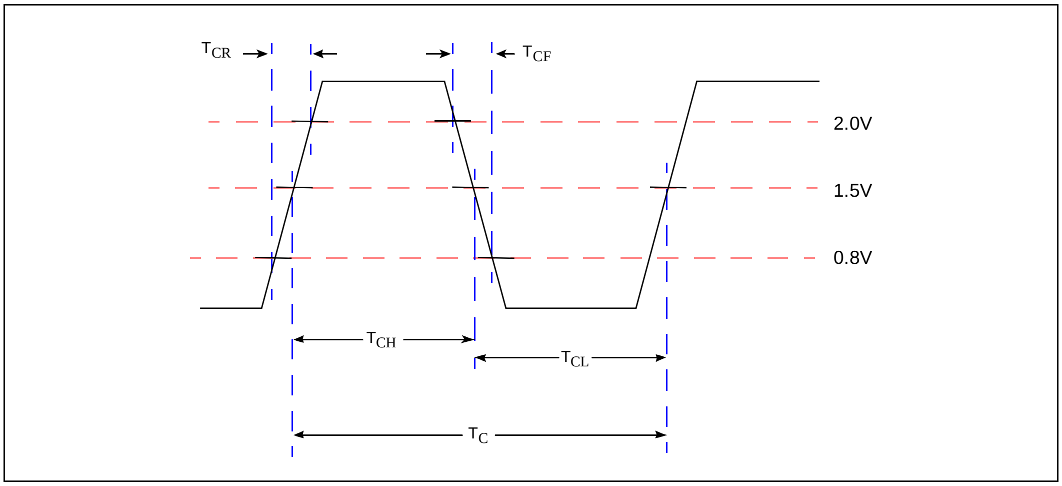


Figure 9. T_{OV} Output Delay Waveform

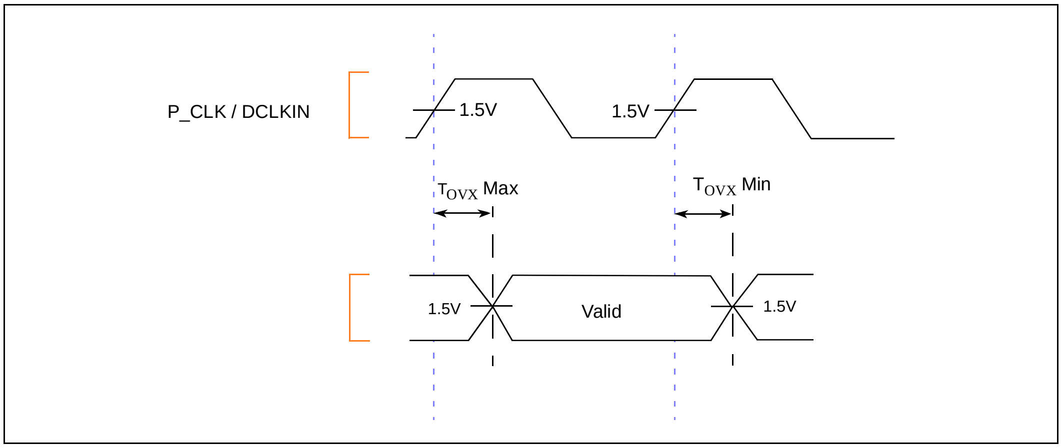


Figure 10. T_{OF} Output Float Waveform

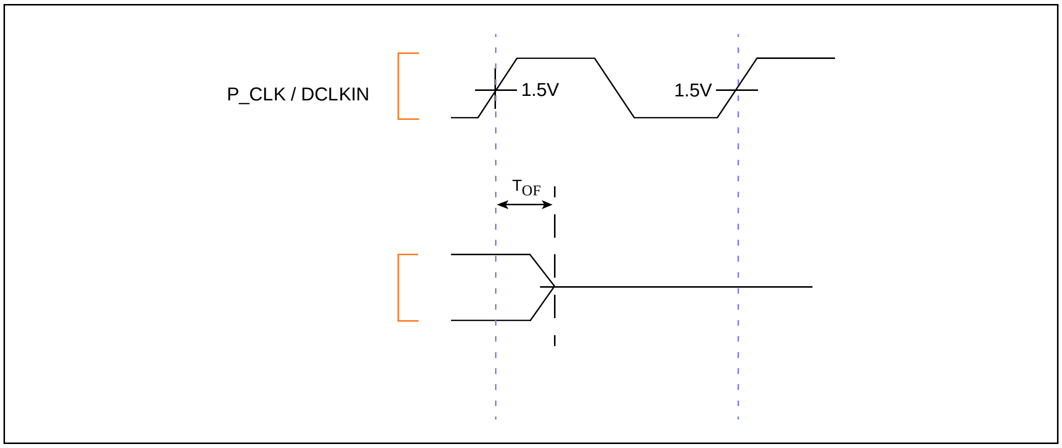


Figure 11. T_{IS} and T_{IH} Input Setup and Hold Waveform

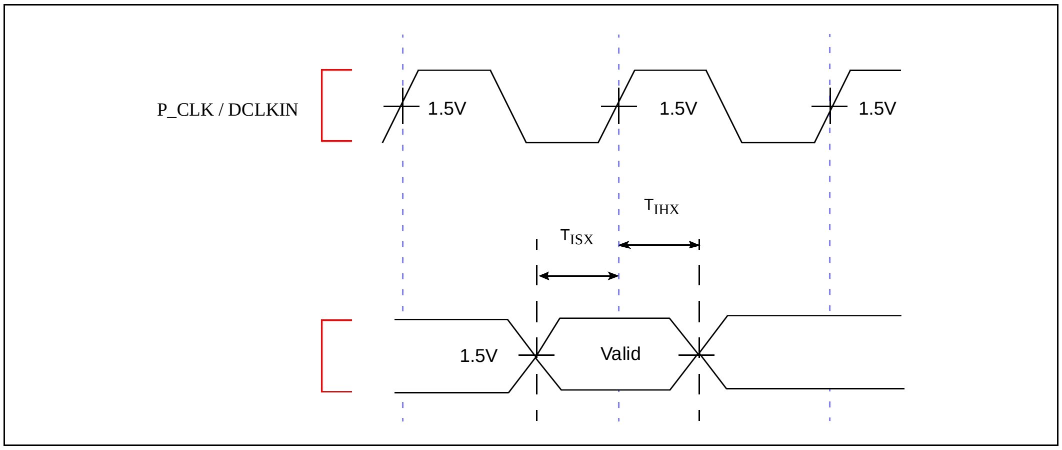
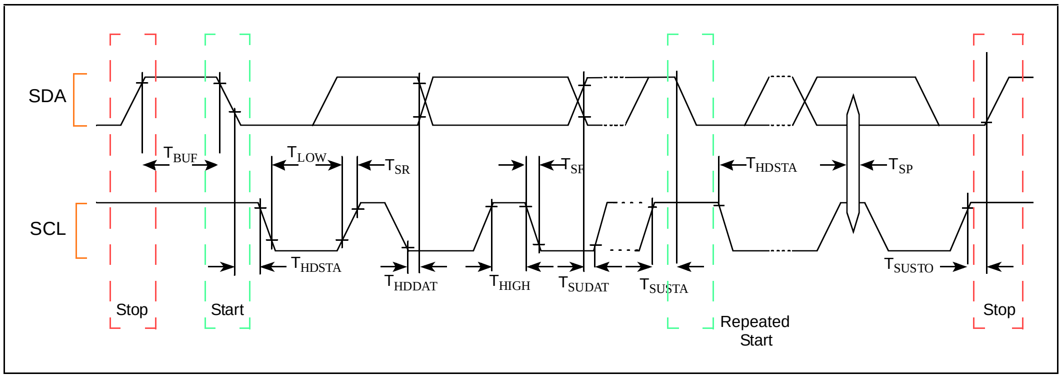


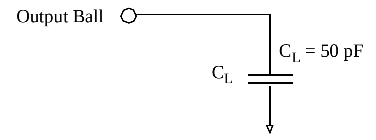
Figure 12. I^2C Interface Signal Timings



4.7 AC Test Conditions

The AC specifications in Section 4.5, “Targeted AC Specifications” on page 46 are tested with a 50 pF load indicated in Figure 13.

Figure 13. AC Test Load (all signals except SDRAM and Flash signals)



The PCI maximum AC specifications are tested with the 50 pF load indicated in Figure 13. The PCI minimum AC specifications are tested with a 0 pF load. All of the SDRAM and Flash timings are specified for a 0 pF load.

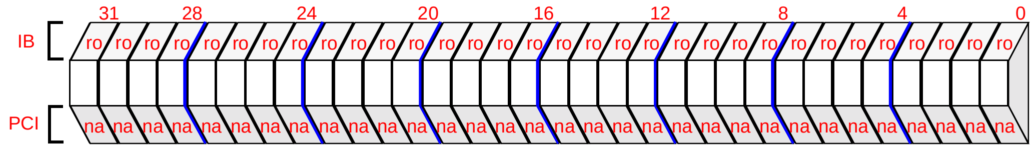
5.0 Device Identification on Reset

During the manufacturing process, values characterizing the i960 RM/RN I/O processor type and stepping are programmed into memory-mapped registers. The i960 RM/RN I/O processor contains two, read-only device ID MMRs. One holds the Processor Device ID (PDIDR MMR Location - 0000 1710H) and the other holds the i960 Core Processor Device ID (DEVICEID MMR Location - FF00 8710H). During initialization, the DEVICEID is placed in g0.

The device identification values are compliant with the IEEE 1149.1 specification and Intel standards. Table 30 describes the fields of the two Device IDs.

Note: The value programmed into these registers varies with stepping. Refer to the Specification Update for the correct value.

Table 30. Device ID Registers



IB:	0000 1710H FF00 8710H	**Legend:**NA = Not AccessibleRO = Read Only RV = ReservedPR = PreservedRW = Read/Write RS = Read/SetRC = Read Clear IB = Internal Bus AddressPCI = PCI Configuration Address Offset
PCI:	NA	

Bit	Default	Description
31:28	X	Version - Indicates stepping changes.
27	X	V_{CC} - Indicates device voltage type. 0 = 5.0 V 1 = 3.3 V
26:21	X	Product Type - Indicates the generation or “family member”.
20:17	X	Generation Type - Indicates the generation of the device.
16:12	X	Model Type - Indicates member within a series and specific model information.
11:01	X	Manufacturer ID - Indicates manufacturer ID assigned by IEEE. 0000 0001 001 = Intel Corporation
0	1	Constant