

74LVC74A

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 7 — 20 November 2012

Product data sheet

1. General description

The 74LVC74A is a dual edge triggered D-type flip-flop with individual data (nD) inputs, clock (nCP) inputs, set ($n\bar{S}D$) and ($n\bar{R}D$) inputs, and complementary nQ and $n\bar{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse. The nD inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

2. Features and benefits

- 5 V tolerant inputs for interlacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40°C to $+85^{\circ}\text{C}$ and -40°C to $+125^{\circ}\text{C}$



3. Ordering information

Table 1. Ordering information

Type number	Package	Temperature range	Name	Description	Version
74LVC74AD		−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC74ADB		−40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC74APW		−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC74ABQ		−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

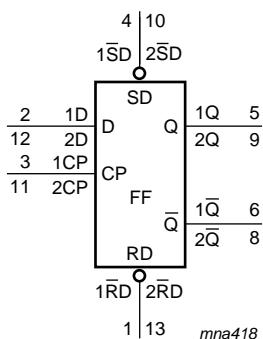


Fig 1. Logic symbol

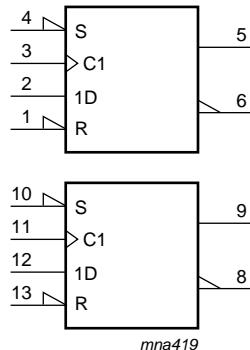


Fig 2. IEC logic symbol

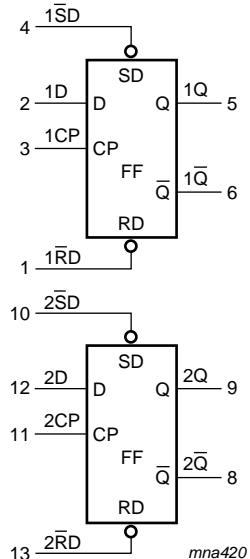


Fig 3. Functional diagram

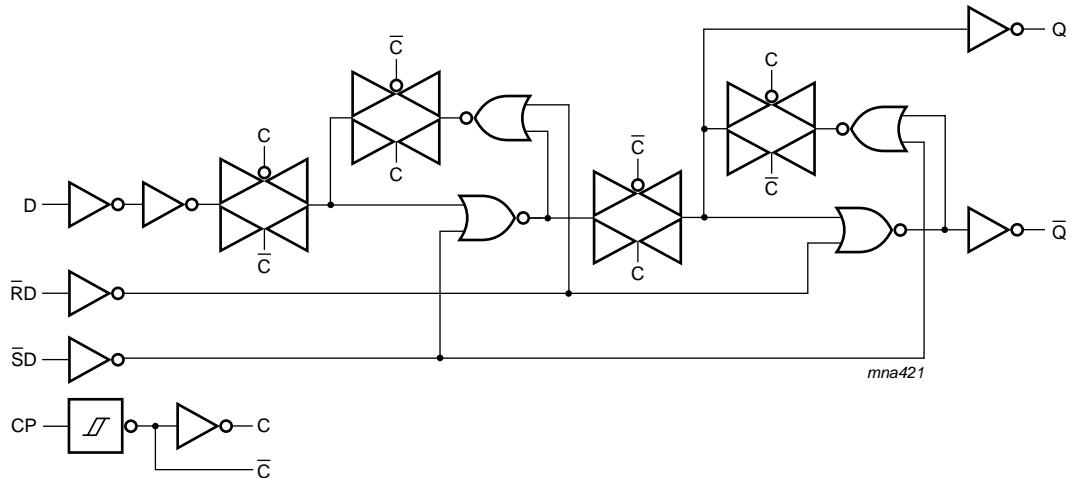


Fig 4. Logic diagram for one flip-flop

5. Pinning information

5.1 Pinning

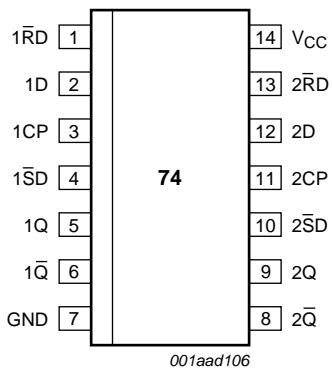


Fig 5. Pin configuration for SO14 and (T)SSOP14

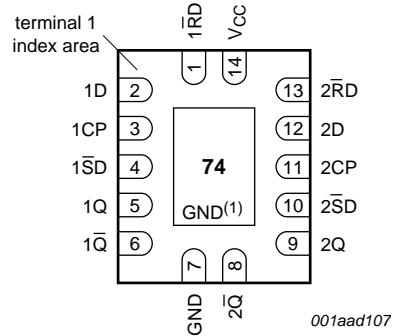


Fig 6. Pin configuration for DHVQFN14

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1RD	1	asynchronous reset-direct input (active LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH, edge-triggered)
1SD	4	asynchronous set-direct input (active LOW)
1Q	5	true output
1Q̄	6	complement output
GND	7	ground (0 V)
2Q̄	8	complement output
2Q	9	true output
2SD	10	asynchronous set-direct input (active LOW)
2CP	11	clock input (LOW-to-HIGH, edge-triggered)
2D	12	data input
2RD	13	asynchronous reset-direct input (active LOW)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input				Output	
nSD	nRD	nCP	nD	nQ	nQ̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care

Table 4. Function table^[1]

Input				Output	
nSD	nRD	nCP	nD	nQ _{n+1}	nQ̄ _{n+1}
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level
L = LOW voltage level
↑ = LOW-to-HIGH transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition
X = don't care

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0 \text{ V}$	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0 \text{ V}$	-	± 50	mA
V_O	output voltage		[2] -0.5	$V_{CC} + 0.5$	V
I_O	output current	$V_O = 0 \text{ V}$ to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{STG}	storage temperature		-65	+150	°C
P_{TOT}	total power dissipation	$T_{AMB} = -40 \text{ }^{\circ}\text{C}$ to $+125 \text{ }^{\circ}\text{C}$	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C the value of P_{TOT} derates linearly with 8 mW/K.

For (T)SSOP14 packages: above 60 °C the value of P_{TOT} derates linearly with 5.5 mW/K.

For DHVQFN14 packages: above 60 °C the value of P_{TOT} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	1.65	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{AMB}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V}$ to 2.7 V	0	-	20	ns/V
		$V_{CC} = 2.7 \text{ V}$ to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
I _I	input leakage current	I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
		V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	4.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	nCP to nQ, n \bar{Q} ; see Figure 7	[2]					
		$V_{CC} = 1.2$ V	-	15	-	-	-	ns
		$V_{CC} = 1.65$ V to 1.95 V	1.0	5.0	10.3	1.0	11.9	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.8	2.9	5.8	1.8	6.7	ns
		$V_{CC} = 2.7$ V	1.0	2.7	6.0	1.0	7.5	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.0	2.6	5.2	1.0	6.5	ns
		n $\bar{S}D$ to nQ, n \bar{Q} ; see Figure 8						
		$V_{CC} = 1.2$ V	-	15	-	-	-	ns
		$V_{CC} = 1.65$ V to 1.95 V	0.5	4.0	10.6	0.5	12.2	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.0	2.4	6.1	1.0	7.1	ns
		$V_{CC} = 2.7$ V	1.0	2.9	6.4	1.0	8.0	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.0	2.2	5.4	1.0	7.0	ns
		n $\bar{R}D$ to nQ, n \bar{Q} ; see Figure 8						
		$V_{CC} = 1.2$ V	-	15	-	-	-	ns
		$V_{CC} = 1.65$ V to 1.95 V	0.5	4.1	10.7	0.5	12.4	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.0	2.4	6.1	1.0	7.1	ns
		$V_{CC} = 2.7$ V	1.0	3.0	6.4	1.0	8.0	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.0	2.2	5.4	1.0	7.0	ns
t_w	pulse width	clock HIGH or LOW; see Figure 7						
		$V_{CC} = 1.65$ V to 1.95 V	5.0	-	-	5.0	-	ns
		$V_{CC} = 2.3$ V to 2.7 V	4.0	-	-	4.0	-	ns
		$V_{CC} = 2.7$ V	3.3	-	-	4.5	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	3.3	1.3	-	4.5	-	ns
		set or reset LOW; see Figure 8						
		$V_{CC} = 1.65$ V to 1.95 V	5.0	-	-	5.0	-	ns
		$V_{CC} = 2.3$ V to 2.7 V	4.0	-	-	4.0	-	ns
		$V_{CC} = 2.7$ V	3.3	-	-	4.5	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	3.3	1.7	-	4.5	-	ns
t_{rec}	recovery time	set or reset; see Figure 8						
		$V_{CC} = 1.65$ V to 1.95 V	1.5	-	-	1.5	-	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.5	-	-	1.5	-	ns
		$V_{CC} = 2.7$ V	1.5	-	-	1.0	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	+1.0	-3.0	-	1.0	-	ns

Table 8. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{su}	set-up time	nD to nCP; see Figure 7						
		V _{CC} = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns
		V _{CC} = 2.7 V	2.2	-	-	2.2	-	ns
t _h	hold time	V _{CC} = 3.0 V to 3.6 V	2.0	0.8	-	2.0	-	ns
		nD to nCP; see Figure 7						
		V _{CC} = 1.65 V to 1.95 V	2.0	-	-	2.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	-	-	1.5	-	ns
f _{max}	maximum frequency	V _{CC} = 2.7 V	1.0	-	-	1.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	+1.0	-0.2	-	1.0	-	ns
		nCP; see Figure 7						
		V _{CC} = 1.65 V to 1.95 V	100	-	-	80	-	MHz
t _{sk(o)}	output skew time	V _{CC} = 2.3 V to 2.7 V	125	-	-	100	-	MHz
		V _{CC} = 2.7 V	150	-	-	120	-	MHz
		V _{CC} = 3.0 V to 3.6 V	150	250	-	120	-	MHz
		V _{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5 ns
C _{PD}	power dissipation capacitance	per flip-flop; V _I = GND to V _{CC}	[4]					
		V _{CC} = 1.65 V to 1.95 V	-	12.4	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	16.0	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	19.1	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

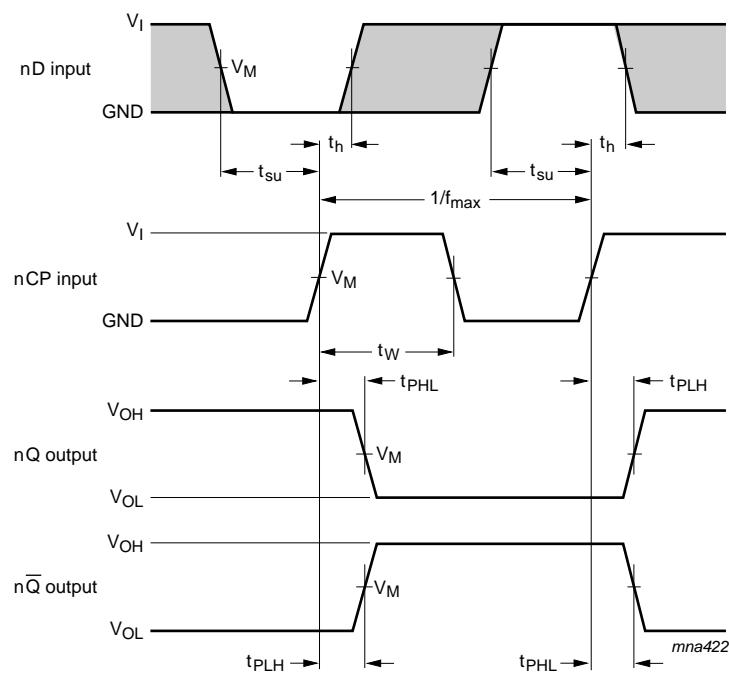
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$$

f_i = input frequency in MHz; f_o = output frequency in MHzC_L = output load capacitance in pFV_{CC} = supply voltage in Volts

N = number of inputs switching

$$\sum(C_L \times V_{CC}^2 \times f_o) = \text{sum of the outputs}$$

11. AC waveforms

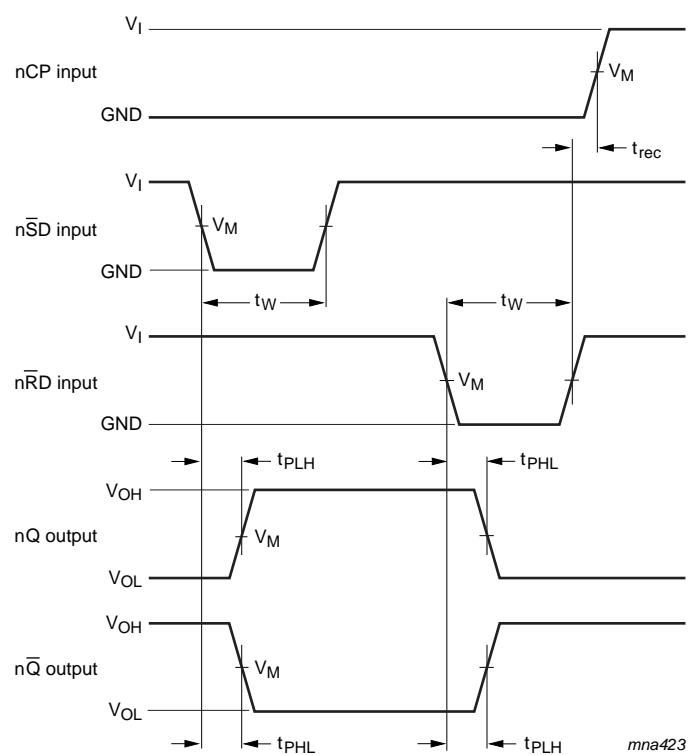


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The clock input (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, and the maximum frequency



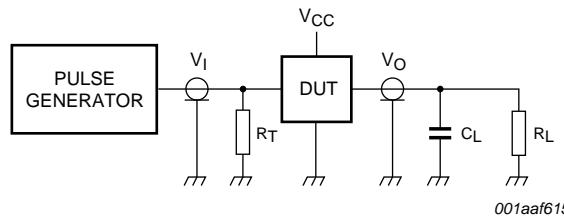
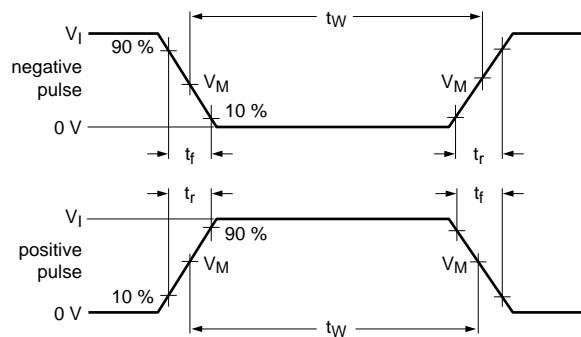
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The set ($n\bar{S}D$) and reset ($n\bar{R}D$) input to output (nQ , $n\bar{Q}$) propagation delays, the set and reset pulse widths, and the nRD to nCP recovery time

Table 9. Measurement points

Supply voltage	Input	Output	
V_{CC}	V_I	V_M	V_M
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 9. Load circuitry for switching times

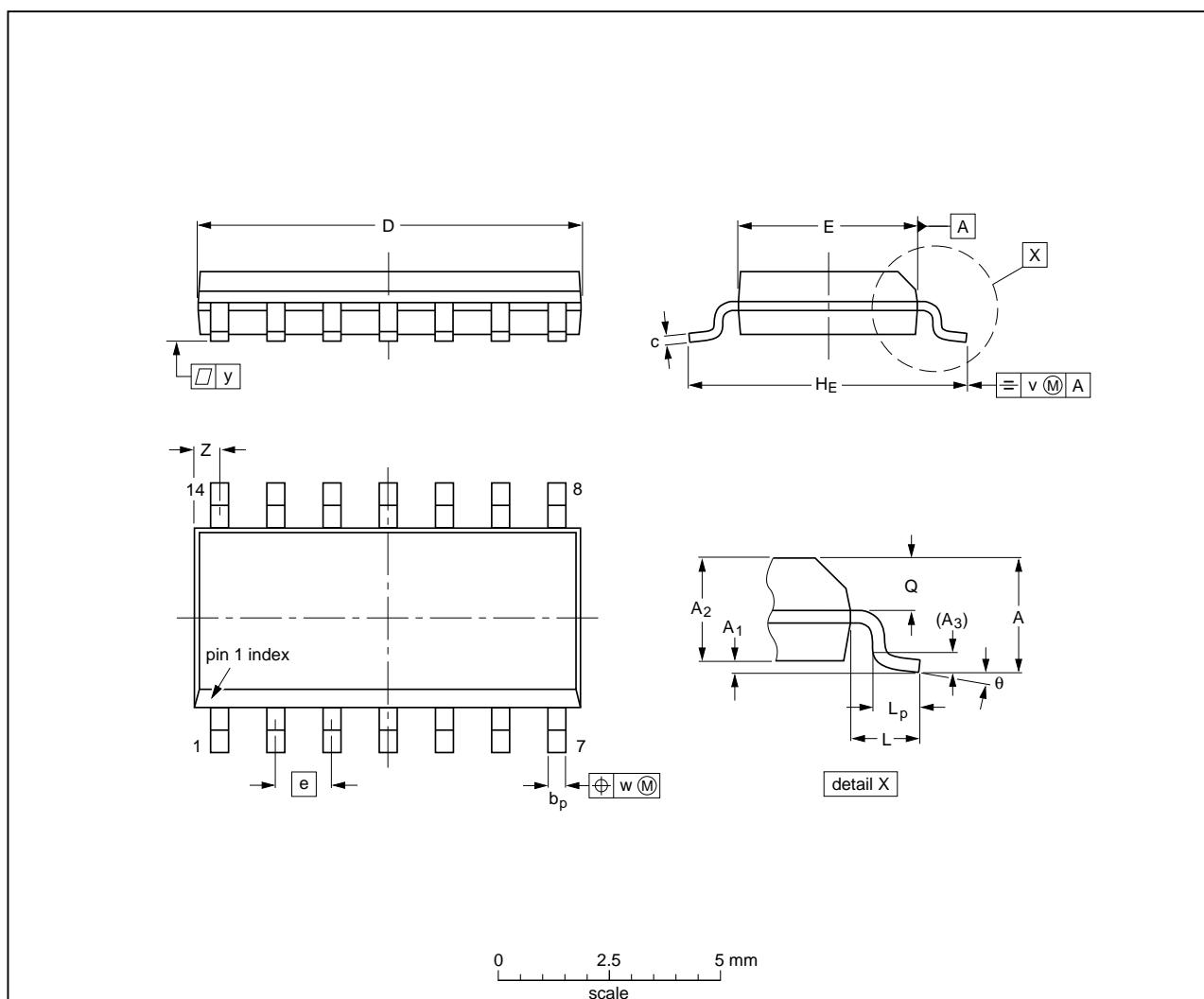
Table 10. Test data

Supply voltage	Input	Load	V_{EXT}				
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75 0.10	0.25 1.45 1.25	0.25	0.25 0.36	0.49 0.19	0.25 8.55	8.75 4.0	3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.057 0.049	0.01	0.019 0.0100	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041 0.016	0.039 0.024	0.028 0.024	0.01 0.01	0.004	0.028 0.012			

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

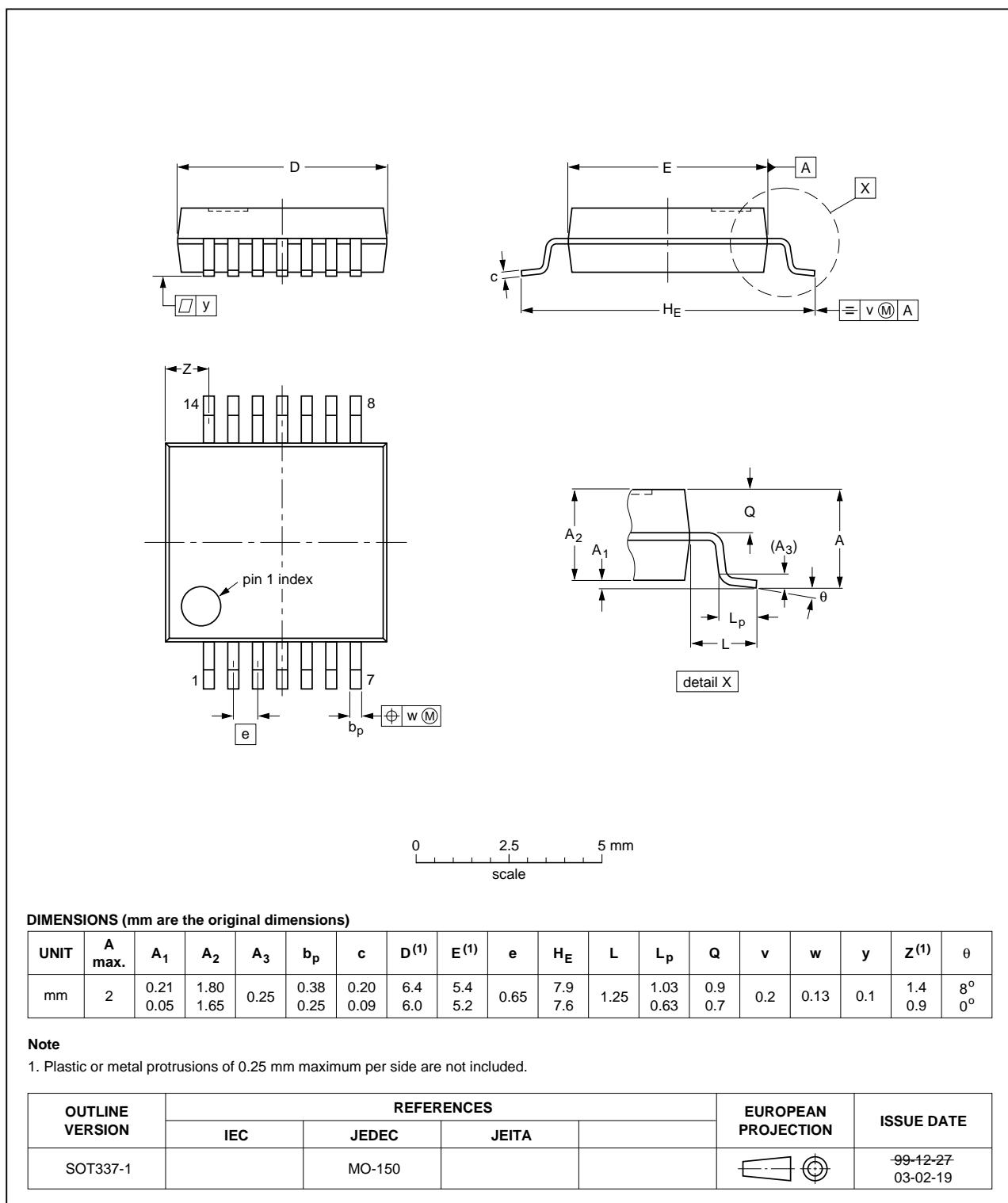
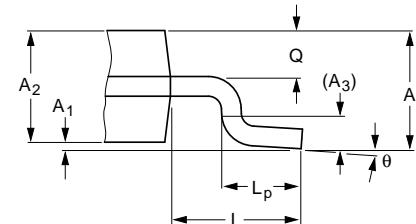
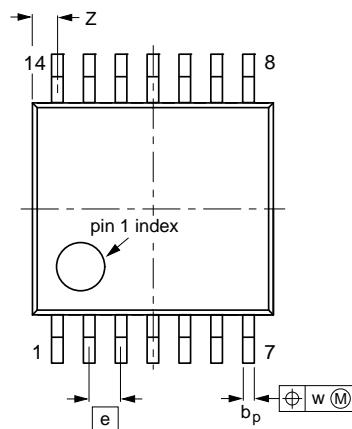
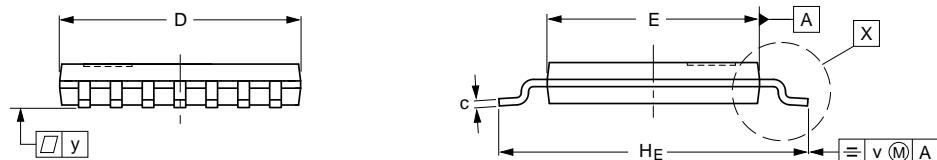


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1 0.05	0.15 0.80	0.95 0.25	0.25 0.19	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT402-1		MO-153			-99-12-27 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

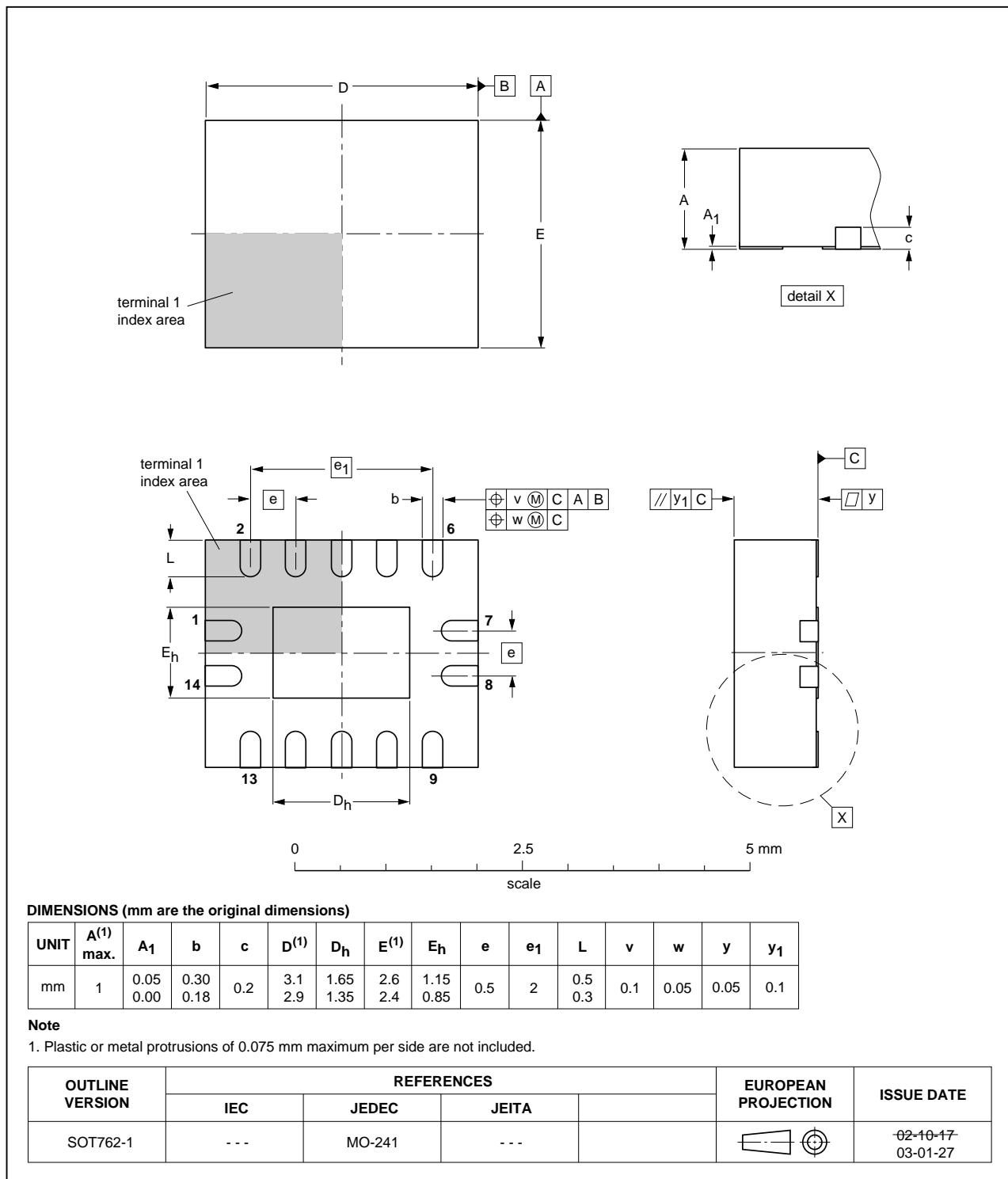


Fig 13. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC74A v.7	20121120	Product data sheet	-	74LVC74A v.6
Modifications:		• Table 6 , Table 7 , Table 8 , Table 9 and Table 10 : values added for lower voltage ranges.		
74LVC74A v.6	20070604	Product data sheet	-	74LVC74A v.5
74LVC74A v.5	20070525	Product data sheet	-	74LVC74A v.4
74LVC74A v.4	20030526	Product specification	-	74LVC74A v.3
74LVC74A v.3	20020618	Product specification	-	74LVC74A v.2
74LVC74A v.2	19980617	Product specification	-	74LVC74A v.1
74LVC74A v.1	19980617	Product specification	-	-

15. Legal information

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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