

Improved Quad CMOS Analog Switches

DESCRIPTION

The DG201B, DG202B analog switches are highly improved versions of the industry-standard DG201A, DG202. These devices are fabricated in Vishay Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG201B and DG202B can handle up to ± 22 V input signals, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply voltages in the off condition.

The DG201B is a normally closed switch and the DG202B is a normally open switch. (see Truth Table.)

FEATURES

- ± 22 V supply voltage rating
- TTL and CMOS compatible logic
- Low on-resistance - $R_{DS(on)}$: 45 Ω
- Low leakage - $I_{D(on)}$: 20 pA
- Single supply operation possible
- Extended temperature range
- Fast switching - t_{ON} : 120 ns
- Low glitching - Q: 1 pC
- **Compliant to RoHS Directive 2002/95/EC**



RoHS*
COMPLIANT

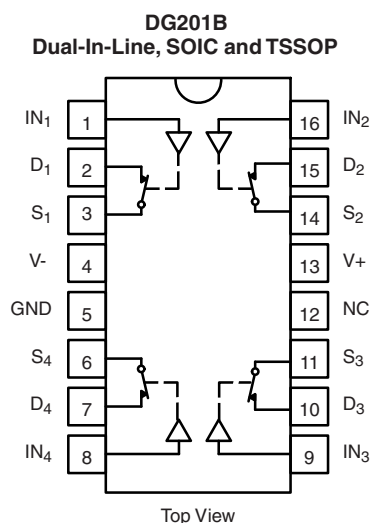
BENEFITS

- Wide analog signal range
- Simple logic interface
- Higher accuracy
- Minimum transients
- Reduced power consumption
- Superior to DG201A, DG202
- Space savings (TSSOP)

APPLICATIONS

- Industrial instrumentation
- Test equipment
- Communications systems
- Disk drives
- Computer peripherals
- Portable instruments
- Sample-and-hold circuits

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	DG201B	DG202B
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply

ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 55 °C to 125 °C	16-pin CerDIP	DG201BAK
		DG202BAK
- 40 °C to 85 °C	16-pin Plastic DIP	DG201BDJ DG201BDJ-E3
		DG202BDJ DG202BDJ-E3
	16-pin narrow SOIC	DG201BDY DG201BDY-E3 DG201BDY-T1 DG201BDY-T1-E3
		DG202BDY DG202BDY-E3 DG202BDY-T1 DG202BDY-T1-E3
	16-pin TSSOP	DG201BDQ DG201BDQ-E3 DG201BDQ-T1 DG201BDQ-T1-E3
		DG202BDQ DG202BDQ-E3 DG202BDQ-T1 DG202BDQ-T1-E3

ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Voltages Referenced, V ₊ to V ₋		44	V
GND		25	
Digital Inputs ^a , V _S , V _D		(V ₋) - 2 to (V ₊) + 2 or 30 mA, whichever occurs first	
Current (Any terminal)		30	mA
Peak Current S or D (Pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(AK, DK suffix)	- 65 to 150	°C
	(DJ, DY, DQ suffix)	- 65 to 125	
Power Dissipation (Package) ^b	16-pin plastic DIP ^c	470	mW
	16-pin narrow SOIC and TSSOP ^d	640	
	16-pin CerDIP ^e	900	
	LCC-20 ^f	750	

Notes:

- Signals on S_X, D_X, or IN_X exceeding V₊ or V₋ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC board.
- Derate 6.5 mW/°C above 75 °C.
- Derate 7.6 mW/°C above 75 °C.
- Derate 12 mW/°C above 75 °C.
- Derate 10 mW/°C above 75 °C.

The schematic diagram illustrates a 5V level shifter circuit. It features a 5V regulator (5V Reg) connected to a 5V input buffer. The input buffer's output is connected to a level shifter, which is then connected to an inverter. The inverter's output is connected to a 5V output buffer, which drives the output signal DX. The circuit is powered by V+ and GND. The input signal INx is connected to the input buffer, and the output signal DX is connected to the output buffer. The level shifter and inverter are connected to the 5V supply and GND. The output buffer is connected to the 5V supply and GND. The output signal DX is connected to the output buffer. The circuit is powered by V+ and GND.

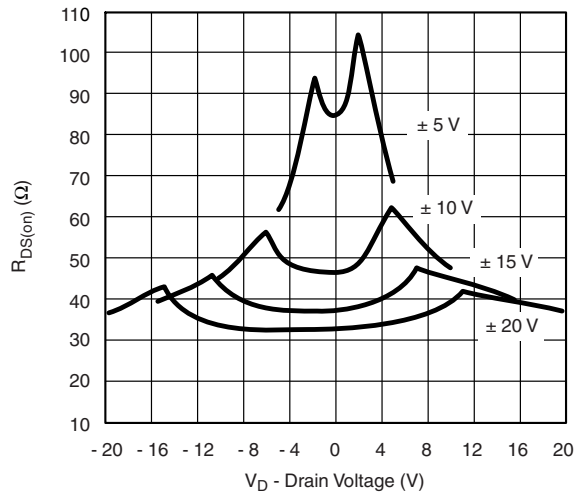
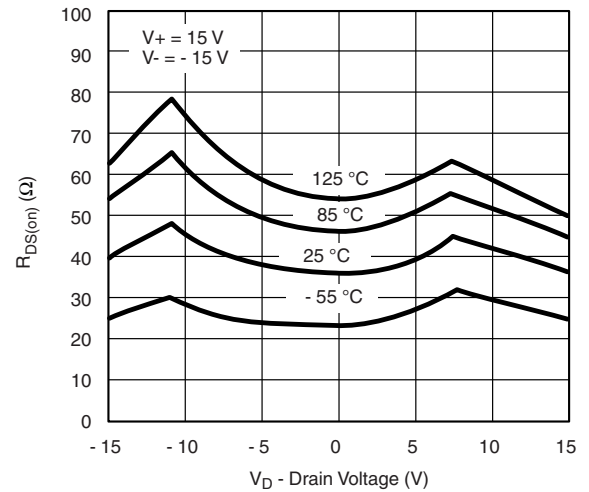
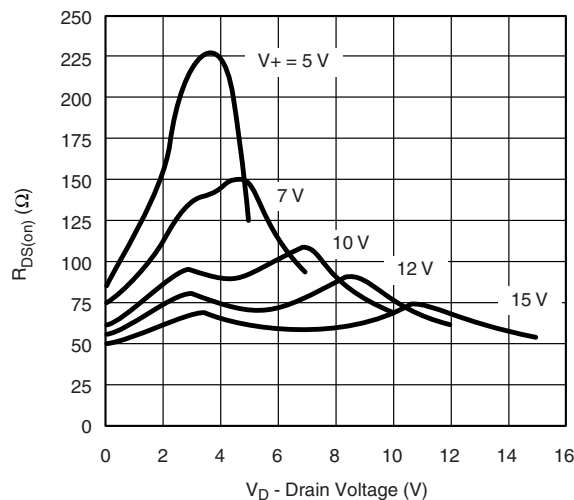
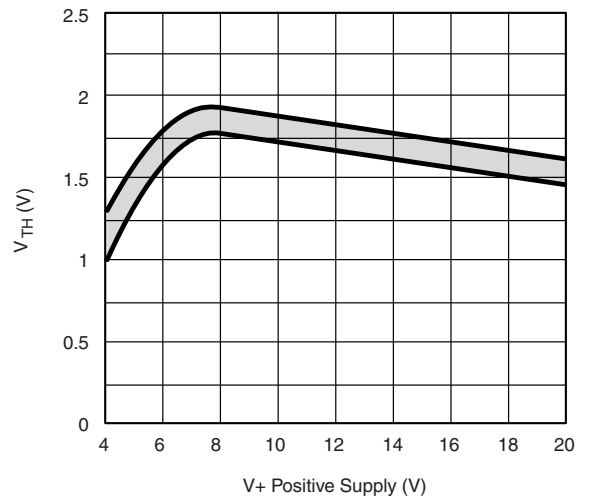
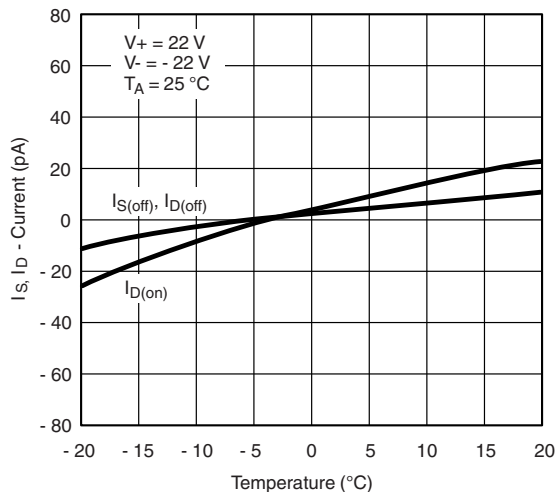
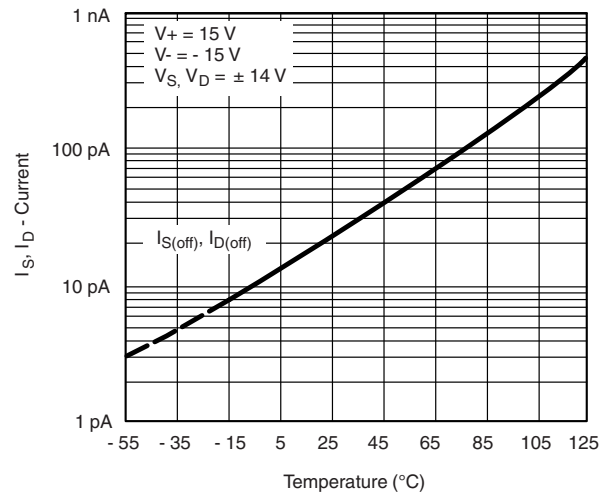
SPECIFICATIONS ^a									
Parameter	Symbol	Test Conditions Unless Specified V ₊ = 15 V, V ₋ = - 15 V V _{IN} = 2.4 V, 0.8 V ^f	Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	R _{DS(on)}	V _D = ± 10 V, I _S = 1 mA	Room Full	45		85 100		85 100	Ω
R _{DS(on)} Match	ΔR _{DS(on)}		Room	2					
Source Off Leakage Current	I _{S(off)}	V _S = ± 14 V, V _D = ± 14 V	Room Full	± 0.01	- 0.5 - 20	0.5 20	- 0.5 - 5	0.5 5	nA
Drain Off Leakage Current	I _{D(off)}	V _D = ± 14 V, V _S = ± 14 V	Room Full	± 0.01	- 0.5 - 20	0.5 20	- 0.5 - 5	0.5 5	
Drain On Leakage Current	I _{D(on)}	V _S = V _D = ± 14 V	Room Full	± 0.02	- 0.5 - 40	0.5 40	- 0.5 - 10	0.5 10	
Digital Control									
Input Voltage High	V _{INH}		Full		2.4		2.4		V
Input Voltage Low	V _{INL}		Full			0.8		0.8	
Input Current	I _{INH} or I _{INL}	V _{INH} or V _{INL}	Full		- 1	1	- 1	1	μA
Input Capacitance	C _{IN}		Room	5					pF
Dynamic Characteristics									
Turn-On Time	t _{ON}	V _S = 2 V see switching time test circuit	Room Full	120		300		300	ns
Turn-Off Time	t _{OFF}		Room Full	65		200		200	
Charge Injection	Q	C _L = 1000 pF, V _g = 0 V R _g = 0 Ω	Room	1					pC
Source-Off Capacitance	C _{S(off)}	V _S = 0 V, f = 1 MHz	Room	5					pF
Drain-Off Capacitance	C _{D(off)}		Room	5					
Channel On Capacitance	C _{D(on)}	V _D = V _S = 0 V, f = 1 MHz	Room	16					
Off Isolation	OIRR	C _L = 15 pF, R _L = 50 Ω V _S = 1 V _{RMS} , f = 100 kHz	Room	90					dB
Channel-to-Channel Crosstalk	X _{TALK}		Room	95					
Power Supply									
Positive Supply Current	I ₊	V _{IN} = 0 or 5 V	Room Full			50 100		50 100	μA
Negative Supply Current	I ₋		Room Full		- 1 - 5		- 1 - 5		
Power Supply Range for Continuous Operation	V _{OP}		Full		± 4.5	± 22	± 4.5	± 22	V

SPECIFICATIONS (for Single Supply) ^a									
Parameter	Symbol	Test Conditions Unless Specified V ₊ = 12 V, V ₋ = 0 V V _{IN} = 2.4 V, 0.8 V ^f	Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	R _{DS(on)}	V _D = 3 V, 8 V, I _S = 1 mA	Room Full	90		160 200		160 200	Ω
Dynamic Characteristics									
Turn-On Time	t _{ON}	V _S = 8 V see switching time test circuit	Room	120		300		300	ns
Turn-Off Time	t _{OFF}		Room	60		200		200	
Charge Injection	Q	C _L = 1 nF, V _{gen} = 6 V R _{gen} = 0 Ω	Room	4					pC
Power Supply									
Positive Supply Current	I ₊	V _{IN} = 0 or 5 V	Room Full			50 100		50 100	μA
Negative Supply Current	I ₋		Room Full		- 1 - 5		- 1 - 5		
Power Supply Range for Continuous Operation	V _{OP}		Full		+ 4.5	+ 25	+ 4.5	+ 25	V

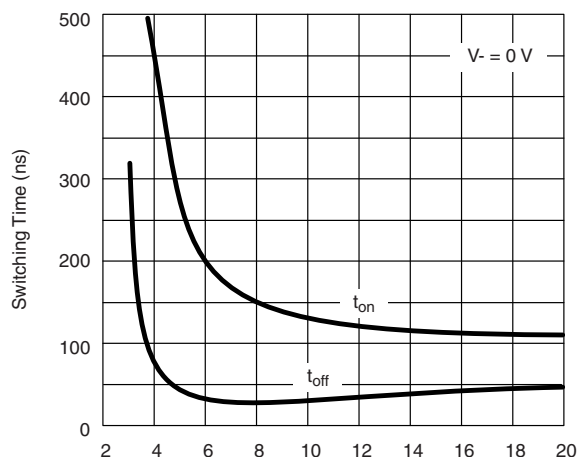
Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

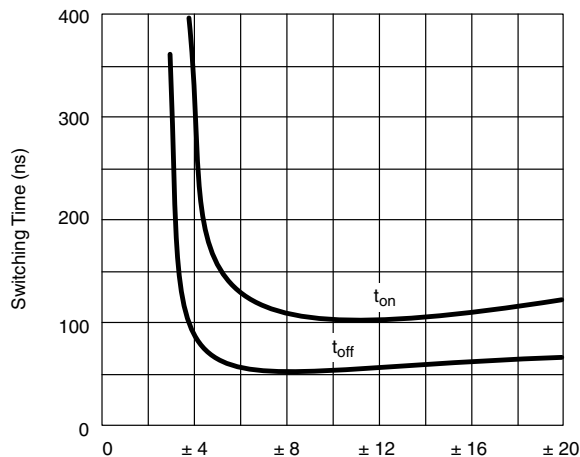
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

 $R_{DS(on)}$ vs. V_D and Power Supply Voltages

 $R_{DS(on)}$ vs. V_D and Temperature

 $R_{DS(on)}$ vs. V_D and Single Power Supply Voltages

Input Switching Threshold vs. Supply Voltage

Leakage Currents vs. Analog Voltage

Leakage Currents vs. Temperature

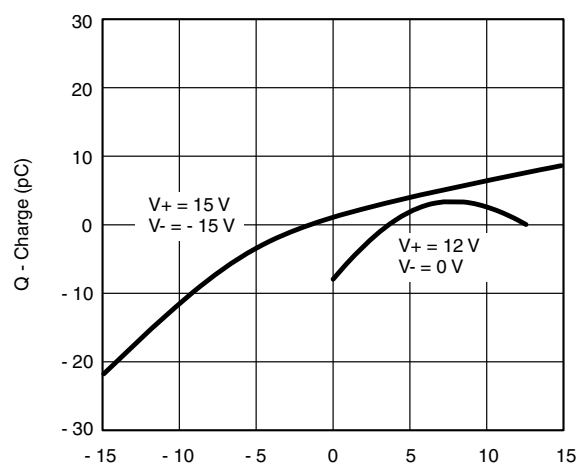
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



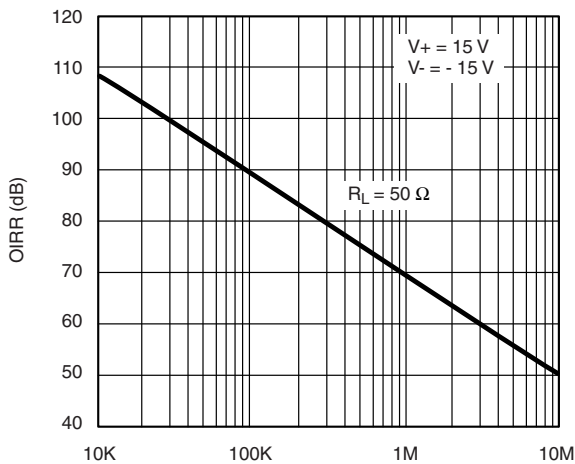
Switching Time vs. Single Supply Voltage



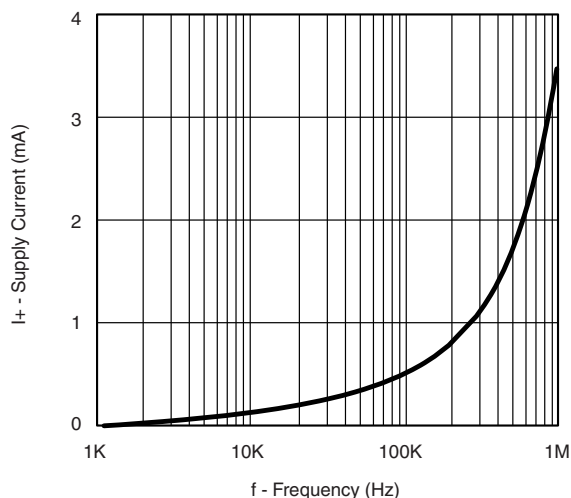
Switching Time vs. Power Supply Voltage



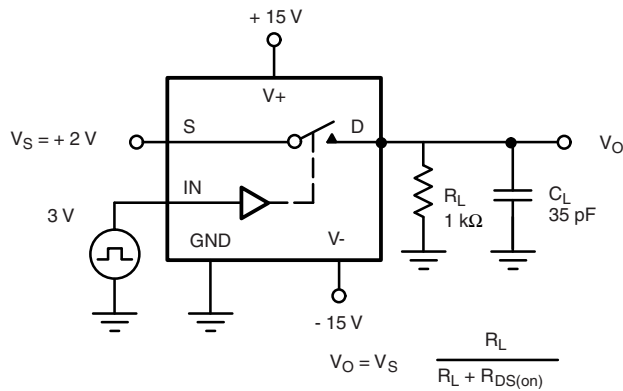
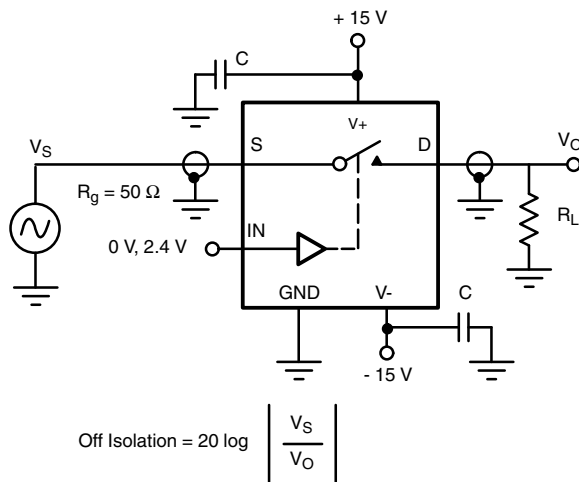
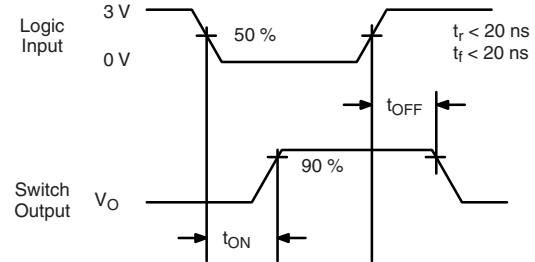
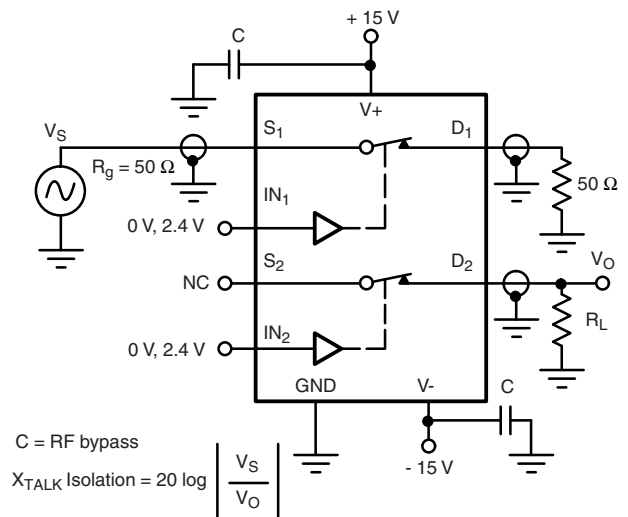
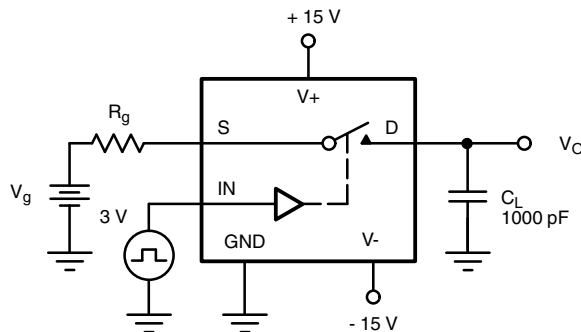
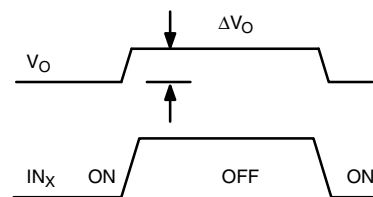
Q_S, Q_D - Charge Injection vs. Analog Voltage



Off Isolation vs. Frequency



Supply Current vs. Switching Frequency

TEST CIRCUITS

Figure 2. Switching Time

Figure 3. Off Isolation

Figure 4. Channel-to-Channel Crosstalk

Figure 5. Charge Injection


ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

APPLICATIONS

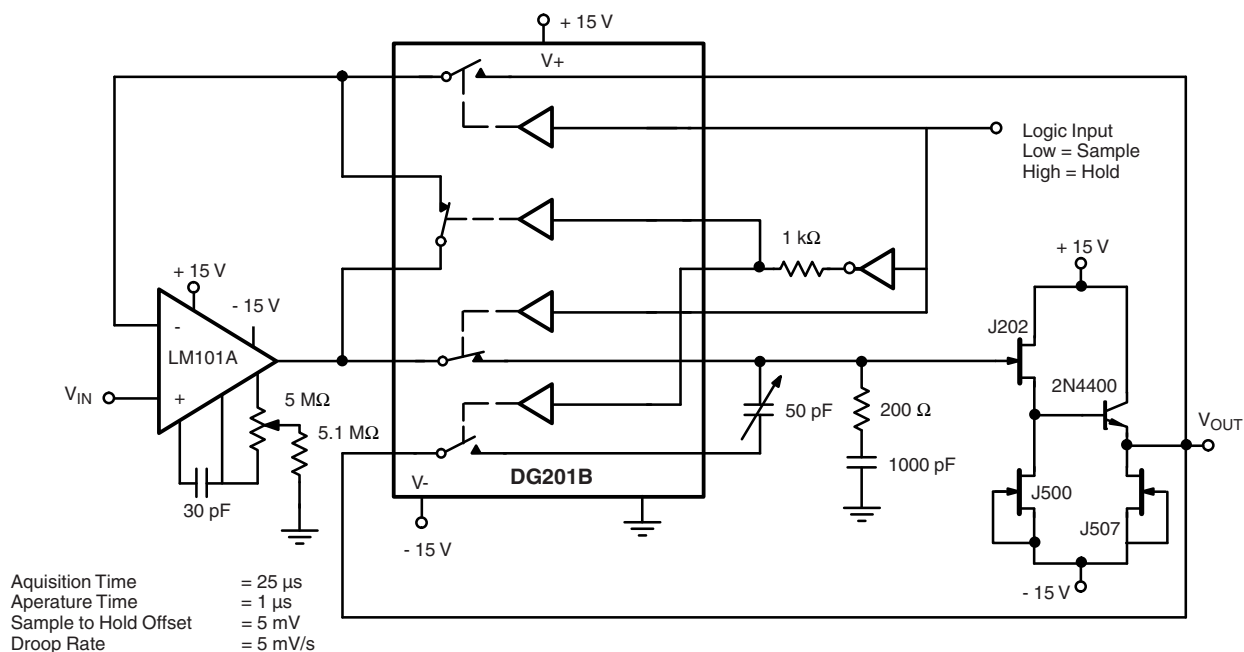
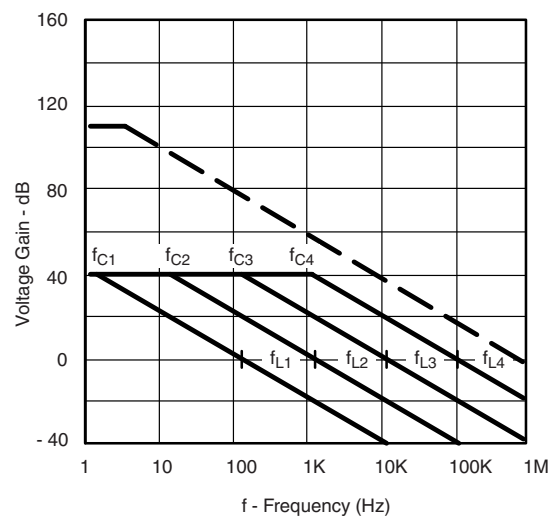
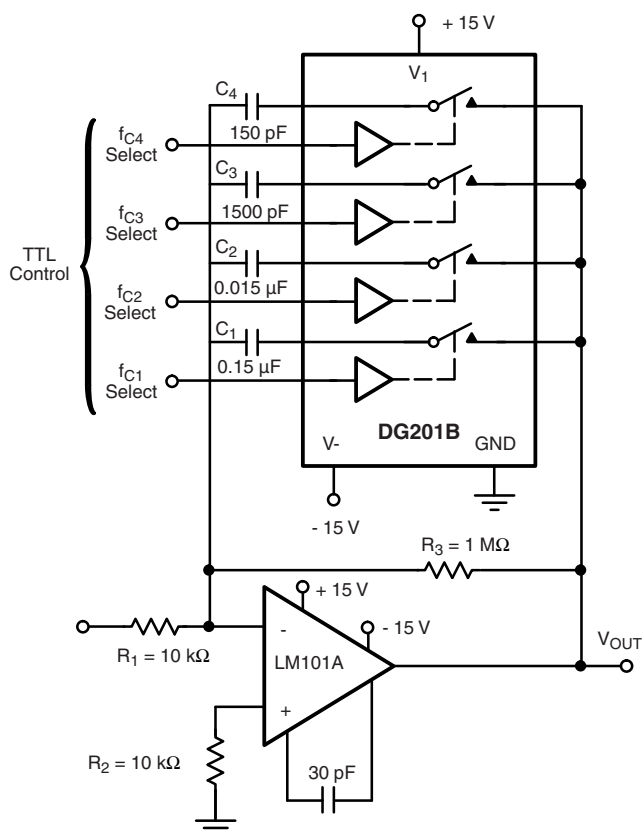


Figure 6. Sample-and-Hold



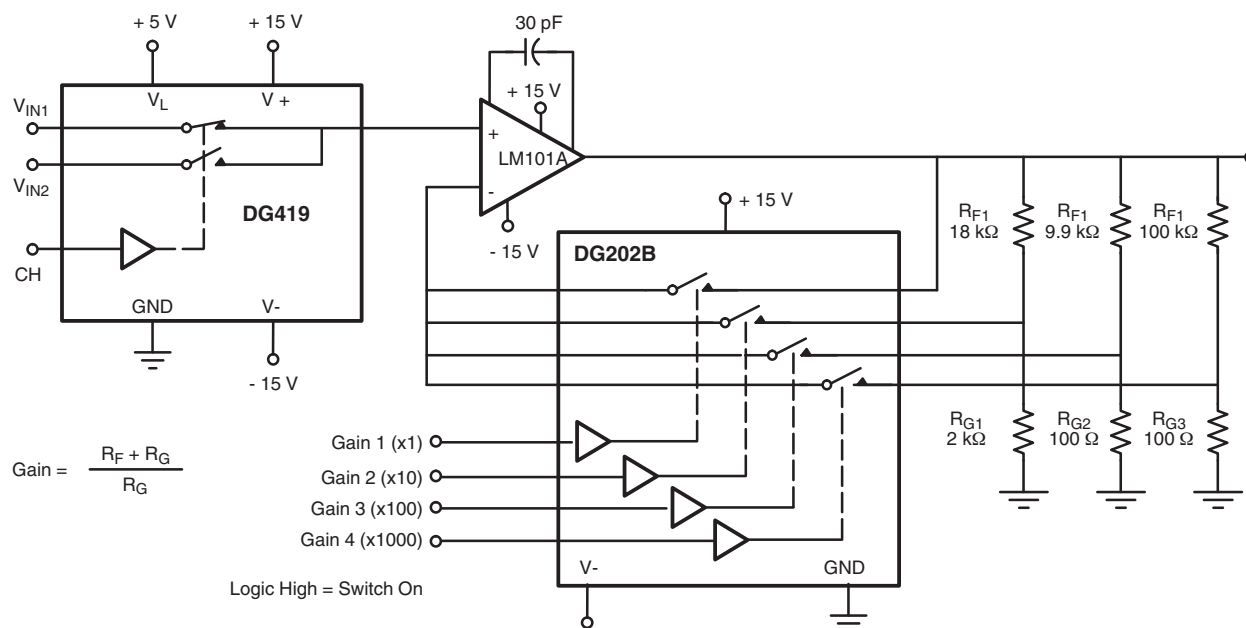
$$A_L \text{ (Voltage Gain Below Break Frequency)} = \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

$$f_C \text{ (Break Frequency)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (Unity Gain Frequency)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{Max. Attenuation} = \frac{R_{DS(on)}}{10 \text{ k}\Omega} \approx -47 \text{ dB}$$

Figure 7. Active Low Pass Filter with Digitally Selected Break Frequency

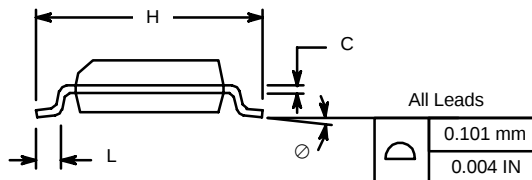
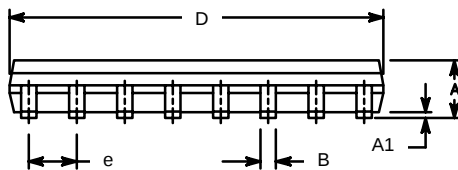
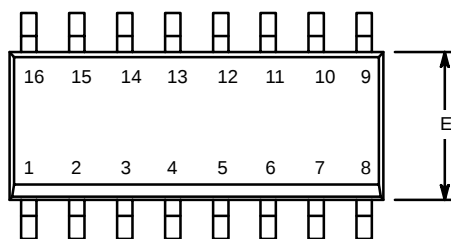
APPLICATIONS

Figure 8. A Precision Amplifier with Digitally Programmable Input and Gains

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SOIC (NARROW): 16-LEAD

JEDEC Part Number: MS-012

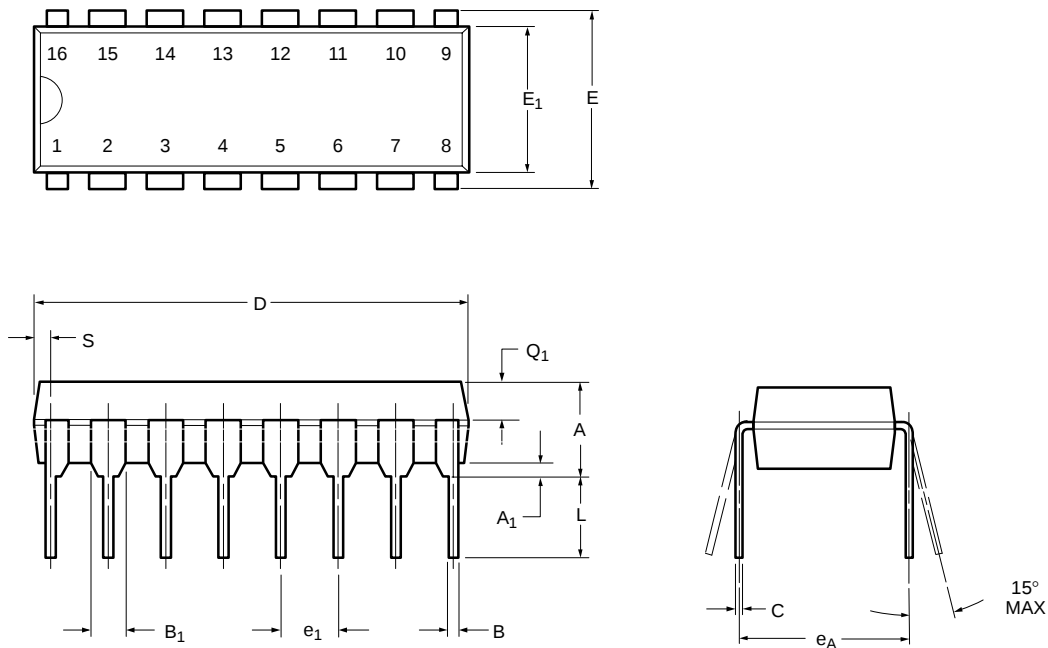


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
Ø	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



PDIP: 16-LEAD

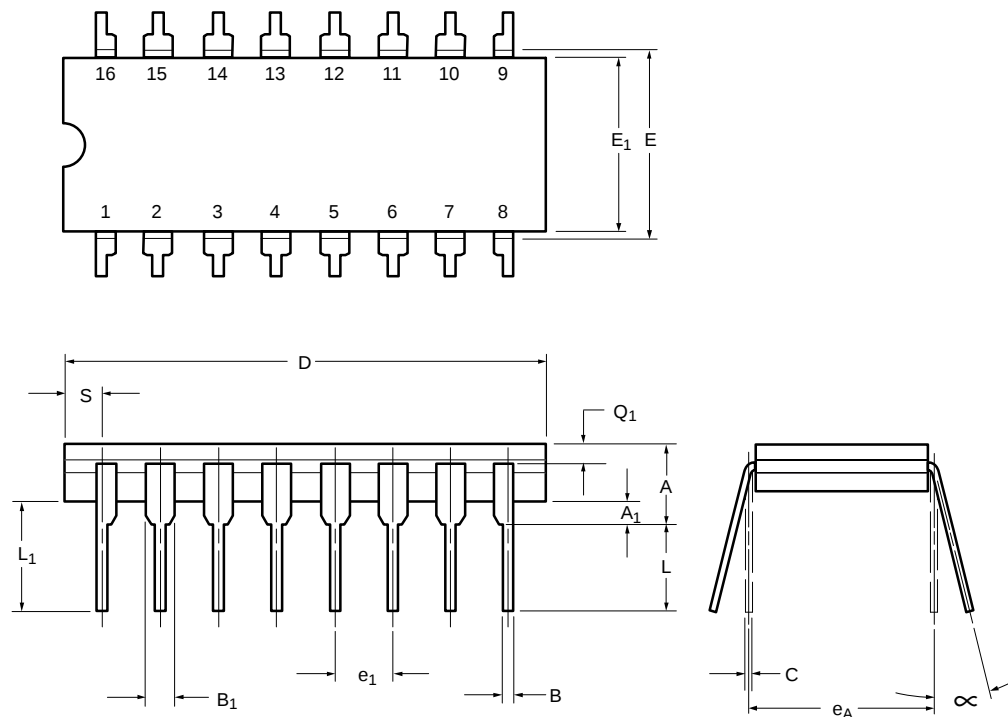


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A ₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B ₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E ₁	5.59	7.11	0.220	0.280
e ₁	2.29	2.79	0.090	0.110
e _A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q ₁	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482

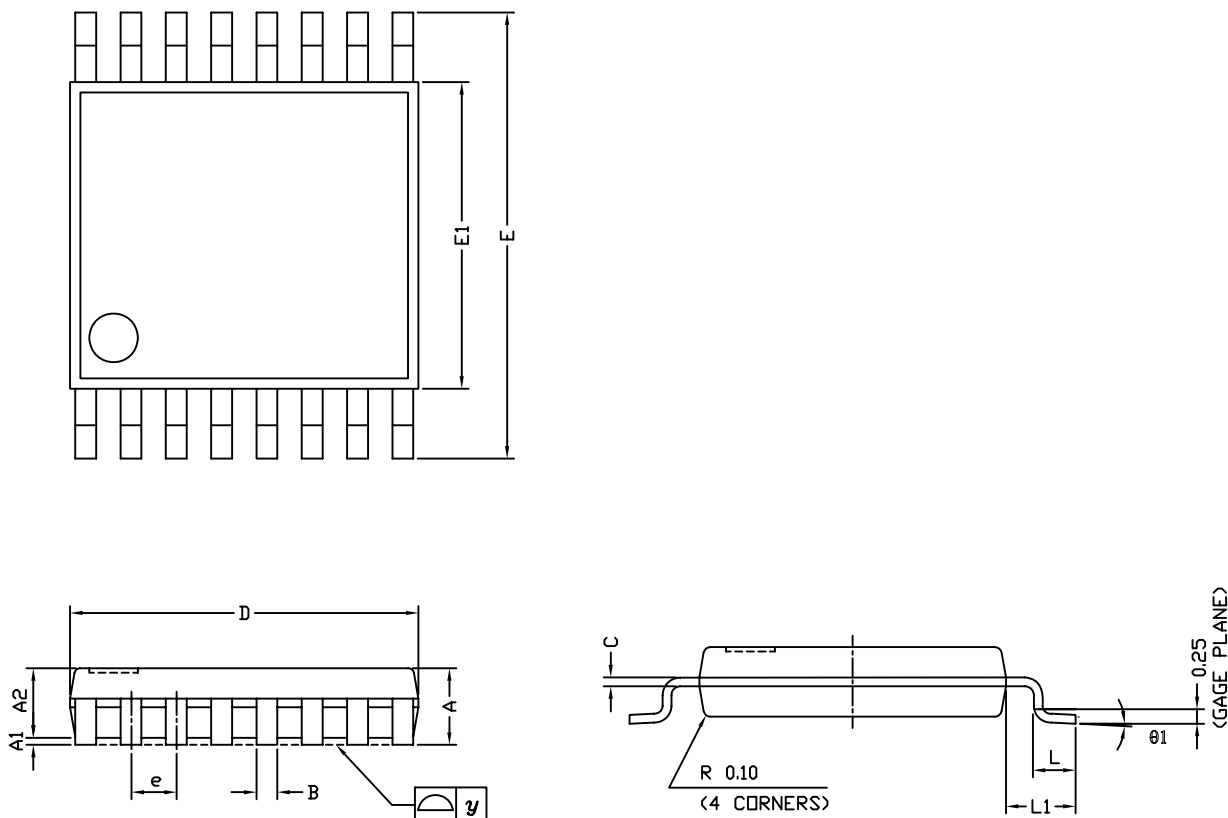


CERDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A ₁	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B ₁	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E ₁	6.60	7.62	0.260	0.300
e ₁	2.54 BSC		0.100 BSC	
e _A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L ₁	3.81	5.08	0.150	0.200
Q ₁	1.27	2.16	0.050	0.085
S	0.38	1.14	0.015	0.045
∞	0°	15°	0°	15°
ECN: S-03946—Rev. G, 09-Jul-01 DWG: 5403				

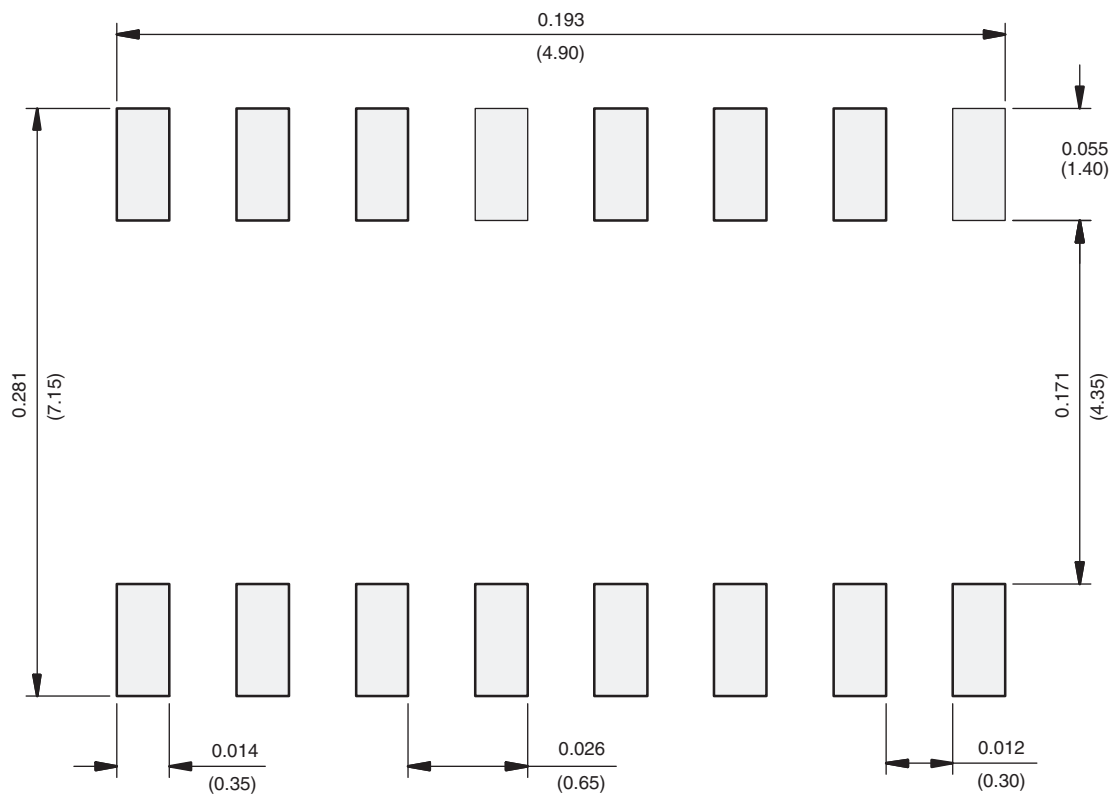
TSSOP: 16-LEAD



Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06			
DWG: 5624			

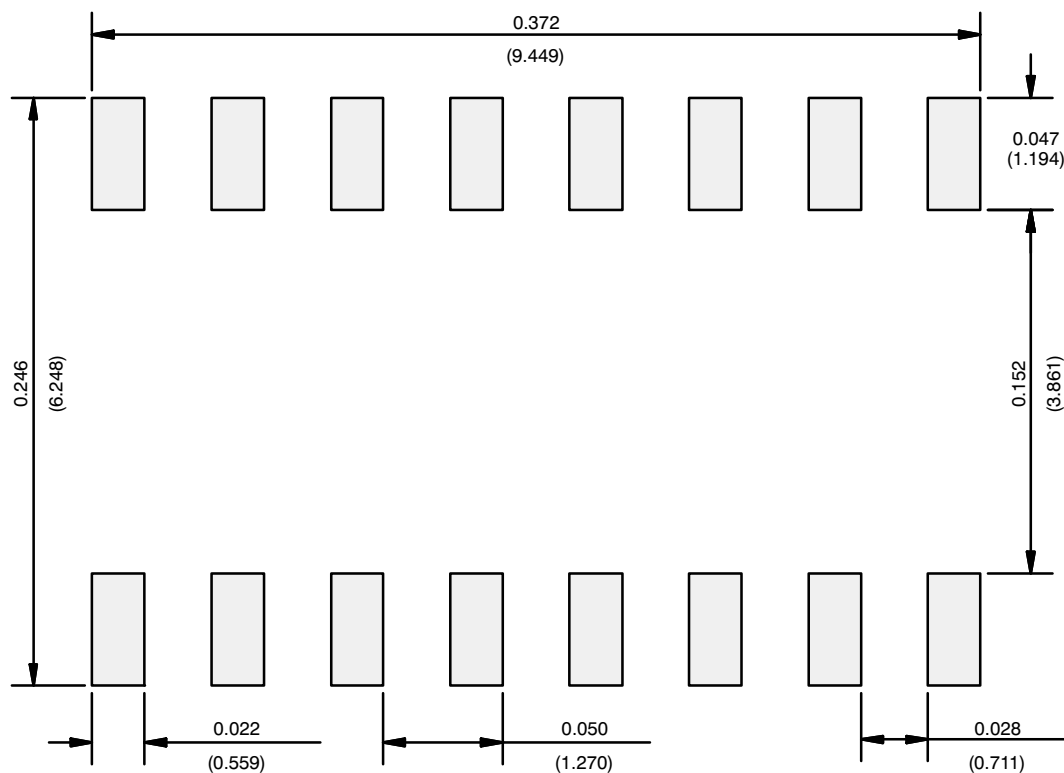


RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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