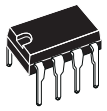
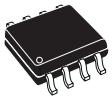
L6615

HIGH/LOW SIDE LOAD SHARE CONTROLLER

- SSI SPECS COMPLIANT
- HIGH/LOW SIDE CURRENT SENSING
- FULLY COMPATIBLE WITH REMOTE OUTPUT VOLTAGE SENSING
- FULL DIFFERENTIAL LOW OFFSET CURRENT SENSE
- 2.7V TO 22V V_{CC} OPERATING RANGE
- 32kΩ SHARE SENSE AMPLIFIER INPUT IMPEDANCE
- HYSTERETIC UVLO

BCD TECHNOLOGY





DIP8 **SO8**

ORDERING NUMBERS:

L6615N **L6615D**
L6615DTR(T & Reel)

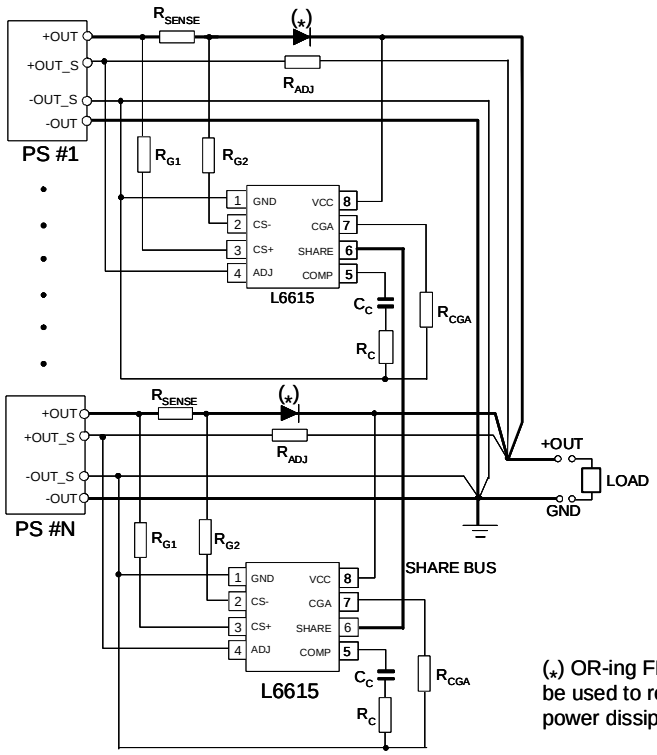
APPLICATION

- DISTRIBUTED POWER SYSTEMS
- HIGH DENSITY DC-DC CONVERTERS
- (N+1) REDUNDANT SYSTEMS, N UP TO 20
- SMPS FOR (WEB) SERVERS

DESCRIPTION

This controller IC is specifically designed to achieve load sharing of paralleled and independent power supply modules in distributed power systems, by adding only few external components. Current sharing is achieved through a single wire connection (share bus) common to all of the paralleled modules.

TYPICAL APPLICATION DIAGRAM



DESCRIPTION (continued)

Load sharing is a technique used in all the systems in which the load requires low voltage, high current and/or redundancy; for this reason a modular power system is necessary in which two or more power supplies or DC-DC converters are paralleled.

The device is able to perform both high side and low side current sensing, that is the sense current resistor can be placed either in series to the power supplies output or on the ground return.

The L6615 then drives the share bus to a voltage proportional to the output current of the master that is to the highest amongst the output currents delivered by the paralleled power supplies.

The share bus dynamics is independent of the power supply output voltage and is clamped only by the device supply voltage (V_{CC}).

The output voltage of the other paralleled power supplies (slaves) is then trimmed by the ADJ pin so that they can support their amount of load current. The slave power supplies work as current-controlled current sources.

Sharing the output currents is useful for equalizing also the thermal stress of the different modules and providing an advantage in term of reliability.

Moreover the paralleled supplies architecture allows achieving redundancy; the failure of one of the modules can be tolerated until the capability of the remaining power supplies is enough to provide the required load current.

PIN DESCRIPTION

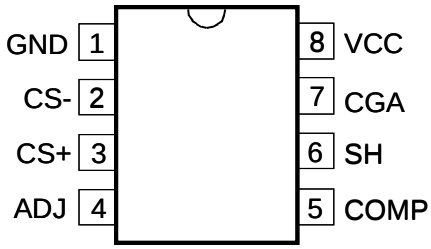
N°	Pin	Function
1	GND	Ground.
2	CS-	Input of current sense amplifier; it is connected to the negative side of the sense resistor through a resistor (R_{G2}).
3	CS+	Input of current sense amplifier. A resistor (R_{G1}, of the same value as R_{G2}) is placed between this pin and the positive side of the sense resistor: its value defines the transconductance gain between I_{CGA} and V_{SENSE}.
4	ADJ	Output of Adjust amplifier; it is connected to both the load (through a resistor R_{ADJ}) and to the positive remote sense pin of the power system. This pin is an open collector diverting (from the feedback path) a current proportional to the difference between the current supplied to the load by the relevant power supply and the current supplied by the master.
5	COMP	Output of the current sharing (transconductance) error amplifier and input of ADJ amplifier. Typically, a compensation network is placed between this pin and ground. The maximum voltage is internally clamped to 1.5V (typ.)
6	SH	Share bus pin. During the power supply *slave* operation, this pin acts as positive input from share bus. During power supply *master* operation, it drives the share bus to a voltage proportional to the load current. The *share* bus connects the SH pins of all the paralleled modules. A capacitor between this pin and GND could be useful to reduce the noise present on the share bus.
7	CGA	Current Gain Adjust pin; current sense amplifier output. A resistor connected between this pin and ground defines the maximum voltage on the share bus and sets the gain of the current sharing system.
8	V_{CC}	Supply voltage of the IC.

ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit
V_{CC}	8	Supply Voltage (*) (I_{CC}<50mA)	selflimit	V
I_{CS}+, I_{CS}-		Sense pin current	10	mA
V_{CS}-, V_{CS+}, V_{SH}, V_{ADJ}, V_{CGA}	2, 3, 6, 4, 7		-0.3 to V_{CC}	V
V_{COMP}	5	Error amplifier output	-0.3 to 1.5	V
(V_{CS+}) - (V_{CS-})		Differential input voltage (V_{CS}+ from 0V to 22V)	-0.7 to 0.7	V
Ptot		Total power dissipation @ Tamb = 70°C SO8 DIP8	 0.45 0.6	W
Tj		Junction temperature range	-40 to +125	°C
Tstg		Storage temperature	-55 to +150	°C

All voltages are with respect to pin 1. Currents are positive into, negative out of the specified terminal.
(*) Maximum package power dissipation limits must be observed

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	MINIDIP	SO8	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance junction to ambient	90	120	°C/W

ELECTRICAL CHARACTERISTCS

(Tj = -40 to 85°C, Vcc=12V, V_{ADJ} = 12V, C_{COMP} = 5nF to GND, R_{CGA} = 16kΩ, unless otherwise specified; $V_{SENSE} = I_L * R_{SENSE}$, $R_{G1} = R_{G2}$ = 200Ω)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vcc						
V_{cc}	Operating range		2.7		22	V
I_{cc}	Quiescent current	V_{SH}= 1V, V_{SENSE}= 0V		5	6	mA
$V_{CC, ON}$	Turn-on voltage	V_{SH}= 0.2V, V_{SENSE}= 0V	2.45	2.60	2.75	V
$V_{CC,OFF}$	Turn-off voltage		2.35	2.5	2.65	V
V_H	Hysteresis			100		mV
Vz		I_{CC} = 20mA	24	26		V
CURRENT SENSE AMPLIFIER						
V_{OS}	Input offset voltage	0.1V ≤ V_{SH} ≤ 10.0V	-1.5	0.0	1.5	mV
V_{CGA}	Out high voltage	V_{SENSE} = 0.25V	V_{cc}-2.2			V
I_{CGAS}	Short circuit current	V_{CGA}= 0V, V_{SENSE}= 0.45V	-1.5	-2.0		mA
$I_{B(CS-)}$	Input bias current (high side sensing)	V_{SENSE} = 0V, V_{CS+}=+12V			1.0	µA
$I_{B(CS+)}$	Input bias current (low side sensing)	V_{SENSE} = 0V, V_{CS+}=0V			-1.0	µA
CMR	Common mode dynamics range	V_{CS-}, V_{CS+}	0		V_{CC}	V
VTH_{CS+}	Switchover threshold low side to high side sensing	V_{CS+}		1.6		V
SW_H	Switchover hysteresis			0.16		V
SHARE DRIVE AMPLIFIER						
HV_{SH}	SH high output voltage	V_{SENSE}= 250mV, I_{SH}= -1mA	V_{cc}-2.2			V
LV_{SH}	SH low output voltage	V_{CGA}= 0mV, R_{SH}= 200Ω			45	mV
α(+)	High side sensing mirror accuracy (*)			±1	±5	%
α(-)	Low side sensing mirror accuracy (*)			±1	±5	%
$V_{SH, load}$	Load regulation	-1.0mA ≤ $I_{SDA(OUT)}$ ≤ -4mA			20	mV
I_{SC}	Short circuit current	V_{SH}= 0V, V_{SENSE}= 25mV	-20	-13.5	-8	mA
SR	Slew rate	V_{SENSE}= -10mV to 90mV step, R_{SH}= 200Ω to GND	0.8	1.5	2.2	V/µs
		V_{SENSE}= 90mV to –10mV step, R_{SH}= 200Ω to GND	2	3	4	V/µs
SHARE SENSE AMPLIFIER						
R_i	Input impedance		22.4	32	41.6	kΩ
ERROR AMPLIFIER						
G_m	Transconductance		3	4	5	mS
V_{os}	Input offset voltage	V_{CGA}=1V	30	50	70	mV

ELECTRICAL CHARACTERISTCS (continued)

(Tj = -40 to 85°C, Vcc=12V, V_{ADJ} = 12V, C_{COMP} = 5nF to GND, R_{CGA} = 16kΩ, unless otherwise specified; $V_{SENSE} = I_L * R_{SENSE}$, $R_{G1} = R_{G2}$ = 200Ω)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{OH}	Source current	V_{COMP}=1.5V, $V_{SH} \geq$ 300mV, V_{SENSE}=-10mV	-150	-350	-400	µA
I_{OL}	Sink current	V_{COMP}= 1.5V, V_{SENSE}=-10mV 200Ω resistor SH to GND	100	200	300	µA
$V_{COMP(L)}$	Low voltage		0.05	0.15	0.25	
V_Z	Clamp Zener voltage	I_Z = 1mA		1.5		V
ADJ AMPLIFIER						
I_{ADJ}	Max. ADJ output current	V_{SH}= 1V, V_{SENSE}= 0V	6.5	10	13	mA
V_T	Threshold voltage	I_{ADJ}=10µA		0.7		V
R_A	Emitter resistor	Guaranteed by design	60	100	140	Ω
$V_{ADJ(MIN)}$	Low saturation voltage	I_{ADJ}=5mA			1	V
		I_{ADJ}=1mA			0.4	V

(*) Mirror accuracy is defined as $\left(\frac{V_{SH}}{V_{SENSE} \cdot \frac{R_{CGA}}{R_G}} - 1 \right) \cdot 100$

and it represents the accuracy of the transfer between the voltage sensed and the voltage imposed on the share bus.

BLOCK DIAGRAM

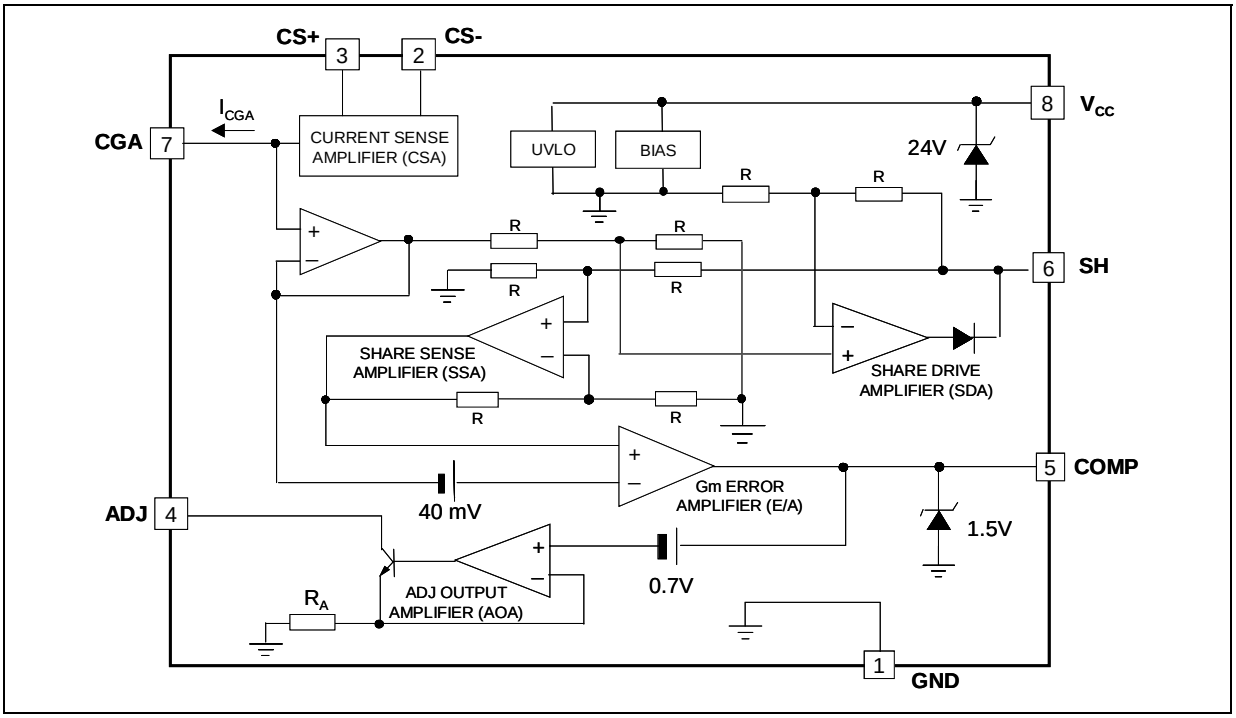


Figure 1. Turn-on and turn-off voltage

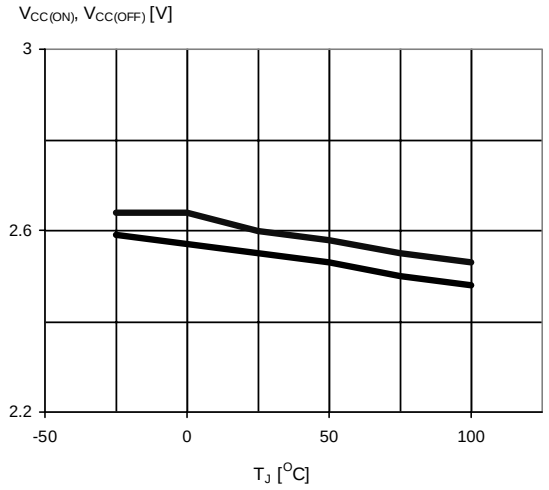


Figure 2. Supply current vs. supply voltage

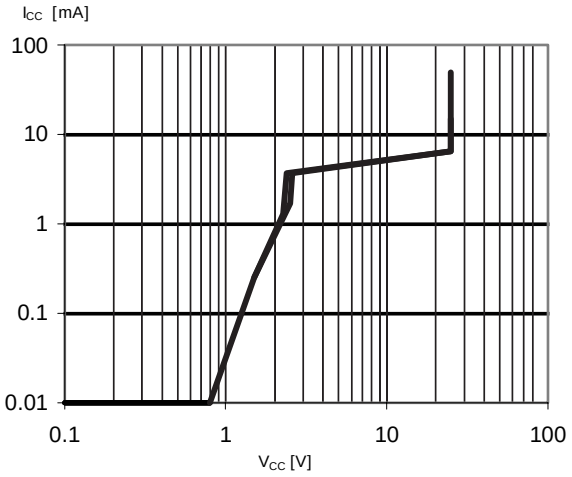


Figure 3. Supply current

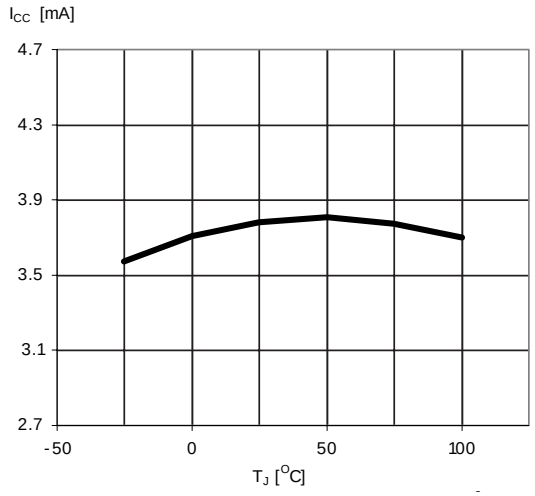


Figure 4. Max CGA current

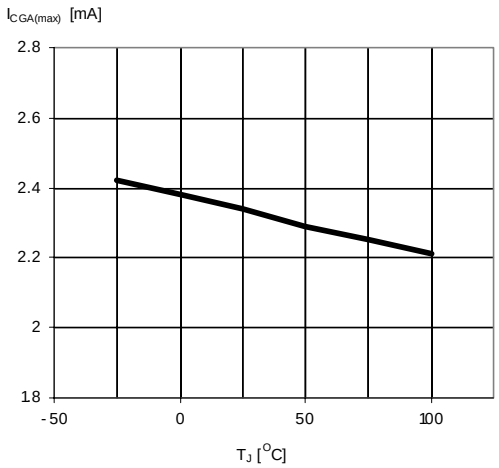


Figure 5. High side/low side sensing switchover threshold

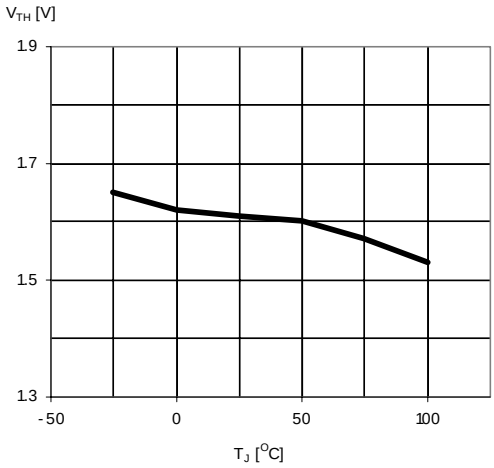


Figure 6. Max. share bus voltage at no load

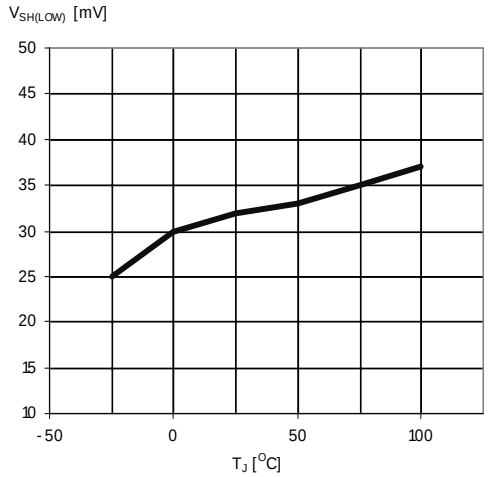


Figure 7. Share bus input impedance

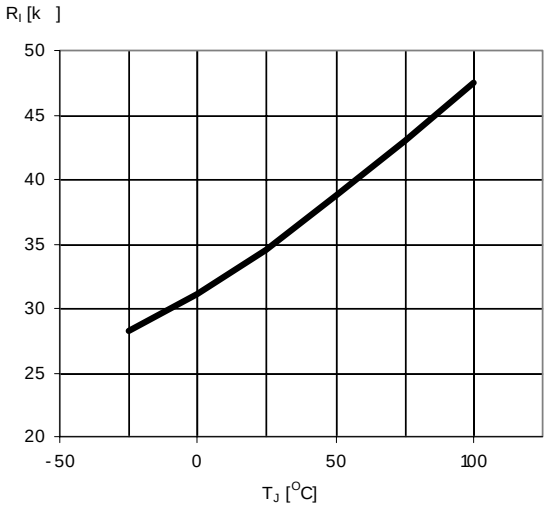
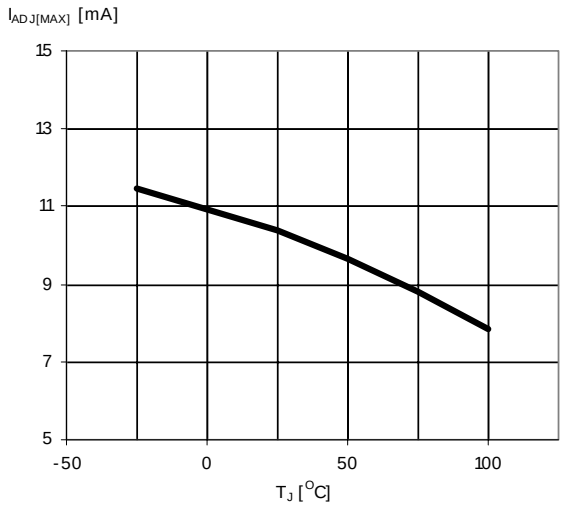


Figure 8. ADJ maximum current



APPLICATION INFORMATION

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1 INTRODUCTION

Power supply systems are often designed by paralleling converters in order to improve performance and reliability.

To ensure uniform distribution of stresses, the total load current should be shared appropriately among the converters.

A typical application is showed in fig. 9 for a series of N paralleled modules (PS#1 to PS#N): each of them exhibits 4 terminals: two for the power output (+OUT, -OUT) and two for the remote sense signals (+OUT_S, -OUT_S).

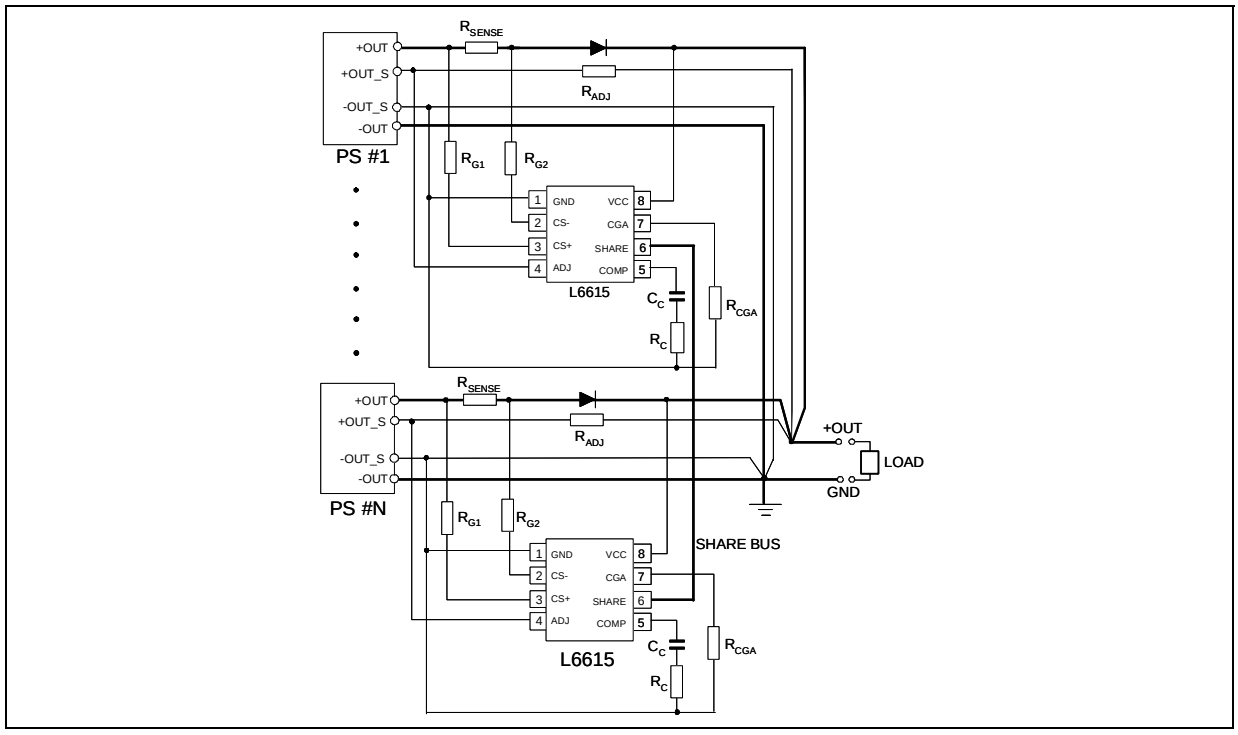
On the power lines are placed the sense resistors R_{SENSE} (for the current sensing) and the OR-ing diodes (to avoid that the failure of one module shorts the load out)

L6615 allows attaining an automatic master-slave current sharing architecture: one L6615 is associated to each power supply and all these IC's are linked each other through the share bus (referred to the common ground).

This kind of system configuration is preferred to the systems in which a single current sharing controller is used because of robustness, reliability and flexibility.

To configure a load share controller, few passive components are used. A brief device explanation will follow with the formulas useful to set these external components.

Figure 9. Typical high side connection



2 CURRENT SENSE SECTION

A sense resistor is typically used to generate the voltage drop, proportional to the load current, measured by the CSA (Current Sense Amplifier), whose input pins (pins #2 and #3) are connected across of R_{SENSE} through two identical resistors (RG1 and RG2).

The CSA consists of 2 sections (see fig. 10), one responsible for the high side sensing, the other for low side sensing. An internal comparator activates the relevant section in accordance with the voltage present at CS+ pin: if this voltage is higher than 1.6V (typ), then the high side sensing section will be activated (fig10.a) otherwise the low side sensing one will (fig 10.b). For the sake of simplicity we will consider R_{G1}= R_{G2}= R_G.

As the voltage drop I_{OUT}*R_{SENSE} is present at the input of the Sense Amplifier section, its output forces the controlled current mirror to:

– sink current from the CS+ pin in case of high side sensing (neglecting input bias current, no current flows through CS- pin);

– source current from the CS- pin in case of low side sensing (neglecting input bias current, no current flows through CS- pin).

The local feedback imposes the same voltage at the current sense input pins, so under closed loop condition V_{SENSE}=VR_G.

The current

$$I_{CS} = \frac{I_{OUT} \cdot R_{SENSE}}{R_G}$$

(IC_{S+} in case of high side, I_{CS-} in case of low side) is then internally mirrored and sent to the CGA pin causing a drop across the R_{CGA} external resistor: two internal buffers transfer V_{CGA} signal on the share pin so:

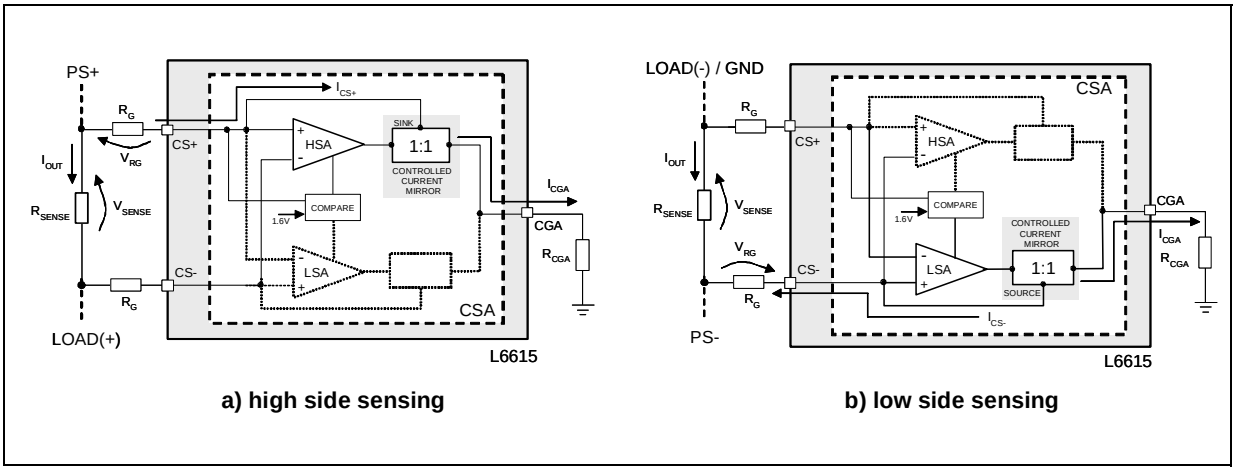
$$V_{SH} = \frac{V_{SNS}}{R_G} \cdot R_{CGA}$$

Only the L6615 V_{CC} limits the upper voltage at the CGA and SH pin, independently of the voltage present at the current sense pins.

In noisy applications, two capacitors of small value (e.g. 1nF) connected between current sense pins and ground could be useful to clean the signal at the input of the current sense amplifier.

For low voltage buses application, see paragraph 7.

Figure 10. Current sense section



3 SHARE DRIVE SECTION, ERROR AMPLIFIER AND ADJUST AMPLIFIER

The gain between the output of CSA (CGA pin) and output of SDA (SH pin) is 1 (typ.) so, for the master power supply, $V_{CGA} = V_{SH}$; the voltage on the share bus is imposed by the master.

In the slave converters, being $V_{CGA(SLAVE)} < V_{CGA(MASTER)}$, the diode at the output of SDA (see block diagram) isolates the output this amplifier from the share bus.

The Share Sense Amplifier (SSA) reads the bus voltage transferring the signal to the non-inverting input of the error amplifier where it is compared with CGA voltage.

Whenever a controller acts as the master in the system, the voltage difference between the E/A inputs is zero. To guarantee its output low in such condition, a 40mV offset is inserted in series with the inverting input.

Instead in the slave converters the input voltage difference is proportional to the difference between the master load current and the relevant slave load current.

The transconductance E/A converts the ΔV at its inputs in a current equal to

$$I_{OUT} = G_M \cdot \Delta V$$

flowing in the compensation network connected between COMP pin and ground.

The E/A output voltage drives the adjust amplifier to sink current from the ADJ pin that is connected to the output voltage through a small resistor along the sense path. The current sunk by ADJ pin is deviated from feedback path of the slave power supply that reacts increasing its duty cycle.

In steady state the current sunk by the ADJ pin is proportional to the value of error amplifier output.

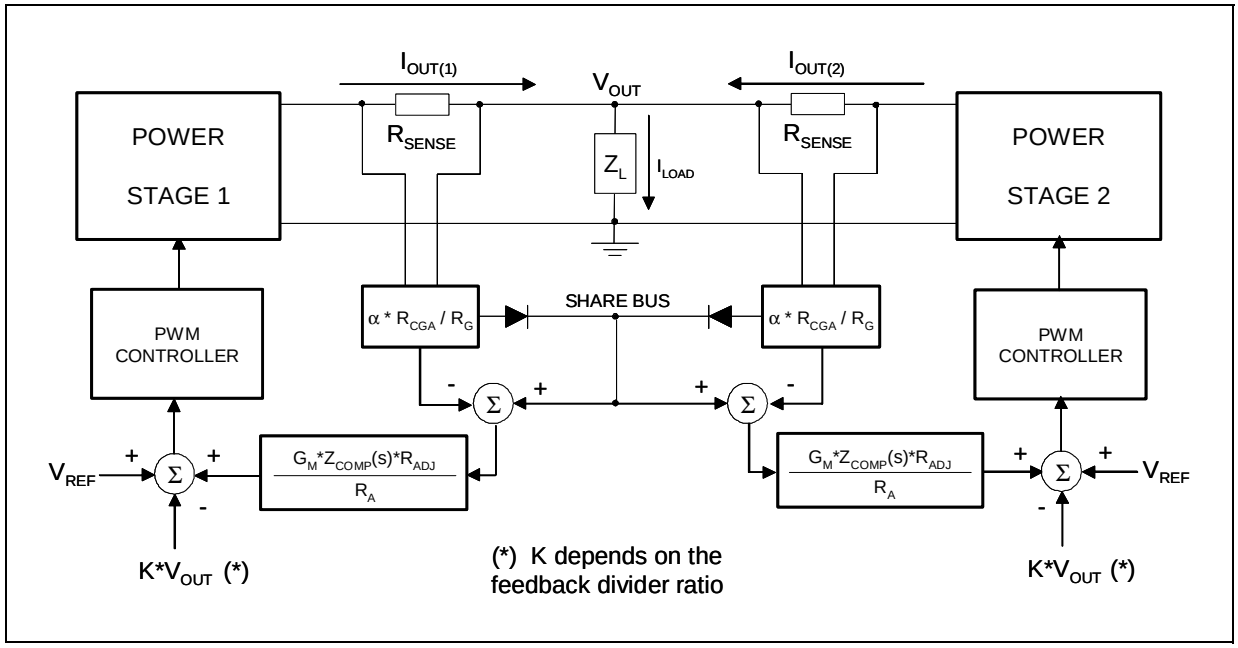
4 DESIGNING WITH L6615

The first design step is usually the choice of the sense resistor whose maximum value is limited by power dissipation; this constraint must be traded off against the precision of L6615 current sensing. In fact a small sense resistance value lowers the power dissipation but reduces the signal available at the inputs of the L6615 current sense amplifier.

Once fixed R_{SENSE} then the values for R_G and R_{GCA} will be chosen in accordance with the application specs: usually these specs define the share bus voltage ($V_{SH(MAX)}$) and the number of paralleled power supplies.

Their value must comply with the constraints imposed by the L6615:

Figure 11. Simplified feedback block diagram.



– maximum share bus voltage is internally limited up to 2.2V below L6615 V_{CC} voltage (pin#8);

– $V_{SH(MAX)}$ represents an upper limit but the designer should select the full scale share bus voltage keeping in mind that every Volt on the share bus will increase the master controller's supply current by approximately 45µA for each slave unit connected in parallel; this total current, provided by the master share drive amplifier, must be lower than its minimum output capabilty (8mA) so

$$V_{SH(MAX)} < \frac{R_{i(MIN)}}{N} \cdot 8mA$$

This condition is not tough to meet in normal applications, as one can easily see by using sensible values for N (number of paralleled power supplies) and $V_{SH(MAX)}$. For example, with $V_{SH(MAX)}$=8V, solving for N, we obtain Nmax=20;

– maximum share drive amplifier current capability ($I_{CGA(MAX)}$=2mA);

– for safety reasons the following relation must be met:

$$R_G > \frac{1}{2} \cdot \left(\frac{V_{out}}{10mA} - 40 \right)$$

in this way no fault will cause I_{CS+} (or I_{CS-}) to overcome its absolute maximum ratings.

At full load, $\Delta V_{SENSE(MAX)} = I_{OUT(MAX)} \cdot R_{SENSE(MAX)}$ is the maximum voltage drop across the resistor R_{SENSE} (typically few hundreds of millivolt).

$I_{OUT(MAX)}$ is the maximum current carried by each of the paralleled power supply; in non redundant systems composed by N power supplies, each of them works at its nominal current, so:

$$I_{OUT(MAX)} = \frac{I_{LOAD}}{N}$$

This relationship is true also in N+M redundant system, even if under normal condition each power supply provides $I_{LOAD}/(N+M)$.

For example in a system composed by two paralleled power supplies 100% redundant (N=M=1), each module is sized to sustain the entire load current (in normal operation it carries only one half): for this reason the sense resistor must be sized considering the whole load current.

The temperature variation of the sense resistor (hence of its resistance value) has to be taken into account, so $R_{SENSE(MAX)}$ is the value at maximum operating temperature to avoid saturating the share bus.

Once fixed $V_{SENSE(MAX)}$, the ratio R_{CGA}/R_G (gain from the sensing section to the share bus) can be calculated:

$$\frac{R_{CGA}}{R_G} = \frac{V_{SH(MAX)}}{V_{SENSE(MAX)}}$$

where $V_{SH(MAX)}$ is defined by the application.

A small capacitor in parallel to R_{CGA} is useful to reduce the noise.

The effect of current sharing feedback loop is to force the voltages of the slave's CGA pins to be equal to V_{SH} (that is to reduce the voltage difference at the inputs of the L6615 error amplifier). For the sake of simplicity we consider 2 paralleled power supplies (as in fig. 11): under closed loop condition:

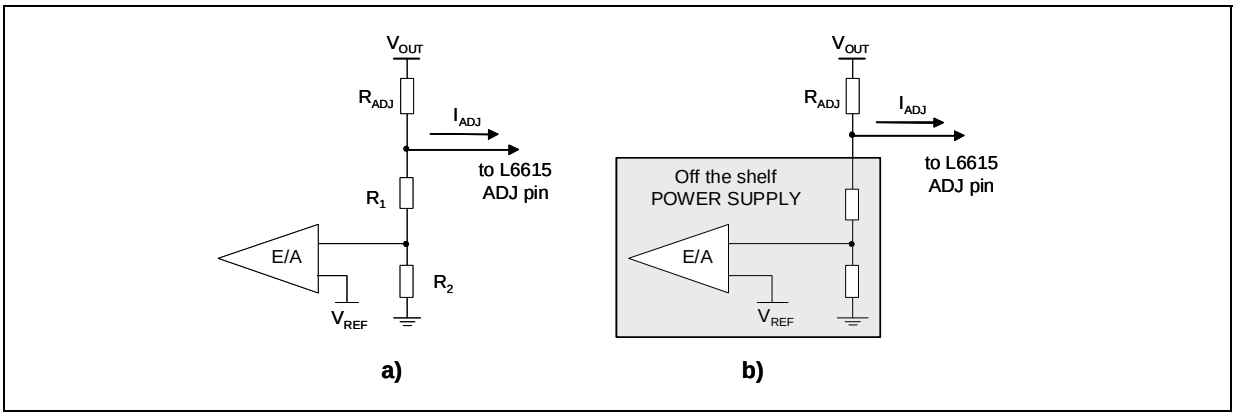
$$I_{OUT(1)} \cdot \frac{R_{SNS(1)}}{R_{G(1)}} \cdot R_{CGA(1)} = I_{OUT(2)} \cdot \frac{R_{SNS(2)}}{R_{G(2)}} \cdot R_{CGA(2)}$$

Ideally all the external component and α are matched so:

$$I_{OUT(1)} = I_{OUT(2)} = \frac{I_{LOAD}}{2}$$

Any mismatch will have repercussion on the sharing precision: in particular the maximum difference between the output currents (sharing error) will be given by the sum of the mismatches amongst the relevant values.

Figure 12. ADJ network



To set the R_{ADJ} value it is necessary to know the tolerance required of the power supply output voltage ($V_{OUT}\pm\Delta V_O$); the maximum difference between master and slave output voltage is $2*\Delta V_O$ and this amount represents the voltage that the L6615 must be able to correct.

Now two different approaches are feasible depending on whether the SMPS (whose output current must be shared) has to be completely designed or it is an "off the shelf" component and only the current sharing section must be designed.

In the first case, the adjustment resistor (R_{ADJ}) can be considered as a fraction of the high resistor of the feedback divider R_H (see fig.12.a): typically the first step consist of fixing the current flowing, under steady state condition, through the feedback divider I_{FB}; by choosing the value for R_2:

$$I_{FB} = \frac{V_{REF}}{R_2}$$

we will have:

$$R_H = R_1 + R_{ADJ} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R_2$$

It can be an useful rule of thumb to use R_{ADJ} lower than (or equal to) one tenth of R1, considering that, in worst case condition, it will be:

$$I_{ADJ(max)} = \frac{\Delta V_{OUT}}{R_{ADJ}}$$

This value must not exceed the one indicated in the "Electrical characteristic section" but this is very easy to meet, as one can easily see by using sensible values for ΔV_{OUT} and R_2.

In the second case (fig 12.b), the feedback divider has been already designed by the SMPS manufacturer and it is not possible to modify it: the design of R_{ADJ} must be done to make the L6615 able to correct the maximum spread without significantly shifting the SMPS regulation point. A minimum R_{ADJ} value can be found by:

$$R_{ADJ(min)} = \frac{\Delta V_{OUT}}{I_{ADJ(max)}}$$

where $I_{ADJ(max)}$ is 8mA.

Especially for low voltage output buses it is important to avoid adjustment network saturation; the design must satisfy the following relationship:

$$V_{OUT} - R_{ADJ} \cdot (I_{ADJ} + I_{FB}) > V_{ADJ(MIN)}$$

where $V_{ADJ(MIN)}$ can be found in the "Electrical characteristic section" for different I_{ADJ} values.

The last point is the design of the compensation network $Z_C(s)$ connected between the COMP pin and ground.
Besides the power supply feedback loop, the current sharing system introduces another, outer loop. To avoid interaction between them it is important to design the bandwidth of the sharing loop at least one order of magnitude lower than the bandwidth of the power supply loop.
For the total system, the loop gain is:

$$G_{LOOP(s)} = R_{SENSE} \cdot \frac{R_{CGA}}{R_G} \cdot G_M \cdot Z_C(s) \cdot \frac{R_{ADJ}}{R_A} \cdot A_{PWR}(s) \cdot \frac{1}{R_{LOAD}}$$

where

$A_{PWR}(s)$ is the transfer function of PWM controller and power stage (see fig. 11)
R_{LOAD} is the equivalent load resistance

Typically the compensation network is built by a R-C series.
A resistor in series with C_C is required to boost the phase margin of the load share loop. The zero is placed at the load share loop crossover frequency, $f_{C(SH)}$.
If $f_{C(SH)}$ is the share loop crossover frequency, then:

$$C_C = \frac{1}{2 \cdot \pi \cdot f_{C(SH)}} \cdot \frac{R_{CGA} \cdot G_M}{R_G} \cdot \frac{R_{ADJ}}{R_A} \cdot \frac{R_{SENSE}}{R_{LOAD}} \cdot \left| A_{PWR(f_{C(SH)})} \right|$$

$$R_C = \frac{1}{2 \cdot \pi \cdot f_{C(SH)} \cdot C_C}$$

5 CURRENT SENSE METHODS

Several are the methods to sense the power supply output current; the simplest one is to use a power resistor (fig. 13a) but increasing load current could require expensive resistor to support the inherent power dissipation, imposing the use of several paralleled resistor.
Other methods to sense the output current are showed in fig. 13b and 13c:

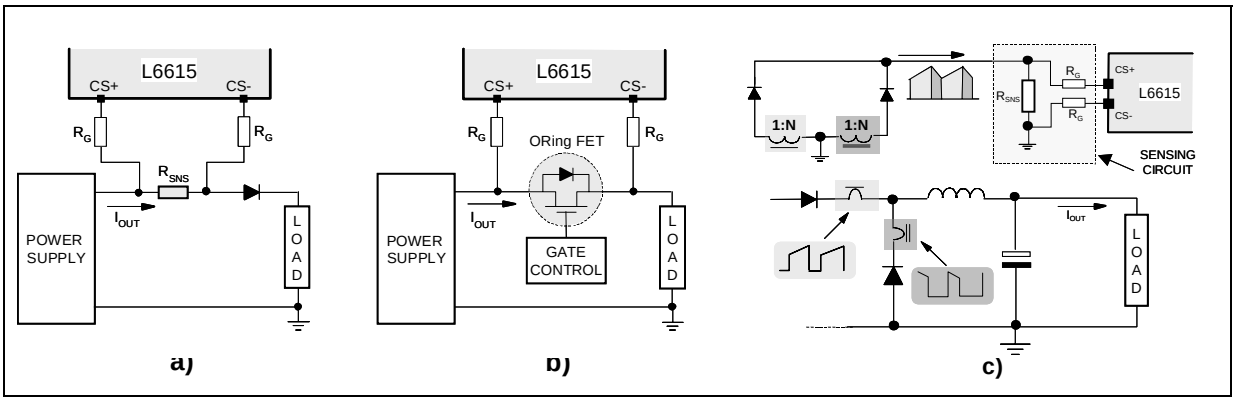
1. **$R_{DS(ON)}$:** a power MOS is placed in series to the output and its channel resistance ($R_{DS(ON)}$) is used as sense resistor (fig 13a): the L6615 sense pins will be connected, through R_G resistors to the drain and to the source of the MOS. Besides providing the sense resistor, the FET is used as "ORing" element: driving properly its gate, it is possible isolate the power supply output from the load (the body diode is reversed biased so it doesn't conduct).
   This is useful whenever features like hot swap or hot plug are required; compared with the well-known solution using ORing diode, the ORing FET greatly reduces the power dissipation, in particular:

   $$P_{(DIODE)} = V_F \cdot I_{OUT} + R_{SENSE} \cdot I_{OUT}^2$$

   $$P_{(MOS)} = R_{DS(ON)} \cdot I_{OUT}^2$$

   where V_F is the forward drop across the diode.
2. **Current transformer:** in case of very high load currents, a transformer allows sensing a smaller current, obtained through a scaling factor equal to the transformer turn ratio. In this way, the sense resistor power dissipation requirements can be less tight: obviously this is paid with the cost of the transformer.
   In fig. 13c it is showed the simplified output stage of a power supply in forward configuration: through two current transformers the load current is reproduced in the sensing circuit scaled by a factor N. R_{SENSE} will read a ripple (at the switching frequency) superimposed on the average current value that doesn't affect the correct behaviour of the current sharing system because its loop gain is designed with a low bandwidth - at least 2 order of magnitude lower than the switching frequency - that will cut this high frequency.

Figure 13. Current sense methods.



6 APPLICATION IDEAS

In fig. 14 is showed a single section of a system in which several DC to DC modules can be paralleled, typical solution whenever the load requires high current at low voltage; the converter is designed for a step down configuration using a synchronous rectification controller (for example L6910 [1] or L6911 [2] ST device).

The L6615 reads the drop across the Rds(ON) of the OR-ing FET and the LM293 drives its gate, pulling it down whenever a fault condition (e.g. short on the low side) appears.

A charge pump could be necessary to be sure that the ORing FET V_{GS} is higher than $V_{GS(TH)}$ (depending on the input and output voltage).

Figure 14. 0.9 to 5V DC-Dc converter with Current Sharing and output hot-pluggability

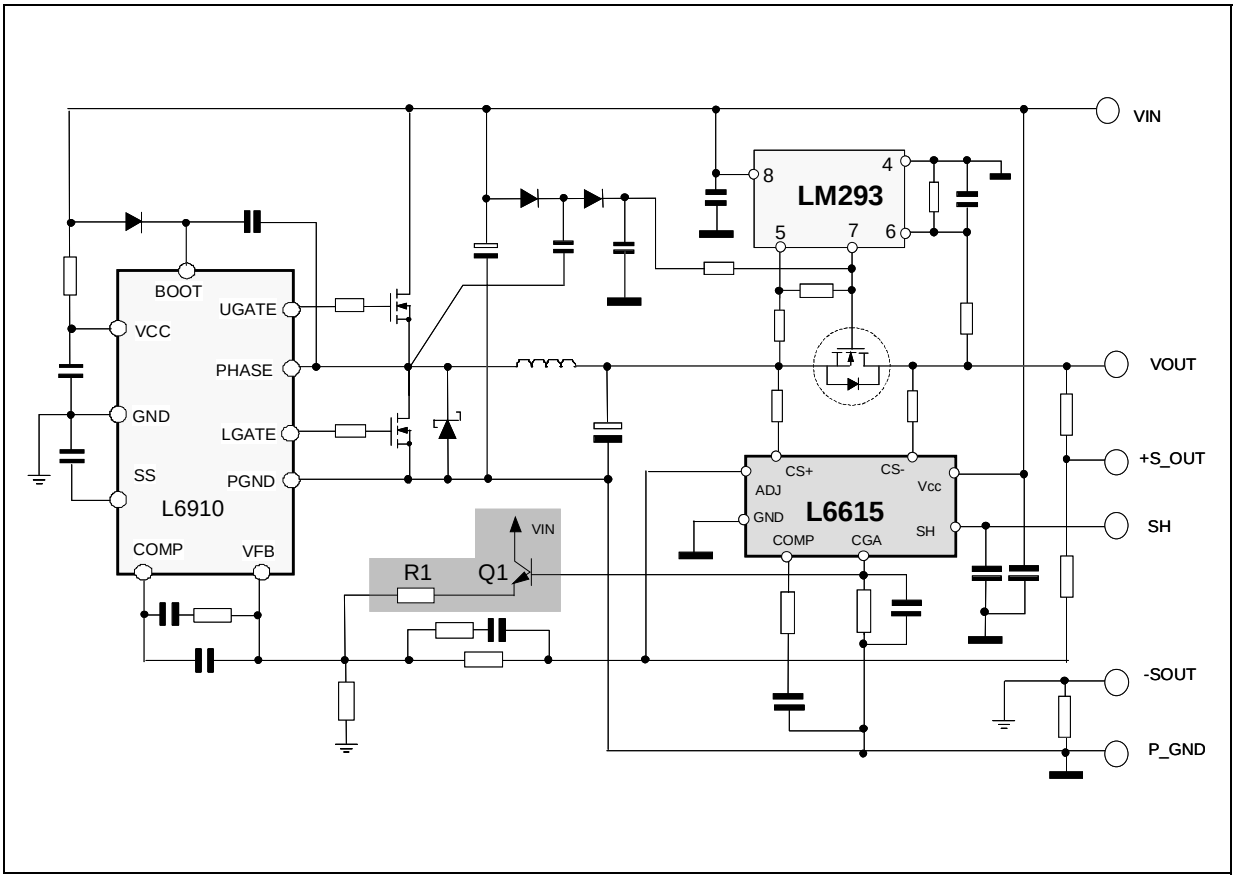
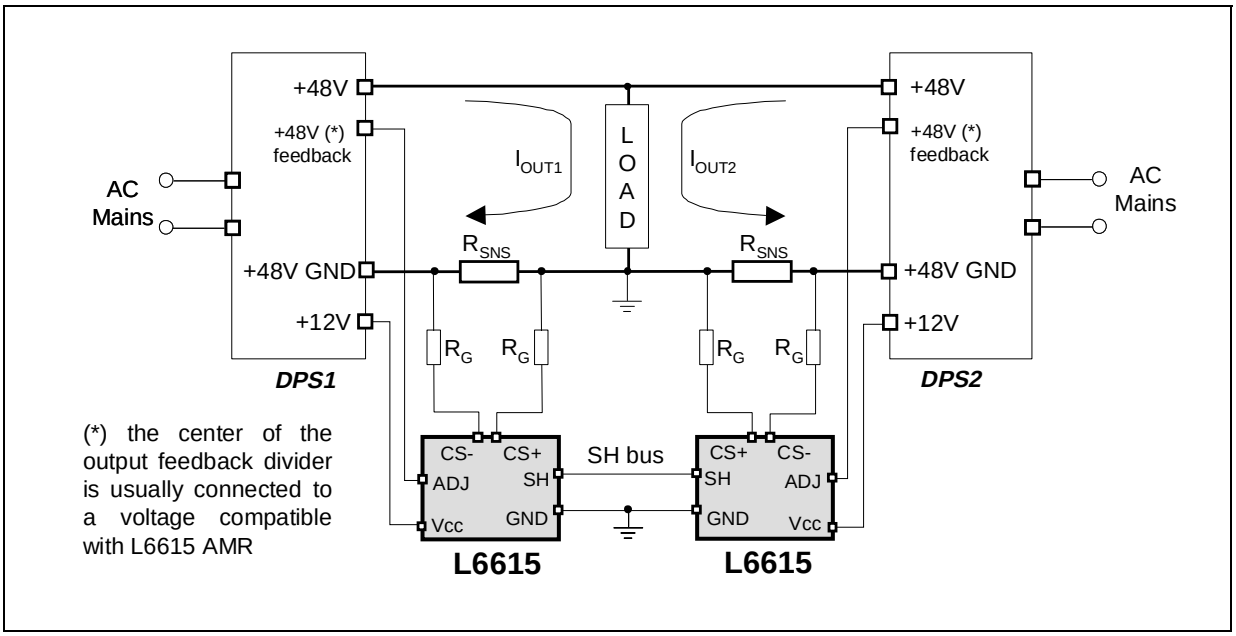


Figure 15. Distributed power system for +48V bus



In this application is inserted also a circuit for the square current limit protection in case of overcurrent (R1-Q1): being the voltage at the CGA pin directly proportional to the current carried by the relevant section, it is possible to set the CGA resistor such that, until the output current is in the right range, the CGA voltage is lower than V_{REF}+0.7. As soon as this value is overcome, then the bipolar pushes current in the feedback path, reducing the duty cycle and consequently the output voltage.

Current sharing can be required in AC to DC application like distributed power system (DPS) for telecom applications: if the output voltage is higher than the absolute maximum rating for the current sense pins (CS+ and CS-) high side sensing can not be performed unless adding other components; the current sense is performed on the ground return.

To maintain high side sensing two resistor dividers (between the edge of R_{SENSE} and ground) could be introduced to translate the sense signal in the L6615 input pin common mode range.

In fig.15 two AC-DC converters supply the same load through a +48V bus; these converters usually exhibit also a +12V auxiliary output useful to supply the L6615 whose ADJ pin works on the +48V feedback section (COMP pin and CGA pin connections are not showed) in figure 15.

7 LOW VOLTAGE BUSES

The L6615 has a "doubled" sense structure, designed to perform both high side and low side sensing: the first solution is usually considered more convenient. Actually low side sensing means to split the ground return as many times as the power supplies paralleled are: on each of these paths it is then necessary to place the sense resistor introducing a drop between the power supply ground and the common load negative reference.

The voltage at CS+ pin is read by an internal comparator and compared with a reference corresponding to the switchover threshold V_{THcs+} whose value is typically 1.6V. If such value is overcome, then the comparator triggers the High Side Amplifier (HSA); being the threshold provided by hysteresis, then the Low Side Amplifier (LSA) will be triggered as VCS+ is lower than 1.44V (typ.).

Hence V_{THcs+} defines the threshold between the operating range of LSA, (referring to fig.10) and the operating range of HSA; usually LSA is operating when the sense resistor is placed on the ground return, between the negative load terminal and the negative power supply output (fig 10.b) and HSA when the sense resistor is placed between the power supply positive output and the load.

It is however possible to perform high side sensing for applications whose output voltage is close to V_{THcs+} threshold (or even lower) exploiting the low sense internal structure (LSA).

Consider, for example an application with V_{OUT} = 1.2V and the sense resistor placed high side; the voltage at CS+:

$$V_{CS+} = V_{OUT} - \Delta V_{SENSE}$$

is lower than 1.6V so the internal comparator triggers on the LSA structure and the pin CS- sources the current I_{CS} (see paragraph "2. CURRENT SENSE SECTION"). The IC works properly because the dynamics of LSA spreads down to zero: in this case it is necessary to pay attention to the design of ADJ network.

Now consider, for example, an application with V_{OUT} =1.5V where, because of the drop across R_{SNS}, the voltage at CS+ pin could be very close to the threshold: if such voltage is overcome (start-up, load regulation, overvoltage,…) , then the HSA structure will be activated; as nominal conditions are restored, the hysteresis will then keep HSA active (unless V_{CS+} falls under the lower threshold).

8 OFFSET TRIMMING

The current sharing accuracy strongly depends on the unbalance between the relevant parameters of the paralleled sections. Each percentage point on the relevant parameters tolerance introduces a maximum error equal to the double of the tolerance.The L6615 introduces an inherent error in current sharing due to the 40mV offset at the negative input of the error amplifier; this offset is necessary to guarantee the low value of the master COMP pin.

Considering perfectly matched all other parameters, the offset introduces a percentage error equal to 4% divided by the voltage on the share bus. In particular:

$$I_{SLAVE} = I_{MASTER} \cdot \left(1 - \frac{40mA}{V_{SH}}\right)$$

Being V_{SH} directly proportional to the load current and fixed the ratio R_{CGA}/R_G, higher are the currents involved in the sharing, lower is the error.

Another error is introduced by the current sense amplifier due to its input offset whose amplitude can be ±1mV: being typically the drop across R_{SNS} about one hundred mV at full load, the offset could lead to an error of some percentage point.

Whenever the application requires very high current sharing accuracy, it is possible to correct these offsets through a triggering process, introducing a trimmer (R_K) between current sense input pins.

Referring to fig. 16, in case of high side sensing, the equations governing the circuit are:

$$\frac{V_{OUT} - V_M}{R_G} = \frac{V_M}{(1-\delta) \cdot R_K}$$

$$\frac{V_{OUT} + V_{SENSE} - V_P}{R_G} - \frac{V_P}{\delta \cdot R_K} = I_G$$

$$V_P = V_M + V_O$$

where V_O is the current sense amplifier input offset.

Solving for I_G, we get:

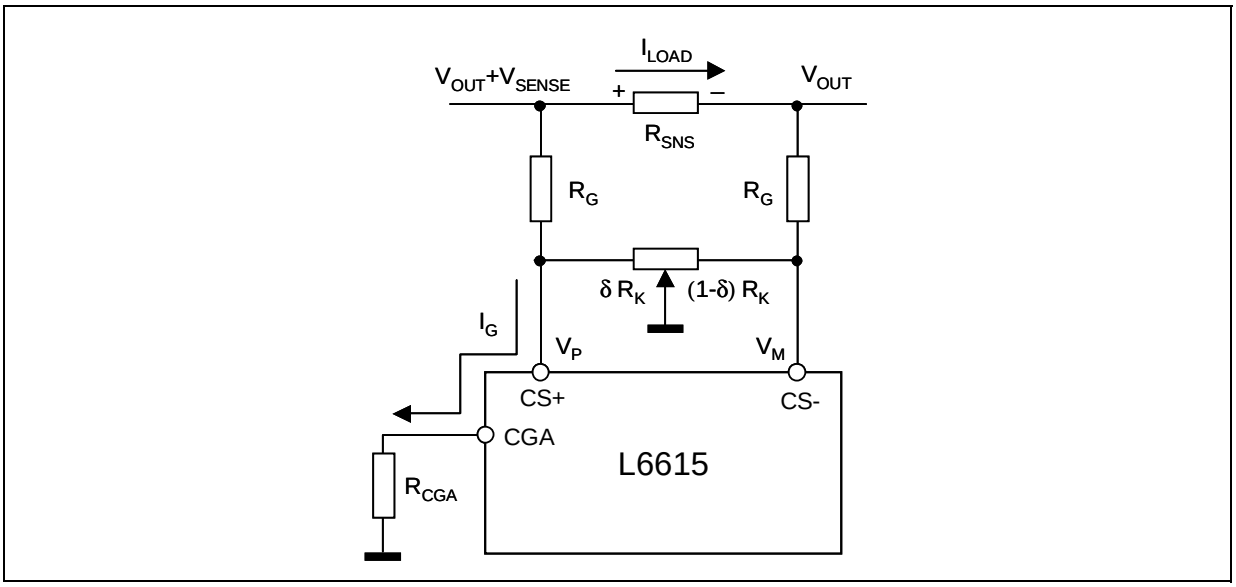
$$I_G = \frac{V_{SENSE}}{R_G} - \frac{\delta \cdot R_K + R_G}{\delta \cdot R_K \cdot R_G} \cdot V_O + V_{OUT} \cdot \frac{2 \cdot \delta - 1}{\delta \cdot [R_K \cdot (1-\delta) + R_G]}$$

Ideally I_G should be equal only to the first term: this current will be sunk by CS+ pin, internally mirrored with 1:1 ratio and sent to CGA pin.

Imposing that the sum of two latter terms is zero it is possible to find the value of δ deleting the effect of the offset:

$$\delta_{OPT} = \frac{1}{2} - \frac{2 \cdot V_{OUT} \cdot R_G - \sqrt{4 \cdot V_{OUT}^2 \cdot R_G^2 + V_O^2 \cdot R_K^2 + 4 \cdot V_O^2 \cdot R_G \cdot R_K}}{2 \cdot V_O \cdot R_K}$$

Figure 16. Offset Trimming



Because of the tolerance of the output voltage, it is not possible to delete completely the effect of the offset on CGA pin on all the allowed output voltage range: if the trimming operation is performed at $V_{OUT(MIN)}$, then on pin CGA the maximum residual voltage will be present at $V_{OUT(MAX)}$ and its value will be:

$$R_{CGA} \cdot (V_{OUT(MAX)} - V_{OUT(MIN)}) \cdot \frac{1 - 2 \cdot \delta_{OPT}}{\delta_{OPT} \cdot (R_K \cdot \delta_{OPT} - R_K - R_G)}$$

To simplify the procedure, the following step-by step process can be used:

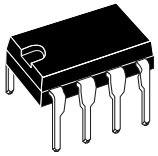
- a trimmer has to be placed between sense pins of each section: the value of the trimmer resistance must be at least one order of magnitude higher than R_G and it has to be set at one half of its range (δ=0.5);
- once the application is running at a load defined by the designer based on the required sharing accuracy, the master section has to be located;
- on the slave sections it is then necessary to operate on the trimmer to make equal the output currents.

REFERENCE

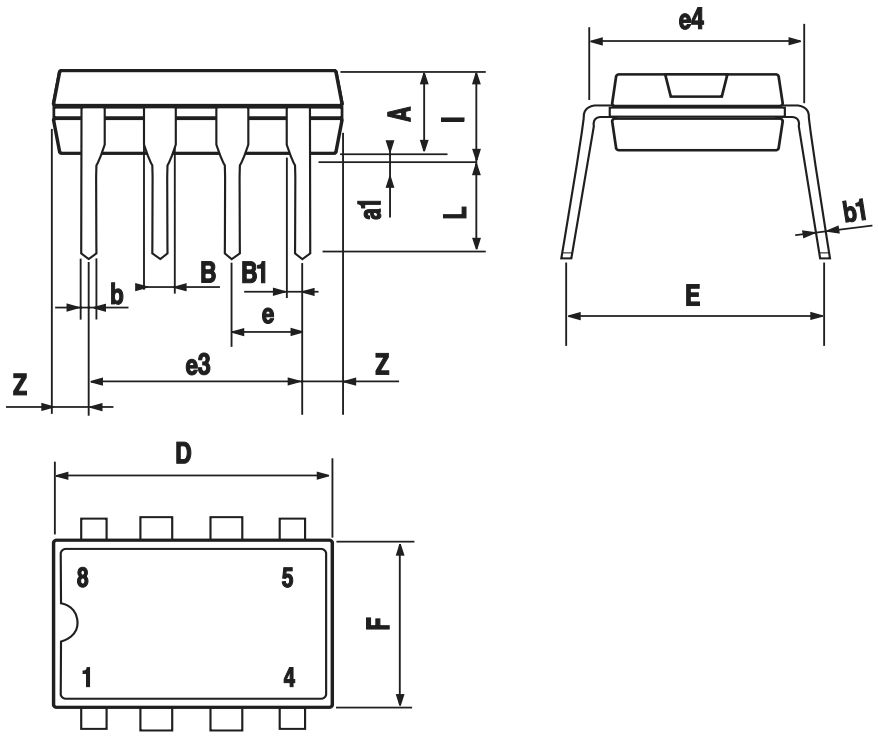
[1] "L6910 - Adjustable step down controller with synchronous rectification" (Datasheet)
[2] "L6911 - 5 bit programmable step down controller with synchronous rectification" (Datasheet

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



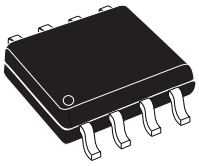
Minidip



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND MECHANICAL DATA



SO8