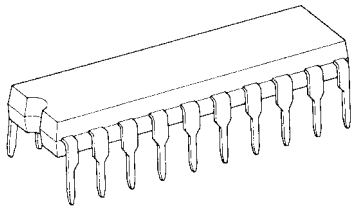
TOSHIBA Bi−CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62702P,TB62702F

10BIT SERIAL−IN PARALLEL−OUT SHIFT REGISTER / LATCH / 10SEGMENT LED DRIVERS

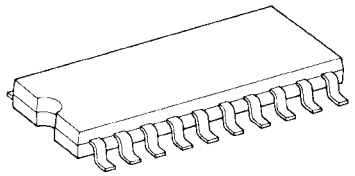
The TB62702P, TB62702F are specifically designed for 10−Segment LED Drivers and LED display. And these are monolithic integrated circuits designed to be used together with Bi−CMOS (DMOS) integrated circuit. The devices consist of a 10bit shift Register and 10bit Latches, and 10bit DMOS structures.

TB62702P



DIP20-P-300-2.54A

TB62702F



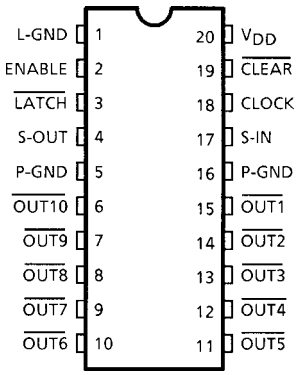
SOP20-P-300-1.27

Weight
DIP20-P-300-2.54A : 2.25 g (typ.)
SOP20-P-300-1.27 : 0.48 g (typ.)

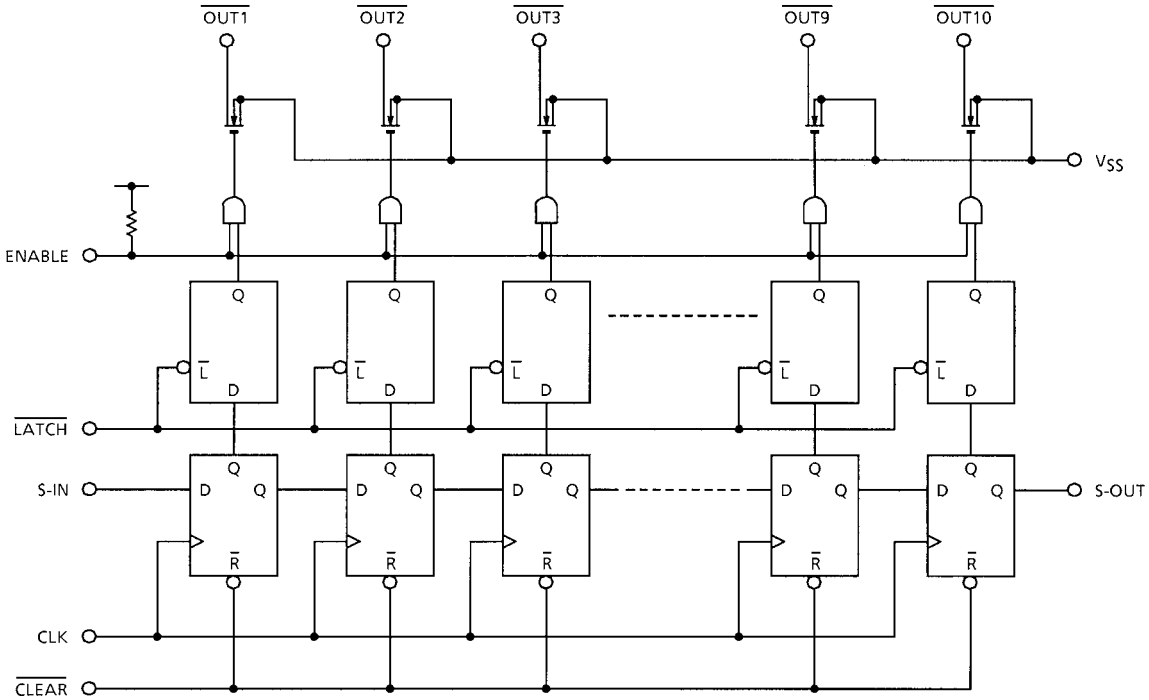
FEATURES

- 10bit serial−in parallel−out shift register / latch / 10segment LED driver (Bi−CMOS process)
- CMOS compatible inputs
- Open−drain DMOS outputs
- Low steady−state power consumption
- Serial data output for cascade operation
- Packge ; P−type DIP−20−P−300A
  F−type SOP−20−P−300

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



MAXIMUM RATINGS (Ta = 25°C, V_{SS} = 0 V)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	−0.3~7.0	V
Input Voltage		V_{IN}	−0.3~V_{DD} +0.3	V
Output Drain−Source Voltage		V_{OUT}	−0.4~30	V
Output Current		I_{OUT}	30	mA / bit
Power Dissipation	P	P_D (Note 1)	1.47	W
	F		0.96 (Note 2)	
Operating Temperature		T_{opr}	−40~85	°C
Storage Temperature		T_{stg}	−55~150	°C

Note 1: Delated above 25°C in the proportion of 11.7 mW / °C(P−type), 7.7 mW / °C(F−type).

Note 2: On Glass Epoxy (50 × 50 × 1.6mm Cu 40%)

RECOMMENDED OPERATING CONDITIONS (Ta = −40~85°C, V_{SS} = 0 V)

CHARACTERISTIC		SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage		V_{DD}	—	4.5	5	5.5	V
Input Voltage	"H" Level	V_{IH}	—	0.7 V_{DD}	—	V_{DD}	V
	"L" Level	V_{IL}	—	0	—	0.3 V_{DD}	
Output Drain−Source Voltage		V_{OUT}	—	—	—	30	V
Output Current		I_{OUT}	Duty = 100%, All output on	—	—	24	mA / ch
Power Dissipation	P	P_D	—	—	—	760	mW
	F		(Note 1)	—	—	470	

Note 1: On Glass Epoxy (50 × 50 × 1.6 mm Cu 40%)

ELECTRICAL CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 4.5~5.5 V, V_{SS} = 0 V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Output Voltage	"L" Level	V_{DS1}	—	I_{OUT} = 15 mA, Ta = 25°C	—	—	0.18	V
	"L" Level	V_{DS1}	—	I_{OUT} = 15 mA	—	—	0.27	
	"L" Level	V_{DS2}	—	I_{OUT} = 26 mA, Ta = 25°C	—	—	0.31	
	"L" Level	V_{DS2}	—	I_{OUT} = 26 mA	—	—	0.47	
Output Resistor		R_{ON}	—	Ta = 25°C, I_{OUT} = 26 mA	—	—	12	Ω
Output Leakage Current		I_{OZ1}	—	V_{OUT} = 30 V, EN = "L" 1 bit	—	—	10	μA
		I_{OZ2}	—	V_{OUT} = 30 V, EN = "L" 10 bit	—	—	±1	
Input Current		I_{IN}	—	V_{IN} = V_{DD} or V_{SS}	—	—	±1	μA
		I_{IL}	—	ENABLE, V_{IN} = V_{SS}	−27.5	−55.0	−110.0	
Output Current	"H" Level	I_{OH}	—	S−OUT V_{DS} = 4.6 V, V_{DD} = 5.0 V	−400	−600	—	μA
	"L" Level	I_{OL}	—	S−OUT V_{DS} = 0.4 V, V_{DD} = 5.0 V	400	600	—	
Input Voltage	"H" Level	V_{IH}	—	—	0.7 V_{DD}	—	V_{DD}	V
	"L" Level	V_{IL}	—	—	0	—	0.3 V_{DD}	
Operating Supply Current		I_{DD1}	—	f_{CLK} = 5 MHz NO loads, 1 bit	—	—	1500	μA
Standby Supply Current		I_{DD2}	—	—	—	—	500	

SWITCHING CHARACTERISTICS

(Ta = 25°C, V_{DD} = 5 V, V_{OUT} = 30 V, R_L = 1150 Ω, C_L = 15 pF, "H" = V_{IH}, "L" = V_{IL})

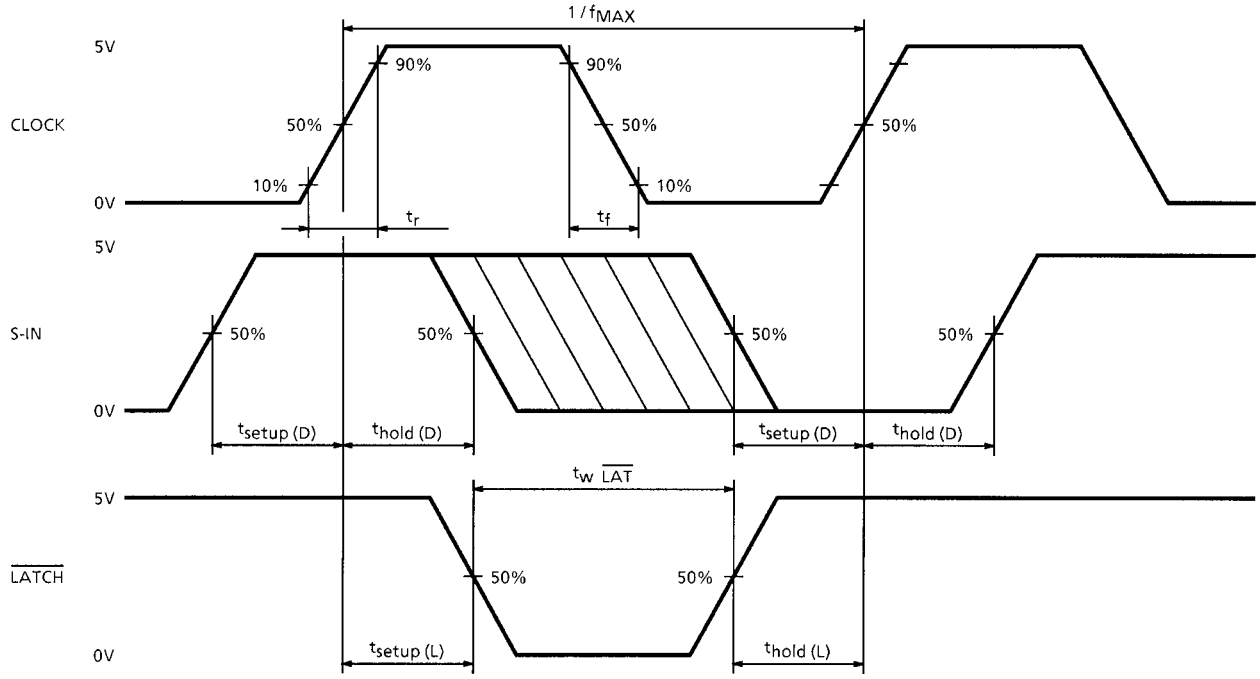
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time (Low−to−High)	CLK− $\overline{OUTn}$	t_{pLH}	$\overline{LAT}$ = "H", $\overline{CLR}$ = "H", EN = "H"	—	—	250	ns
	CLK− $\overline{OUTn}$		$\overline{LAT}$ = "H", EN = "H"	—	—	250	
	$\overline{LAT}$ − $\overline{OUTn}$		$\overline{CLR}$ = "H", EN = "H"	—	—	200	
	EN− $\overline{OUTn}$		$\overline{LAT}$ = "H", $\overline{CLR}$ = "H"	—	—	150	
Propagation Delay Time (High−to−Low)	CLK− $\overline{OUTn}$	t_{pHL}	$\overline{LAT}$ = "H", $\overline{CLR}$ = "H", EN = "H"	—	—	250	ns
	$\overline{LAT}$ − $\overline{OUTn}$		$\overline{CLR}$ = "H", EN = "H"	—	—	200	
	EN− $\overline{OUTn}$		$\overline{LAT}$ = "H", $\overline{CLR}$ = "H"	—	—	150	
Set Up Time	CLK− $\overline{LAT}$	$t_{setup\ (L)}$	—	—	—	50	ns
	CLK−S−IN	$t_{setup\ (D)}$	—	—	—	35	
Hold Time	CLK− $\overline{LAT}$	$t_{hold\ (L)}$	—	—	—	105	
	CLK−S−IN	$t_{hold\ (D)}$	—	—	—	50	
Clock Pulse Width		$t_{w\ CLK}$	—	—	—	100	ns
Latch Pulse Width		$t_{w\ \overline{LAT}}$	—	—	—	50	
Clear Pulse Width		$t_{w\ \overline{CLR}}$	—	—	—	50	
Enable Pulse Width		$t_{w\ EN}$	—	—	—	400	
Output Rise Time		t_{or}	$\overline{OUTn}$	—	—	1000	ns
		t_r	S−OUT, V_{SS} = 0V	—	—	50	
Output Fall Time		t_{of}	$\overline{OUTn}$	—	—	150	
		t_f	S−OUT, V_{SS} = 0V	—	—	50	
Maximum Clock Frequency		f_{MAX1}	Duty = 50% Cascade connected	5	8	—	MHz
		f_{MAX2}	Duty = 50%	6	12	—	

RECOMMENDED TIMING CONDITIONS (Ta = −40~85°C, V_{DD} = 4.5~5.5 V, V_{SS} = 0)

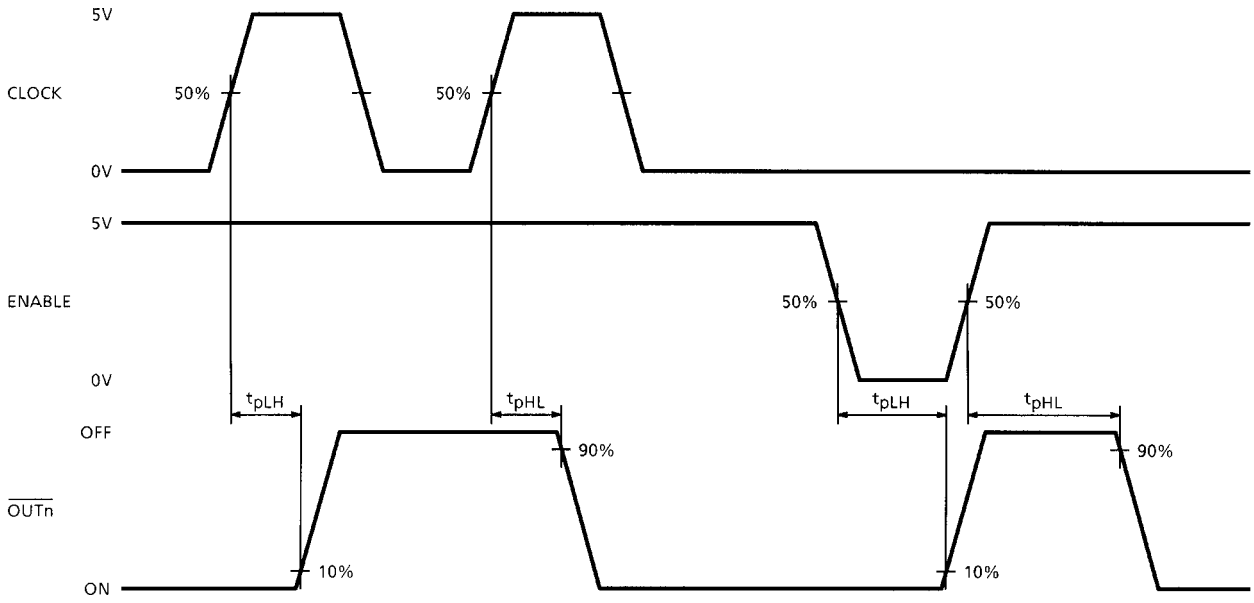
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Pulse Width	$t_{w\ CLK}$	—	100	—	—	ns
Enable Pulse Width	$t_{w\ EN}$	—	400	—	—	μs
Latch Pulse Width	$t_{w\ \overline{LAT}}$	—	100	—	—	ns
Clear Pulse Width	$t_{w\ \overline{CLR}}$	—	100	—	—	ns
Data Set Up Time	t_{setup}	—	100	—	—	ns
Data Hold Time	t_{hold}	—	150	—	—	ns

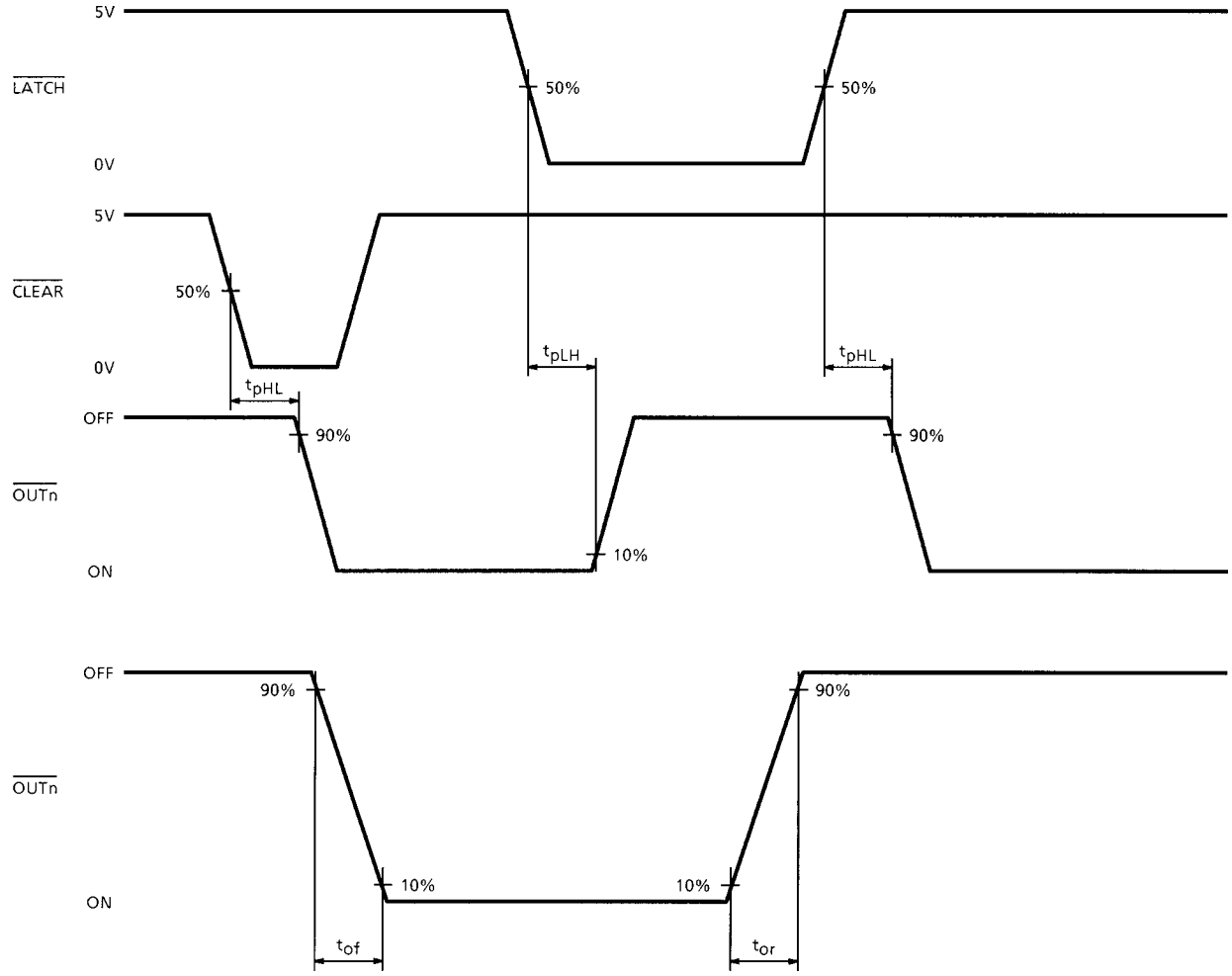
TIMING DIAGRAM

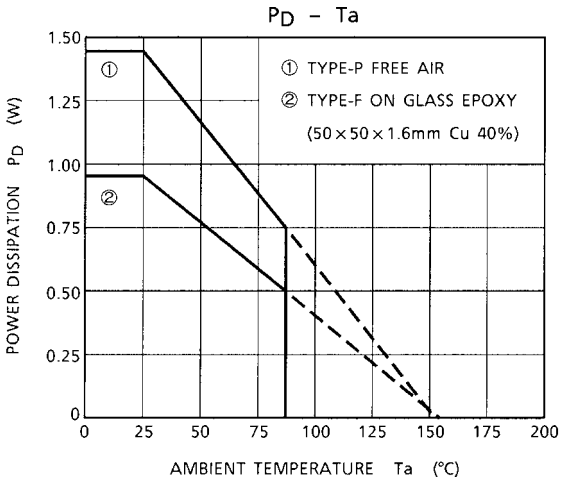
1. Input timing diagram



2. Propagation delay time





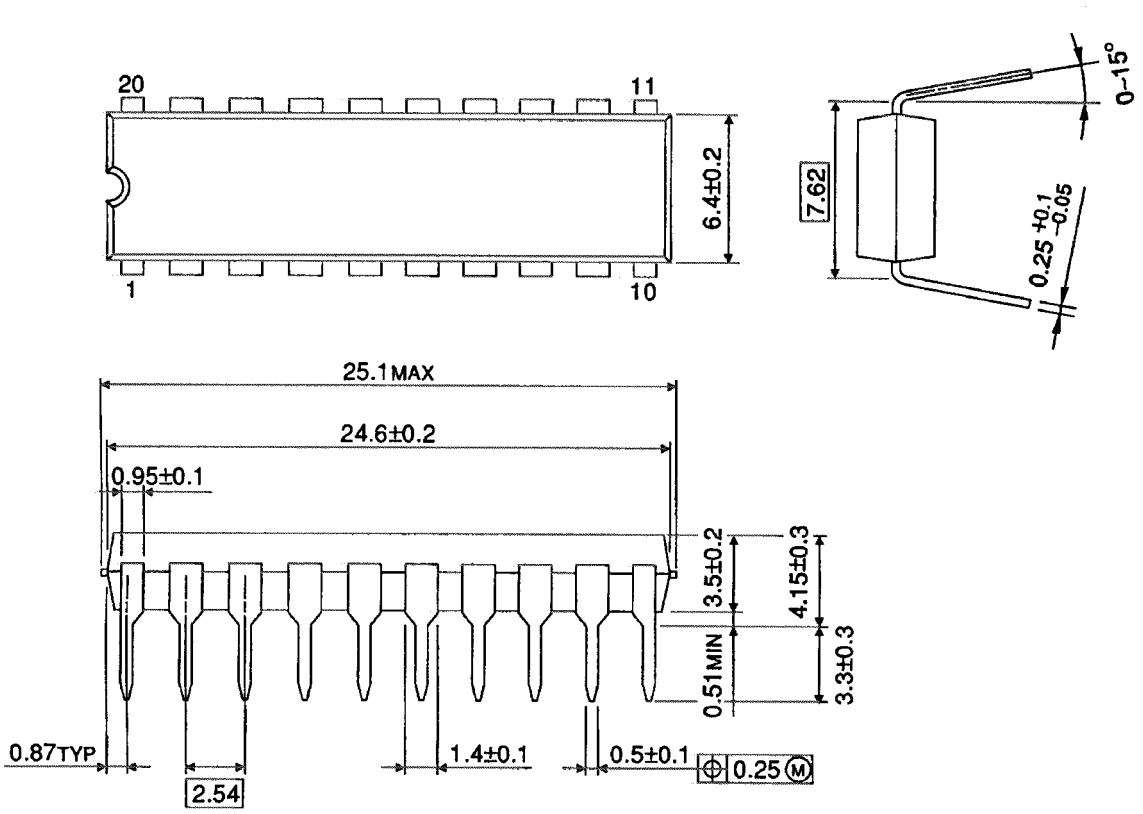


PRECUATIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND (L–GND, P–GND) line since IC may be destroyed due to short–circuit between outputs, air contamination fault, or fault by improper grounding.

Package Dimensions

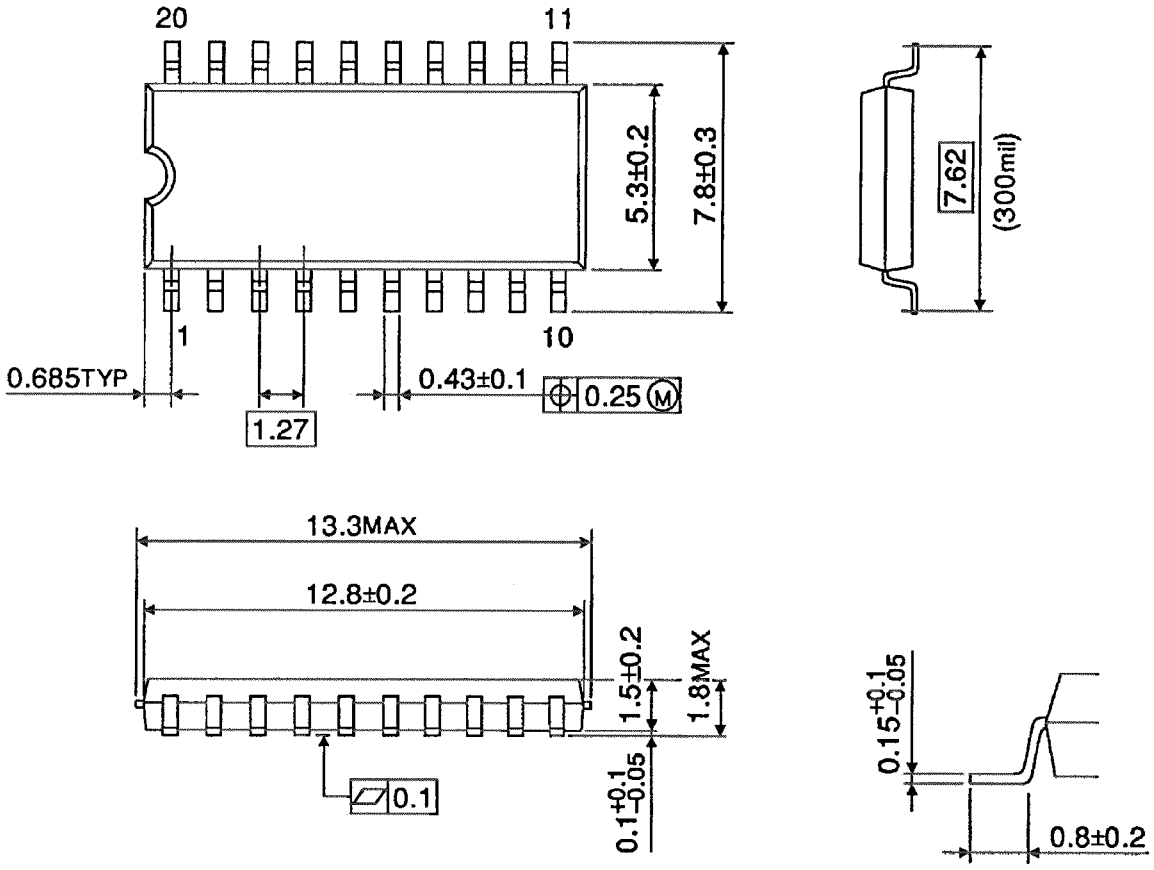
DIP20-P-300-2.54A Unit : mm



Weight: 2.25 g (typ.)

Package Dimensions

SOP20-P-300-1.27 Unit : mm



Weight: 0.48 g (typ.)

RESTRICTIONS ON PRODUCT USE

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