

MNLMC6464AM-X REV 1A1

Original Creation Date: 04/03/96

Last Update Date: 05/19/98

Last Major Revision Date: 02/08/98

PRECISION CMOS QUAD MICROPOWER OPERATIONAL AMPLIFIER

General Description

The LMC6464 is a quad low offset voltage amplifier, combining rail-to-rail Input and Output Range with very low power consumption. Performance characteristics include low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that exceeds both rails, operating at 3V, 5V, and 15V. The rail-to-rail output swing of the amplifier, for loads down to 25 KOhms, assures maximum dynamic signal range. These features, plus its low power consumption, make the LMC6464 ideally suited for battery powered applications.

The LMC6464 is an excellent upgrade for circuits using limited common-mode range amplifiers.

For designs that require higher speed, see the LMC6484 quad operational amplifier.

Industry Part Number

LMC6464

NS Part Numbers

 LMC6464AMJ-QML
 LMC6464AMWG-QML*

Prime Die

LMC6464

Controlling Document

5962-9560302QCA, QXA*

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

(Typical Unless Otherwise Noted)

- Low offset voltage. 500 μ V
- Ultra low supply current. 23 μ A/Amplifier
- Operates from 3V to 15V single supply.
- Low input bias current. 150fA typ.
- Rail-to-Rail Output Swing within 10mV of rail, Vs = 5V, 25k Ohm load.

Applications

- Battery Operated Circuits.
- Transducer Interface Circuits.
- Portable Communications Devices.
- Medical Application.
- Battery Monitoring.

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (V+ - V-)	16V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V+)+0.3V, (V-)-0.3V
Current at Input Pin (Note 6)	±5mA
Current at Output Pin (Note 3, 5)	±30mA
Current at Power Supply Pin	40mA
Junction Temperature (Note 3)	150 C
Power Dissipation (Note 2)	6mW
Operating Temperature Range	-55 C ≤ TA ≤ +125 C
Thermal Resistance (Note 7)	
ThetaJA	
14-Pin CERAMIC DIP	(Still Air) 74 C/W
	(500LF/Min Air flow) 37 C/W
14-Pin CERAMIC SOIC	(Still Air) 132 C/W
	(500LF/Min Air flow) 78 C/W
ThetaJC	
14-Pin CERAMIC DIP	8 C/W
14-Pin CERAMIC SOIC	8 C/W
Package Weight (Typical)	TBD
Storage Temperature Range	-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)	260 C
ESD Tolerance (Note 4)	2kV

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{dmax} = (T_{jmax} - TA)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 C. Output currents in excess of ±30mA over long term may adversely affect reliability.

Note 4: Human body model, 1.5k Ohms in series with 100pF.

Note 5: Do not connect output to V+, when V+ is greater than 13V or reliability will be adversely affected.

(Continued)

Note 6: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 7: All numbers apply for packages soldered directly into a PC board.

Recommended Operating Conditions

(Note 1)

Supply Voltage

3.0 <- V+ <- 15.5V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS: 5 Volt

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_+ = 5V$, $V_- = 0V$, $V_{cm} = V_o = V_+/2$, $R_l = > 1M$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage					0.5	mV	1
						1.4	mV	2, 3
Iib	Input Bias Current		4			25	pA	1
			4			100	pA	2, 3
Iio	Input Offset Current		4			25	pA	1
			4			100	pA	2, 3
CMRR	Common Mode Rejection Ratio	$0V \leq V_{cm} \leq 5.0V$			70		dB	1
					67		dB	2, 3
Vcm	Input Common-Mode Voltage Range	For CMRR $\geq$ 50 dB			5.25	-0.10	V	1
					5.00	0.00	V	2, 3
Vop	Output Swing	$R_l = 100K \text{ Ohms to } V_+/2$			4.990	0.010	V	1
					4.980	0.020	V	2, 3
		$R_l = 25K \text{ Ohms to } V_+/2$			4.975	0.020	V	1
					4.965	0.035	V	2, 3
Icc	Supply Current	$V_o = V_+/2$				110	μA	1
						140	μA	2, 3
Isc	Output Short Circuit Current	Sourcing, $V_o = 0V$			19		mA	1
					15		mA	2, 3
		Sinking, $V_o = 5V$			22		mA	1
					17		mA	2, 3

Electrical Characteristics

DC PARAMETERS: 15 Volt

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_+ = 15V$, $V_- = 0V$, $V_{cm} = V_o = V_+/2$, $R_l > 1M$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage					1.8	mV	1
						2.3	mV	2, 3
Iib	Input Bias Current		4			25	pA	1
			4			100	pA	2, 3
Iio	Input Offset Current		4			25	pA	1
			4			100	pA	2, 3
CMRR	Common Mode Rejection Ratio	$0V \leq V_{cm} \leq 15.0V$			70		dB	1
					67		dB	2, 3
Vcm	Input Common Mode Voltage Range	For CMRR $\geq 50dB$			15.25	-0.15	V	1
					15.00	0.00	V	2, 3
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V_+ \leq 15V$, $V_- = 0V$, $V_o = 2.5V$			70		dB	1
					67		dB	2, 3
-PSRR	Negative Power Supply Rejection Ratio	$-5V \leq V_- \leq -15V$, $V_+ = 0V$, $V_o = -2.5V$			70		dB	1
					67		dB	2, 3
Vop	Output Swing	$R_l = 100K \Omega$ to $V_+/2$			14.975	0.025	V	1
					14.965	0.035	V	2, 3
		$R_l = 25K \Omega$ to $V_+/2$			14.900	0.050	V	1
					14.850	0.150	V	2, 3
Icc	Supply Current	$V_o = V_+/2$				120	uA	1
						140	uA	2, 3
Isc	Output Short Circuit Current	Sourcing, $V_o = 0V$			24		mA	1
					17		mA	2, 3
		Sinking, $V_o = 12V$	1		55		mA	1
			1		45		mA	2, 3

Electrical Characteristics

DC PARAMETERS: 15 Volt (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_+ = 15V$, $V_- = 0V$, $V_{cm} = V_o = V_+/2$, $R_l > 1M$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Av	Large Signal Voltage Gain	Sourcing, $R_l = 100K \text{ Ohms}$	2		110		dB	1
			2		80		dB	2, 3
		Sinking, $R_l = 100K \text{ Ohms}$	2		100		dB	1
			2		70		dB	2, 3
		Sourcing, $R_l = 25K \text{ Ohms}$	2		110		dB	1
			2		70		dB	2, 3
		Sinking, $R_l = 25K \text{ Ohms}$	2		95		dB	1
			2		60		dB	2, 3

DC PARAMETERS: 3 Volt

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_+ = 3V$, $V_- = 0V$, $V_{cm} = V_o = V_+/2$, $R_l > 1M$

Vio	Input Offset Voltage				0.8		mV	1
					1.7		mV	2
Iib	Input Bias Current		4		25		pA	1
			4		100		pA	2
Iio	Input Offset Current		4		25		pA	1
			4		100		pA	2, 3
CMRR	Common Mode Rejection Ratio	$0V \leq V_{cm} \leq 3.0V$			60		dB	1
					57		dB	2, 3
Vcm	Input Common Mode Voltage Range	For $CMRR \geq 50 \text{ dB}$			3.0	0.0	V	1
					2.9	0.1	V	2, 3
Vop	Output Swing	$R_l = 25K \text{ Ohms to } V_+/2$			2.9	0.10	V	1
					2.8	0.15	V	2, 3
Icc	Supply Current	$V_o = V_+/2$			110		uA	1
					140		uA	2, 3
Isc	Output Short Circuit Current	Sourcing, $V_o = 0V$			8		mA	1
					6		mA	2, 3
		Sinking, $V_o = 3V$			23		mA	1
					17		mA	2, 3

Electrical Characteristics

AC PARAMETERS:15 Volts

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_+ = 15V$, $V_- = 0V$, $V_{cm} = V_o = V_+/2$, $R_l > 1M$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Sr	Slew Rate		3		15		V/mS	4
			3		7		V/mS	5, 6
Gbw	Gain-Bandwidth				60		KHz	4
					45		KHz	5, 6

Note 1: Do not short circuit output to V_+ , when V_+ is greater than 13V or reliability will be adversely affected.

Note 2: $V_{cm}=7.5V$ and R_l connected to 7.5V. For Sourcing tests, $7.5V \leq V_o \leq 11.5V$. For Sinking tests, $3.5V \leq V_o \leq 7.5V$.

Note 3: Device configured as a voltage follower, with a 10V input step. For Positive Slew, V_{in} swing is 2.5V to 12.5V, V_{out} is measured between 6.0V and 9.0V. For Negative Slew, V_{in} swing is 12.5V to 2.5V, V_{out} is measured between 9.0V and 6.0V.

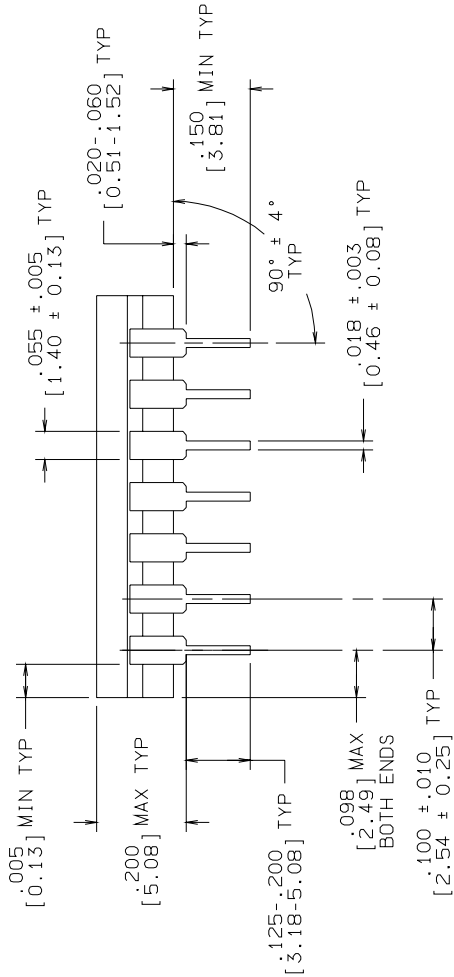
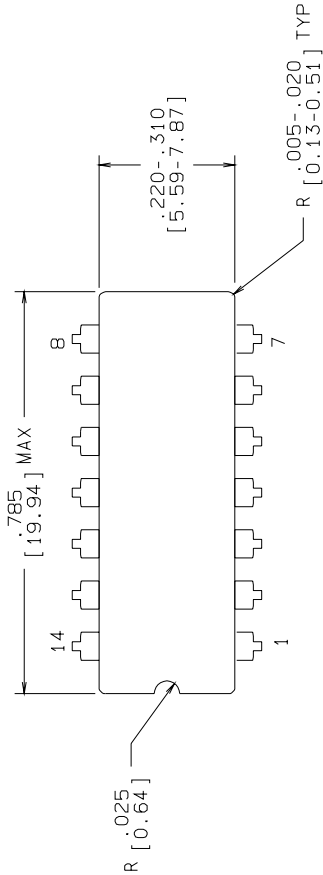
Note 4: Limits are dictated by testing limitations and not device performance.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06087HRB4	CERDIP (J), 14 LEAD (B/I CKT)
06213HRA3	CERAMIC SOIC (WG), 14LD (B/I CKT)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000116A	CERDIP (J), 14 LEAD (PIN OUT)
P000360A	CERAMIC SOIC (WG), 14 LEAD (PINOUT)
WG14ARC	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.

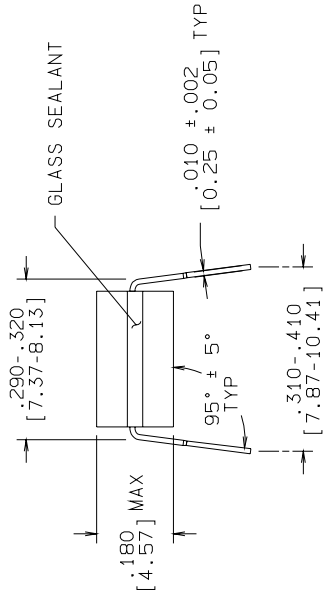
R E V I S I O N S				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/



CONTROLLING DIMENSION: INCH

NOTES: UNLESS OTHERWISE SPECIFIED

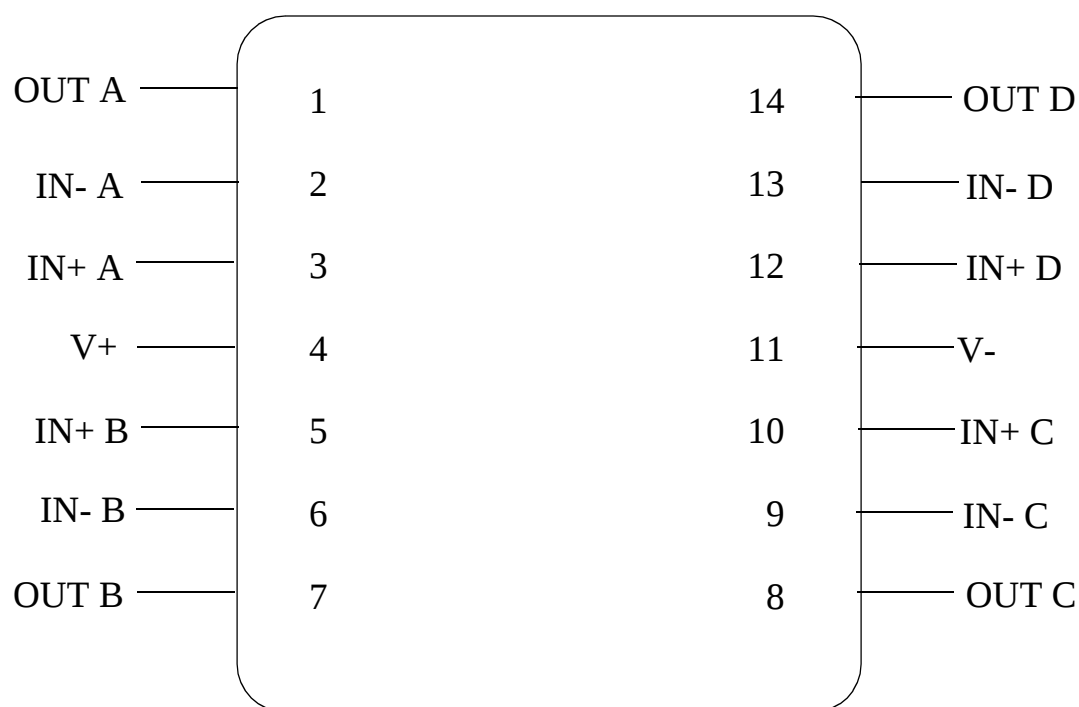
1. LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.



MIL/AERO MIL-M-38510
CONFIGURATION CONTROL CONFIGURATION CONTROL

APPROVALS		DATE	 NATIONAL SEMICONDUCTOR CORPORATION			
DRAWN  T. LEQUANG		09/15/93	2900 Semiconductor Drive, Santa Clara, CA 95052-8090			
DFTG. CHK.			CERDIP (J) , 14 LEAD ,			
ENGR. CHK.						
APPROVAL						
 PROJECTION			SCALE	SIZE	DRAWING NUMBER	REV
			N/A	B	MKT-J14A	H
			DO NOT SCALE DRAWING		SHEET 1 OF 1	

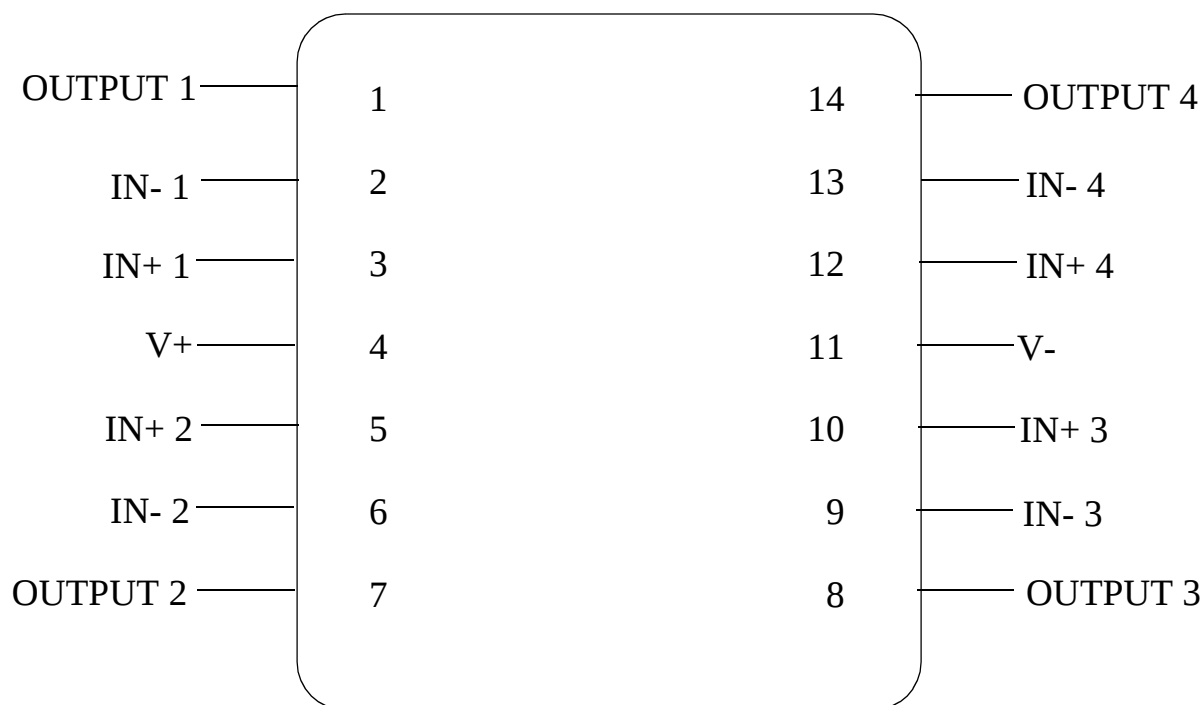
CERDIP (J) ,
14 LEAD,



LMC6464AMJ
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000116A



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LMC6464AMWG
14 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000360A



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Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A1	M0002890	05/19/98	Rose Malone	Changed MDS: MNLMC6464AM-X Rev. 0A0 to MNLMC6464AM-X Rev. 1A1. Updated subgroups to match SMD. Updated graphics the WG package. Added Package Weight Title. Updated B/I Ckt. Rev. adding a 0 in front of number.