SC1403
Mobile Multi-Output PWM Controller with Virtual Current Sense™

Description

The SC1403 is a multiple-output power supply controller designed to power battery operated systems. The SC1403 provides synchronous rectified buck converter control for two (3.3 V and 5 V) power supplies. An efficiency of 95% can be achieved for the two supplies. The SC1403 uses Semtech's proprietary Virtual Current Sense™ technology along with external error amplifier compensation to achieve enhanced stability and DC accuracy over a wide range of output filter components while maintaining fixed frequency operation. The SC1403 also provides a linear regulator for system housekeeping. The 5 V linear regulator takes its input from the battery; for efficiency, the output is switched to the 5V output when available.

Control functions include: power up sequencing, soft start, power-good signaling, and frequency synchronization. Line and load regulation is to +/-1% of the output voltage. The internal oscillator can be adjusted to 200 kHz or 300 kHz or synchronized to an external clock. The MOSFET drivers provide >1A peak drive current for fast MOSFET switching.

The SC1403 includes a PSAVE# input to select pulse skipping mode for high efficiency at light load, or fixed frequency mode for low noise operation.

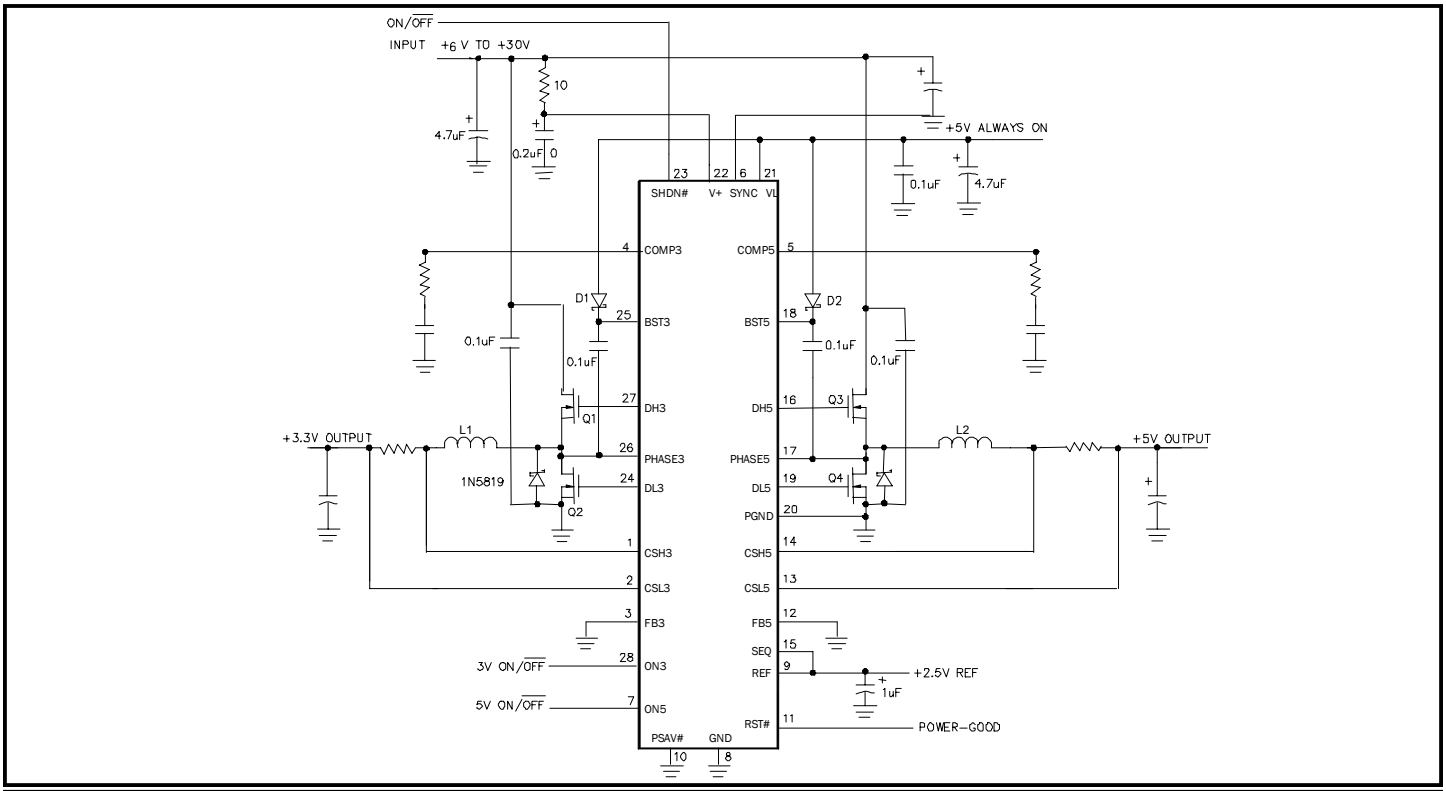
Features

- 3.3V and 5V dual synchronous outputs, resistor programmable to 2.5V
- Fixed frequency or PSAVE for maximum efficiency over wide load current range
- 5V / 50mA linear regulator
- Virtual Current Sense ™ for enhanced stability
- Accurate low loss current limiting
- Out of phase switching reduces input capacitance requirements
- External compensation supports wide range of output filter components
- Programmable power-up sequence
- Power good output
- Output overvoltage & overcurrent protection with output undervoltage shutdown
- 4µA typical shutdown current
- 6mW typical quiescent power

Applications

- Notebook and subnotebook computers
- Automotive electronics
- Desktop DC-DC converters

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage, V+ to GND	V_{IN}	-0.3 to +30	V
Boost Voltages, BST3, BST5, to GND		-0.3 to +36	V
PGND to GND		± 0.3	V
BST3 to PHASE3; BST5 to PHASE5; CSL5, CSH5 to GND; CSL3, CSH3 to GND		-0.3 to +6 DC -2.0 to +7 Transient , 100nS	V
REF, SYNC, SEQ, PSAVE#, ON5, RESET#, VL, FB3, FB5, COMP3, COMP5 to GND		-0.3V to +6	V
ON3, SHDN# to GND		-0.3V to (V+ + 0.3V)	V
VL, REF Short to GND		Continuous	
REF Current		+5	mA
VL Current		+50	mA
Lead Temperature (Soldering) 10 seconds	T_{LEAD}	+300	°C
Storage Temperature Range	T_{STG}	-65 to +200	°C
Junction Temperature Range	T_J	+150	°C

Electrical Characteristics

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A =-40 to 85°C. Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
MAIN SMPS CONTROLLERS					
Input Voltage Range		6.0		30.0	V
3.3V Output Voltage in Adjustable Mode	V+ = 6.0 to 30V, CSL3 tied to FB3, 3V Load = 0A to current limit	2.45	2.5	2.55	V
3.3V Output Voltage in Fixed Mode	V+ = 6.0 to 30V, FB3 = 0V, 3V Load = 0A to current limit	3.23	3.3	3.37	V
5V Output Voltage in Adjustable Mode	V+ = 6.0 to 30V, CSL5 tied to FB5, 5V Load = 0A to current limit	2.45	2.5	2.55	V
5V Output Voltage in Fixed Mode	V+ = 6.0 to 30V, FB5 = 0V, 5V Load = 0A to current limit	4.9	5.0	5.1	V
Output Voltage Adjust Range	Either SMPS	REF		5.5	V
Adjustable Mode Threshold Voltage		0.5	0.8	1.1	V
Load Regulation	Either SMPS, 0A to current limit		-0.4		%
Line Regulation	Either SMPS, 6.0V < V+ <30; PSAVE# = V_L		0.05		%/V

Electrical Characteristics (Cont.)

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A=-40 to 85°C. Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Current-Limit Threshold	CSH5 -CSL5, CSH3 -CSL3	40	50	70	mV
Negative OC limit Threshold			-50		mV
Zero Crossing Threshold	CSH5 - CSL5, CSH3 - CSL; PSAVE# = 0V, not tested		5		mV
Soft-Start Ramp Time	From enable to 95% full current limit with respect to f_{OSC}		512		clks
Oscillator Frequency	SYNC = VL SYNC = 0V	220 170	300 200	380 230	kHz
Maximum Duty Factor	SYNC = VL SYNC = 0V	92 94	94 96		%
SYNC Input High Pulse	Not Tested	300			ns
SYNC Input Low Pulse Width	Not Tested	300			
SYNC Rise/Fall Time	Not Tested			200	
SYNC Input Frequency Range		240		350	kHz
Current-Sense Input Leakage Current	CSH3 = CSH5 = 5.5V		3	10	µA
ERROR AMP					
Closed Loop Gain			18		V/V
Closed Loop Bandwidth			8		MHz
Out Resistance	COMP3, COMP5	15	25	35	kΩ
Offset Voltage	Internal FB - REF		±2		mV
INTERNAL REGULATOR AND REFERENCE					
VL Output Voltage	SHDN# = V+; 6V < V+ <30V; 0mA <I_{LOAD} <50mA; ON3 = ON5 = 0V	4.6		5.2	V
VL Undervoltage Lockout Fault Threshold	Falling edge, hysteresis = 0.7V	3.5	3.7	4.0	
VL Switchover Lockout	Switchover at startup		4.5		
REF Output Voltage	No external load	2.45	2.5	2.55	
REF Load Regulation	0µA < I_{LOAD} < 50µA			12.5	mV
	0mA < I_{LOAD} < 5mA			50	

Electrical Characteristics (Cont.)

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A =-40 to 85°C. Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
REF Sink Current			10		µA
REF Fault Lockout Voltage	Falling edge	1.8		2.2	V
V+ Operating Supply Current	VL switched over to VOUT5, both SMPS on, lLoad3 = 0A, lLoad5 = 0A		10	50	µA
V+ Standby Supply Current	V+ = 6V to 30V, SMPS off, includes current into SHDN#		180		
V+ Shutdown Supply Current	V+ = 6V to 30V, SHDN# = 0V		4	10	
Quiescent Power Consumption	SMPS enabled, FB3 = FB5 = 0V, No Load on SMPS		6.0		mW
FAULT DETECTION					
Overvoltage Trip Threshold	With respect to unloaded output voltage	7	10	15	%
Overvoltage-Fault Propagation Delay	Output driven 2% above overvoltage trip V_{TH}		1.5		µs
Output Undervoltage Threshold	With respect to unloaded output voltage	65	75	85	%
Output Undervoltage Lockout Time	From each SMPS enabled, with respect to f_{OSC}	5000	6144	7000	clks
Thermal Shutdown Threshold	Typical hysteresis = +10°C		150		°C
RESET#					
RESET# Trip Threshold	With respect to unloaded output voltage, falling edge; typical hysteresis = 1%	-13	-10	-7	%
RESET# Propagation Delay	Falling edge, output driven 2% below RESET# trip threshold		1.5		µs
RESET# Delay Time	With respect to f_{OSC}	27,000	32,000	37,000	clks
INPUTS AND OUTPUTS					
Feedback Input Leakage Current	FB3, FB5 = 2.6V			+1	µA
Logic Input Low Voltage	ON3, PSAVE#, ON5, SHDN#, SYNC (SEQ = 0V or VL)			0.6	V
Logic Input High Voltage	ON3, PSAVE#, ON5, SHDN#, SYNC (SEQ = 0V or VL)	2.4			V

Electrical Characteristics (Cont.)

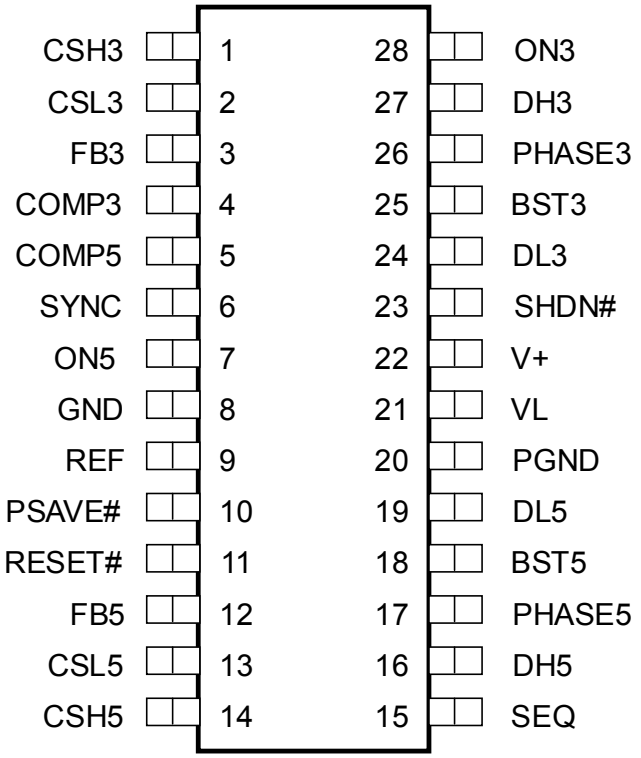
Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A =-40 to 85°C. Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Leakage Current	ON3, PSAVE#, ON5, SHDN#, SYNC (SEQ = 0V or VL)			+1	µA
Logic Output Low Voltage	RESET#, ISINK = 4mA			0.4	V
Logic Output High Current	RESET# = 3.5V	1			mA
ON5 Pull-Down Resistance	ON5, ON3 = 0V, SEQ = REF		100		Ω
Gate Driver Sink/Source Current	DL3, DH3, DL5, DH5, forced to 2.5V		1		A
Gate Driver On-Resistance	High or low		1.5	7	Ω
Non-Overlap Threshold	PHASE3, PHASE5, DL3, or DL5		1.0		V
Non-Overlap Delay	Falling edge of DH to rising edge of DL Falling edge of DL to rising edge of DH (1V threshold on DH and DL, no capacitance on DL or DH)	10 35	17 75	25 115	nsec nsec

Note:
(1) This device is ESD sensitive. Use of standard ESD handling precautions required.

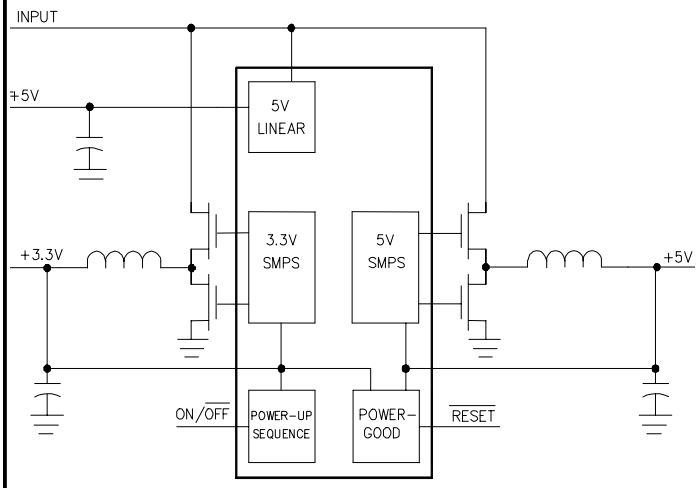
Pin Configuration

TOP VIEW



(28 Pin TSSOP)

Block Diagram



Ordering Information

Device	Package	Temp. (T_A)
SC1403ITSTR	TSSOP-28	-40 - +85°C

Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	CSH3	Current limit sense input for 3.3 V SMPS. Connect to the inductor side of a current sense resistor .
2	CSL3	Output voltage sense input for 3.3 V SMPS. Connect to the output side of a current sense resistor .
3	FB3	Feedback Input for the 3.3 V SMPS; regulates at FB3 = REF (approx. 2.5 V) in adjustable mode. FB3 selects the 3.3 V fixed output voltage setting when tied to GND. Connect FB3 to a resistor divider for adjustable output mode.
4	COMP3	The output of the error amplifier for 3.3V SMPS.
5	COMP5	The output of the error amplifier for 5.0V SMPS.
6	SYNC	Oscillator Synchronization and Frequency Select. Tie to VL for 300 kHz operation; tie to GND for 200 kHz. Driven externally to SYNC between 240 kHz and 350 kHz.
7	ON5	5V ON/OFF Control Input.
8	GND	Low noise Analog Ground and Feedback reference point.
9	REF	2.5 V Reference Voltage Output. Bypass to GND with 1 µF minimum.
10	PSAVE#	Logic Control Input that disables PSAVE Mode when high. Connect to GND for normal use.
11	RESET#	Active Low Timed Reset Output. RESET# swings GND to VL. Goes high after a fixed 32,000 clock cycle delay following power up.
12	FB5	Feedback Input for 5 V SMPS; regulates at FB5 = REF (approx. 2.5 V) in adjustable mode. FB5 selects the 5 V fixed output voltage setting when tied to GND. Connect FB5 to a resistor divider for adjustable output mode.
13	CSL5	Output voltage sense input for 5 V SMPS. Connect to the output side of a current sense resistor .
14	CSH5	Current limit sense input for 5 V SMPS. Connect to the inductor side of a current sense resistor .
15	SEQ	Input that selects SMPS sequence for RESET#.
16	DH5	Gate Drive Output for the 5 V, high side N-Channel switch.
17	PHASE5	Switching Node (inductor) connection.
18	BST5	Boost capacitor connection for high side gate drive.

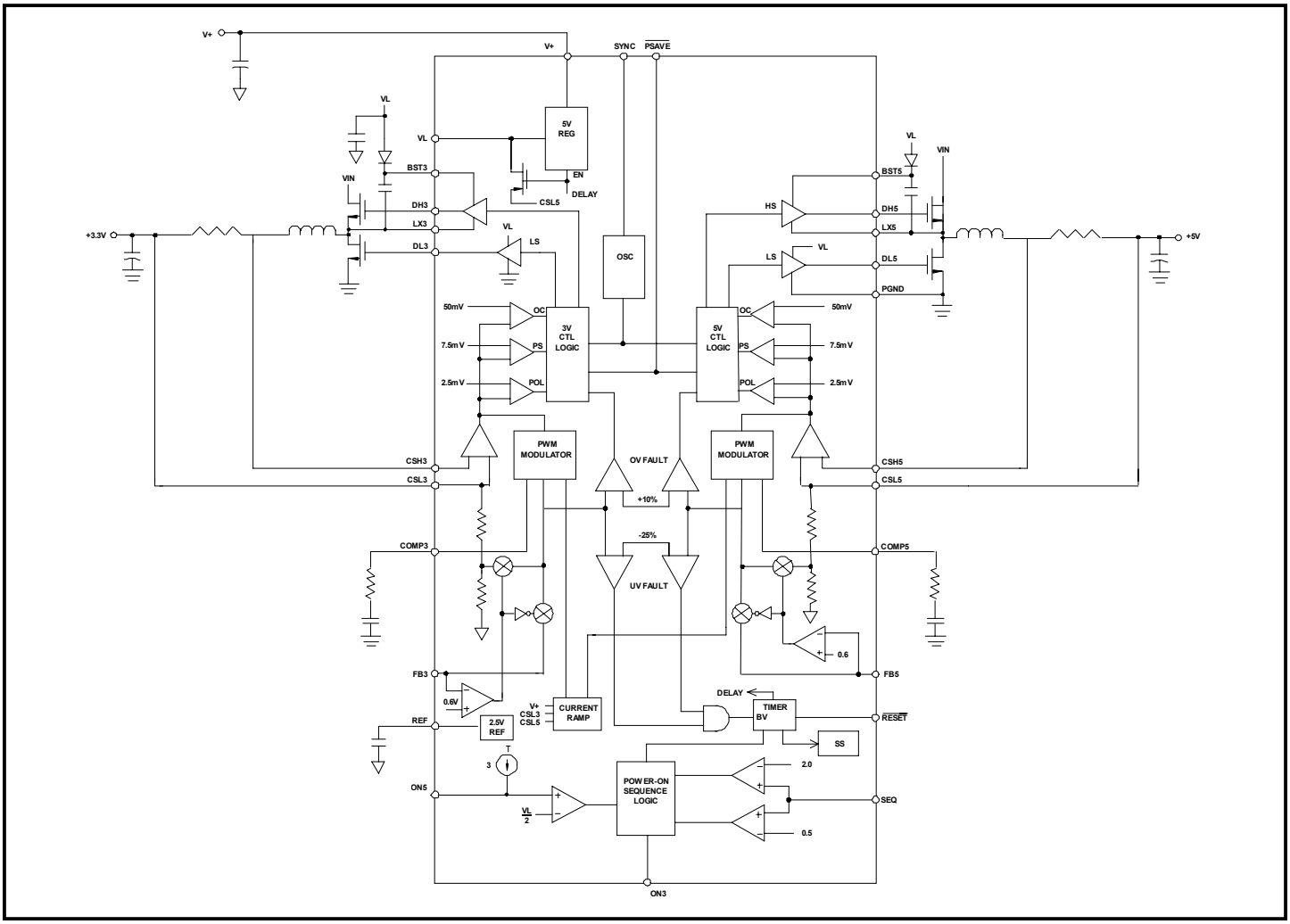
Note: All logic level inputs and outputs are open collector TTL compatible.

Pin Descriptions (Cont.)

Pin #	Pin Name	Pin Function
19	DL5	Gate Drive Output for the low side synchronous rectifier MOSFET.
20	PGND	Power Ground.
21	VL	5 V Internal Linear Regulator Output.
22	V+	Battery Voltage Input.
23	SHDN#	Shutdown Control Input, active low.
24	DL3	Gate Drive Output for the low side synchronous rectifier MOSFET.
25	BST3	Boost Capacitor Connection for high side gate drive.
26	PHASE3	Switching Node (inductor) Connection.
27	DH3	Gate Drive Output for the 3.3 V, high side N-Channel switch.
28	ON3	ON/OFF Control Input.

Note: All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Functional Information

Detailed Description

The SC1403 is a versatile multiple-output power supply controller designed to power battery operated systems. Out of phase switching design is adopted to improve signal quality and reduce input RMS current, therefore reducing size of input filter inductor and capacitors. The SC1403 provides synchronous rectified buck control in fixed frequency forced-continuous mode and hysteretic PSAVE mode for two switching power supplies over a wide load range. The two switchers have on-chip preset output voltage of 5.0V and 3.3V. An external resistor divider can be used to set the switcher outputs from 2.5V to 5.5V. The control and fault monitoring circuitry associated with each PWM controller includes digital softstart, turn-on sequencing, voltage error amplifier with built-in slope compensation, pulse width modulator, power save, over-current, over-voltage and under-voltage fault protection. One linear regulator and a precision reference voltage are also provided by the SC1403. The 5V/50mA linear regulator takes input from the battery to power the gate drivers, however to improve efficiency, the 5V switcher output is used instead when available. Semtech's proprietary Virtual Current Sense™ provides greater advantages in the aspect of stability and signal to noise ratio than the conventional current sense method.

PWM control

There are two separate PWM control blocks for the 3V and 5V switchers. They are out-of-phase with each other. The interleaved topology offers greater advantage over in-phase solutions. It reduces steady state input filter requirements by reducing current drawn from the filter capacitors. To avoid both switchers switching at the same instance, there is a built-in delay between the on-time of the 3.3V switcher and 5V switcher, the amount of which depends on the input voltage (see Out-of-Phase Switching). The PWM provides two modes of control over the entire load range. The SC1403 operates in forced continuous conduction mode as a fixed frequency peak current mode controller with falling edge modulation. Current sense is done differently than that in the conventional peak current mode control. Semtech's proprietary Virtual Current Sense™ emulates the necessary inductor current information for proper functioning of the IC. In order to accommodate a wide range of output filters, a COMP pin is also available for compensating the error amplifier externally. A nominal gain of 18 is used in the error amplifier to further improve the system loop gain response and the output transient behavior. When the switcher is operating in continuous conduction mode, the high-side MOSFET is turned on at the beginning of each switching cycle. It is turned off when the desired duty cycle is reached. Active shoot-through protection delays the turn-on of the lower MOSFET until the phase node drops below 2.5V. The low-side MOSFET remains on until the beginning of the next switching cycle. Again, active shoot-through protection ensures that the gate to the low-side MOSFET has dropped low before the high-side MOSFET is turned on. Under light load conditions when the $\overline{\text{PSAVE}}$ pin is low, the SC1403 operates as a hysteretic controller in the discontinuous conduction mode to reduce its switching frequency and switching bias current. The switching of the output MOSFET does not depend on a given oscillator frequency, but on the hysteretic FB trip voltage set around the reference. When entering PSAVE mode, if the minimum (valley) inductor current measured across the CSH and CSL pins is below the PSAVE threshold for four switching cycles, the virtual current sensing circuitry is shutdown and PWM switches from forced continuous to hysteretic mode. If the minimum (valley) inductor current is above the threshold for four switching cycles, PWM control changes from hysteretic to forced continuous mode. The SC1403 provides built-in hysteresis to prevent chattering between the two modes of operation.

Gate Drive / Control

The gate drivers on the SC1403 are designed to switch large MOSFETs up to 350KHz. The high-side gate driver is required to drive the gates of high-side MOSFET above the V+ input. The supply for the gate drivers is generated by charging a boostrap capacitor from the VL supply when the low-side driver is on. Monitoring circuitry ensures that the bootstrap capacitor is charged when coming out of shutdown or fault conditions where the bootstrap capacitor may be depleted. In continuous conduction mode, the low-side driver output that controls the synchronous rectifier in the power stage is on when the high-side driver is off. Under light load conditions when $\overline{\text{PSAVE}}$ pin is low, the inductor ripple current will approach the point where it reverses polarity. This is detected by the low-side driver control and the synchronous rectifier is turned off before the current reverses, preventing energy drain from the output. The low-side driver operation is also affected by various fault conditions as described in the Fault Protection section.

Internal Bias Supply

The VL linear regulator provides a 5V output that is used to power the gate drivers, 2.5V reference and internal control section of the SC1403. The regulator is capable of supplying up to 50mA (including MOSFET gate charge current). The VL pin should be bypassed to GND with 4.7uF to supply the peak current requirements of the gate driver outputs. The regulator receives its input power from the V+ battery input. Efficiency is improved by providing a boot-strapping mode for the VL bias. When the 5V SMPS output voltage reaches 5V, internal circuitry detects this condition and turns on a PMOS pass device between CSL5 and VL. The internal VL regulator is then disabled and the VL bias is provided by the high efficiency switcher.

The REF output is accurate to +/- 2% over temperature. It is capable of delivering 5mA max and should be bypassed with 1uF minimum capacitor. Loading the REF pin will reduce the REF voltage slightly.

Functional Information

Loading Resistance (ohm)	511	2.67K	49.9K	255K	1Meg
Deviation from Vref = 2.4920V	8.3mV	3.1mV	0.5mV	0.3mV	0mV

Current Sense (CSH, CSL)

The output current of the power supply is sensed as the voltage drop across an external resistor between CSH and CSL pins. Over-current is detected when the current sense voltage exceeds +/-50mV. A positive over-current will turn off the high-side driver; a negative over-current will turn off the low-side driver, each on a cycle by cycle basis.

Oscillator

When the SYNC pin is set high the oscillator runs at 300KHz; when SYNC is set low the frequency is 200KHz. The oscillator can also be synchronized to the falling edge of a clock on the SYNC pin with a frequency between 240KHz and 350KHz. In general, 200KHz operation is used for highest efficiency, and the 300KHz for minimum output ripple and/or smaller filter components.

Fault Protection

In addition to cycle-by-cycle current limit, the SC1403 monitors over-temperature, and output over-voltage and under-voltage conditions. The over-temperature detect will shut the part down if the die temperature exceeds 150°C with 10°C of hysteresis.

If either SMPS output is more than 10% above its nominal value, both SMPS are latched off and synchronous rectifiers are latched on. To prevent the output from ringing below ground in a fault condition, a 1A Schottky diode should be placed across each output. Two different levels of undervoltage are detected. If the output falls 10% below its nominal output, the $\overline{\text{RESET}}$ output is pulled low.If the output falls 25% below its nominal output following a start-up delay, both SMPS are latched off. Both of the latched fault modes persist until $\overline{\text{SHDN}}$ or RUN/ON3 is toggled or the V+ input is brought below 1V.

Shutdown and Operating Modes

Holding the $\overline{\text{SHDN}}$ pin low disables the SC1403, reducing the V+ input current to less than 10uA. When $\overline{\text{SHDN}}$ goes high, the part enters a standby mode where the VL regulator and VREF are enabled. Turning on either SMPS will put the SC1403 in run mode.

SHDN	ON3	ON5	MODE	DESCRIPTION
Low	X	X	Shut-down	Minimum bias current
High	Low	Low	Standby	VREF and VL regulator enable
High	High	High	Run Mode	Both SMPS Running

Output Voltage Selection

If FB is connected to ground, internal resistors setup 3.3V and 5V output voltages. If external resistors are used, the internal feedback is disabled and the output is regulated based on 2.5V reference at the FB pin. (see comment in the application design section).

Power up Controls and Soft Start

The user has control of the SC1403 RESET# by setting the SEQ, ON3 and ON5 pins as described in the following table.

Each SMPS contains its own counter and DAC to gradually increase the current limit at startup to prevent surge currents. The current limit is increased from 0, 20%, 40%, 60%, 80%, to 100% linearly over the course of 512 switching cycles.

A RESET# output is also generated at startup. The RESET# pin is held low for 32K switching cycles. Another timer is used to enable the undervoltage protection. The undervoltage protection circuitry is enabled after 6144 switching cycles at which time the SMPS should be in regulation.

When SEQ is set to REF, the RESET# pin only monitors the 3.3V SMPS in regulation and the 5V SMPS is ignored.

Applications Information

Reference Circuit Design

Introduction

The SC1403 is a versatile dual switching regulator adjustable from 2.5V to 5.5V with fixed 5V and 3.3V modes. In addition, there is an on-chip 5V linear regulator capable of supplying 50mA output current. The SC1403 is designed for notebook applications but has applications where high efficiency, small package and low cost are required.

Functional Information (Cont.)

SC1403 Startup Sequence Chart

SEQ	ON3	ON5	RESET	DESCRIPTION
REF	LOW	LOW	Follows 3.3V SMPS.	Independant start control mode. Both SMPSs off.
REF	LOW	HIGH	Low.	5V SMPS ON, 3.3V SMPS OFF.
REF	HIGH	LOW	Follows 3.3V SMPS.	3.3V SMPS ON, 5V SMPS OFF.
REF	HIGH	HIGH	Follows 3.3V SMPS.	Both SMPSs on.
GND	LOW	X	Low.	Both SMPSs off.
GND	HIGH	HIGH/LOW	High after both outputs are in regulation.	5V starts when ON3 goes high. If ON5 = HIGH, 3V is on. If ON3 = LOW, 3V is off.
VL	LOW	X	Low.	Both SMPSs off.
VL	HIGH	HIGH/LOW	High after both outputs are in regulation.	3V starts when ON3 goes high. If ON5 = HIGH, 5V is on. If ON3 = LOW, 5V is off.

Applications Information

Design Guidelines

The schematic for the reference circuit is shown on page 24. The reference circuit is configured as follows:

Switching Regulator 1 Vout1 = 3.3V @ 6A
Switching Regulator 2 Vout2 = 5.0V @ 6A
Linear Regulator Vout3 = 5.0V @ 50mA

Designing the Output Filter

Before calculating the output filter inductance and output capacitance, an acceptable amount of output ripple current is to be determined. The maximum allowable ripple current depends on the transient requirement of the power supply. Under normal situation, the ripple current is usually set at 10 to 20% of the maximum load. However, in order to speed up the output transient response, ripple current can be much higher. In this design, we are going to set the ripple current to be 40% of maximum load. So once the ripple voltage specification is determined, the capacitor ESR is chosen. The output ripple voltage is usually specified at +/- 1% of the output voltage.

For the reference circuit 3.3V switcher, we selected a maximum ripple voltage of 33mV. Choosing one 180uF, 4V Panasonic SP Polymer Aluminum Electrolytic Cap, of which ESR is 15 $m\Omega$, sets the maximum ripple current as follows:

$$\Delta I_O = \frac{\Delta V_{O\_MAX}}{ESR} \qquad \Delta I_O = \frac{0.033V}{0.015\Omega} = 2.2A$$

Checking to see if the maximum RMS current can be met by the SP cap.

$$I_1 = -\frac{\Delta I_O}{2} \qquad I_2 = +\frac{\Delta I_O}{2}$$

$$I_{RMS} = \sqrt{\frac{I_1^2 + I_1 \cdot I_2 + I_2^2}{3}}$$

Irms=0.635 A << Irms_rated=3.0A

The output inductance can now be found by:

$$L_O = \frac{(V_{IN\_NOM} - V_O) \cdot D_{NOM} \cdot T_S}{\Delta I_O}$$

Applications Information

where Vin_nom=15V, Vo=3.3V, D=Vo/Vin_nom, Fs=300KHz, Ts=3.33uS and ΔIo=2.2 A. Lo is subsequently calculated to be 3.9uH. For the interest of this design, Lo is chosen to be 4.7uH.

Choosing Current Sense Resistor

Since the SC1403 implements Virtual Current Sense™, the external current sense resistor is not required for the control loop. However, it is required for cycle-by-cycle current limit. Cycle-by-cycle current limit is enabled when the voltage across the current sense resistor exceeds 50mV nominal. Depending on the system requirement, this current limit can vary, it is usually 10 to 30% higher than the maximum load. Taking into consideration of the +/-20% variation on the 50mV, the value of the current sense resistor can be calculated using the following equation:

$$R_{SENSE} = \frac{40mV_{(min)}}{I_{PK\_OC}}$$

For a DC OC trip point between 6.3A to 9.8A, Rsense is chosen to be 5.5mΩ. Considering the maximum power dissipation, two Vishay WSL2010 11mΩ 1% resistors are used.

Choosing the Main Switching MOSFET

Before choosing the main switch MOSFET, we need to know two critical parameters: voltage and current rating. In order to minimize the conduction loss, we recommend using the lowest Rds(on) for the same voltage and current rating. The maximum drain to source voltage of the switch MOSFET is mainly decided by the topology of the switcher. Since this is a buck topology,

$$V_{DS\_MAX} = V_{IN\_MAX} = 21V$$

Applying a derating of 70%, a 30V MOSFET is used in the design. The peak current of the MOSFET is determined by

$$I_{PEAK} = \frac{60mV}{5.5m\Omega} = 11A$$

According to the calculated voltage and current rating, Si4886DY, IRF7413, FDS9412 or STS12NF30L meets the requirement. The specs for these MOSFETs are listed in the table below. For the purpose of this exercise, STS12NF30L is chosen. Next step is to determine its power handling capability. Based on 85°C ambient temperature, 150°C junction temperature and 50°C /W thermal resistance, its power handling is calculated as follows:

T_J = 150°C; T_A = 85°C; θ_{JA}= 50°C/W

$$P_T = \frac{T_J - T_A}{\theta_{JA}} = \frac{150 - 85}{50} = 1.30W$$

Vendor P/N	VDS (V)	ID (A)	Rds(0n) @ 4.5V (ohm)	Package
Si4886DY	30	13	0.0135	SO-8
IRF7413	30	13	0.011	SO-8
FDS9412	30	7.9	0.036	SO-8
STS12NF30L	30	12	0.0085	SO-8

The following calculations are done to verify that the power dissipation of the main switch MOSFET is well within 1.86W, which is the maximum allowable power dissipation for the package.

$$P_{TOTAL\_DISS} = P_{CONDUCTION} + P_{SWITCHING} + P_{GATE}$$

$$P_{CONDUCTION} = R_{ds(on)} \cdot I_{RMS}{}^2 \cdot D_{nom}$$

where Rds(on) = 0.01Ω @Tj=25°C and Vgs = 4.5V. In order to find Rds(on)@ Tj=100°C, use 1.40*Rds(on)@25°C. Therefore, Rds(on) @ Tj = 100°C is equal to 0.014Ω.

$$I_{RMS} = \sqrt{(\frac{I_1{}^2 + I_1 \cdot I_2 + I_2{}^2}{3})}$$

where

$$I_1 = I_{MAX} + \frac{\Delta Io\_MAX}{2} = 7.1A, \quad I_2 = I_{MAX} - \frac{\Delta Io\_MAX}{2} = 4.9A \text{ and}$$

$$D_{nom} = \frac{V_{OUT}}{V_{IN\_NOM}}$$

The worst case conduction loss is calculated to be 112mW. And the switching loss of the MOSFET is given by,

$$P_{SWITCHING} = \frac{C_{RSS} \cdot V_{IN}{}^2 \cdot f_S \cdot I_{OUT}}{I_G}$$

where Crss is the reverse transfer capacitance of the MOSFET; it is equal to 200pF for STS12NF30L, Ig is the gate driver current; it is equal to 1A for SC1403. And Vin_nom = 15V, fs = 300KHz. The switching loss is calculated to 81mW. And the gate loss is given by,

$$P_{GATE} = \frac{1}{2} \cdot C_G \cdot V^2 \cdot f_S$$

where Cg=11nF, V=5V and fs=300KHz. The gate loss is calculated to be 41mW.

So the total power dissipation is calculated to be 234mW and is well within the maximum power dissipation allowance of the MOSFET. No special heating sinking is required when laying out the MOSFET.

Applications Information (Cont.)

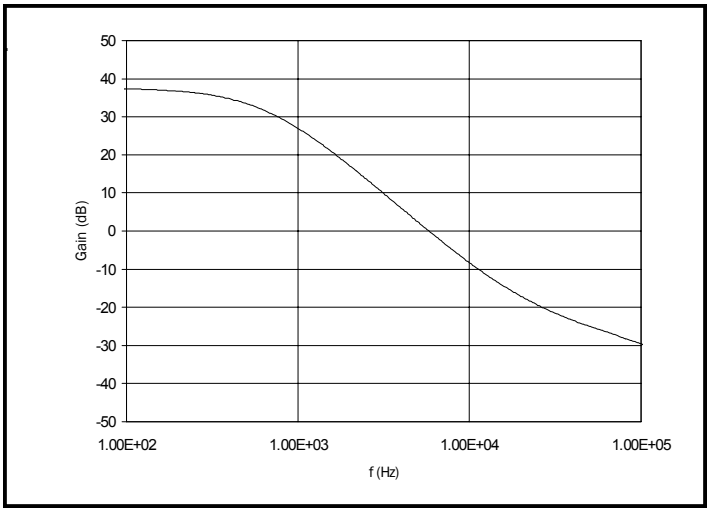
Designing the Loop

There are two aspects concerning the loop design. One is the power train design and the other is the external compensation design. A good loop design is a combination of the two. In the SC1403, the control-to-output/power train response is dominated by the load impedance, the effective current sense resistor, output capacitance, and the ESR of the output caps. The low frequency gain is dominated by the output load impedance and the effective current sense resistor. Inherent to Virtual Current Sense™, there is one additional low frequency pole sitting between 100Hz and 1KHz and a zero between 15KHz and 25KHz. To compensate for the SC1403 is easy since the output of error amplifier COMP pin is available for external compensation. A traditional pole-zero-pole compensation is not necessary in the design using SC1403. To ensure high phase margin at crossover frequency while minimizing the component count, a simple high frequency pole is usually sufficient. In the reference design below, single-pole compensation method is demonstrated. And the loop measurement results are compared to that obtained from the simulation model. Transient response is also done to validate the model. Also, to help speeding up the design process, a list of recommended output caps vs. compensation caps value is given in table I.

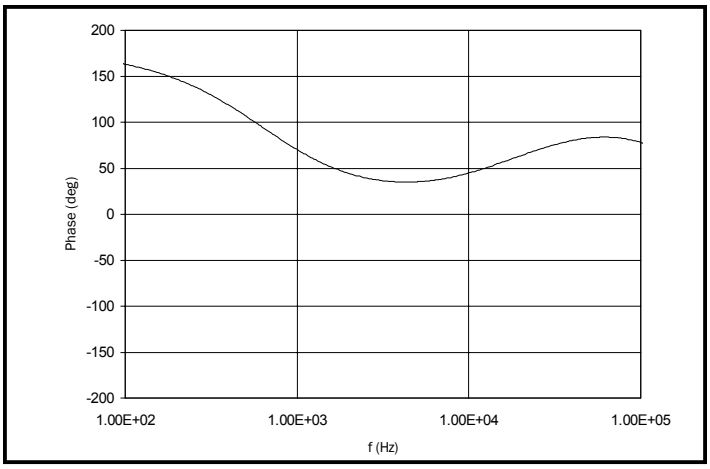
Single-Pole compensation Method

Given parameters:
Vin = 19V, Vout = 3.3V @ 2.2A,
Output impedance, Ro = 3.3V/2.2A = 1.5 Ω ,
Panasonic SP cap, Co = 180uF, Resr = 15 mΩ ,
Output inductor, Lo = 4.7uH
Switching frequency, Fs = 300KHz

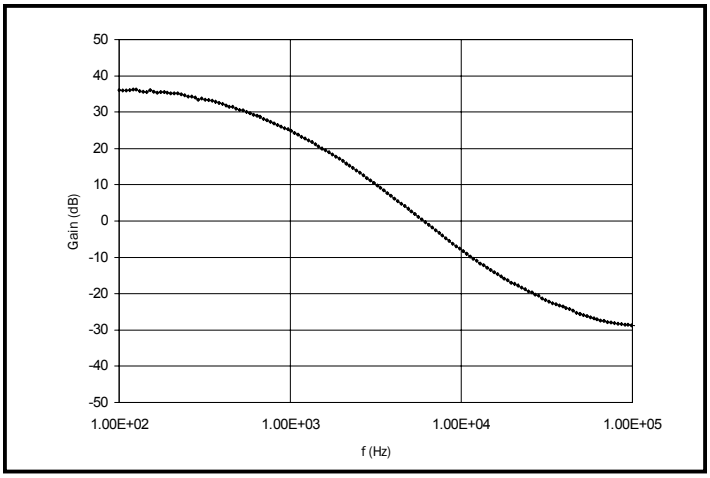
Simulated Control-to-Output gain & phase response (up to 100KHz) is plotted below

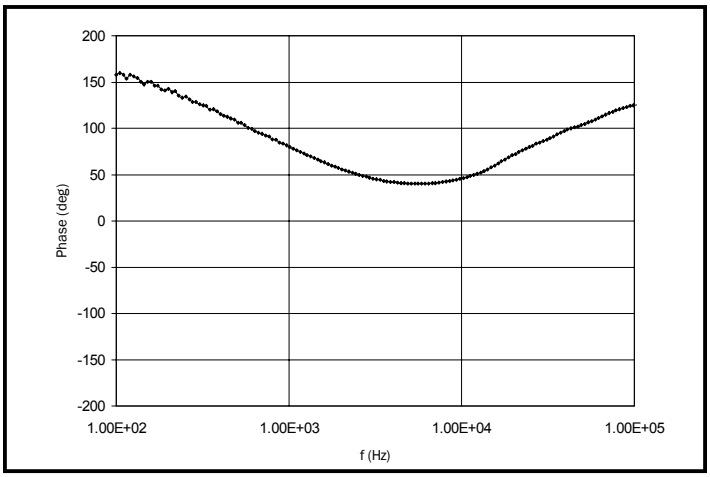


.



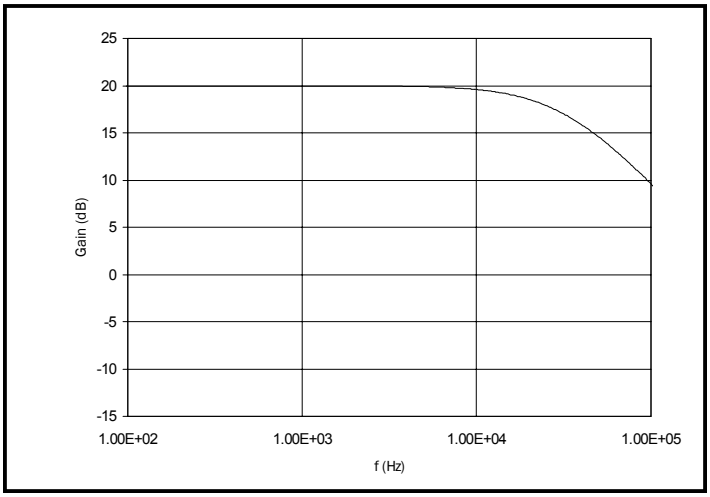
Measured Control-to-Output gain & phase response (up to 100KHz) is plotted below.

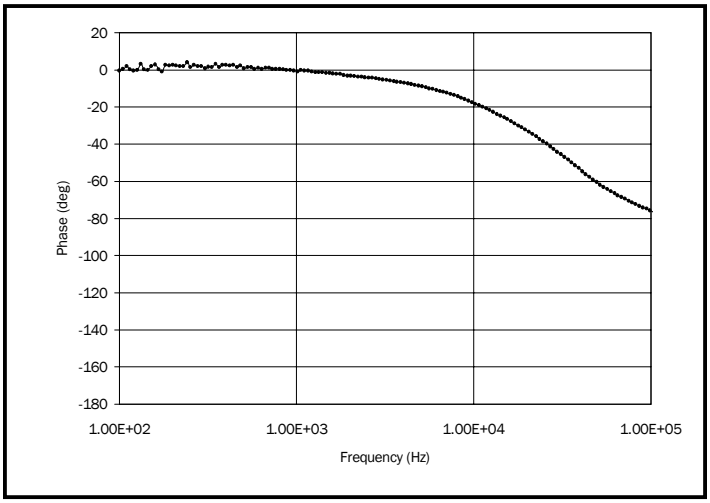


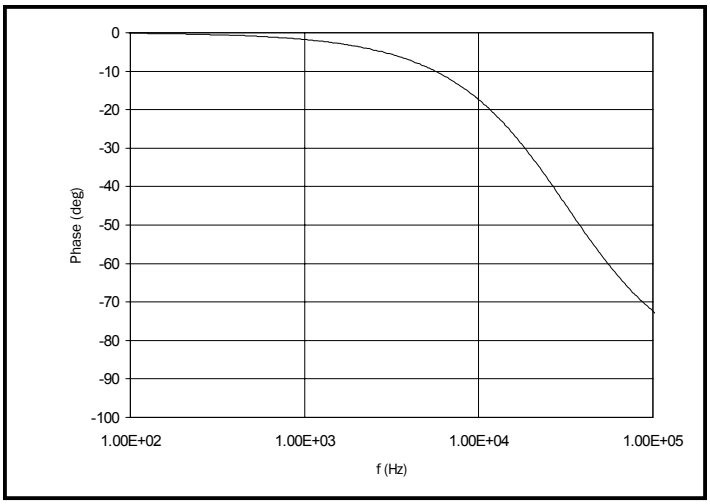


Single-pole compensation of the error amplifier is achieved by connecting a 100pF capacitor from the COMP pin of the SC1403 to ground. The simulated feedback gain & phase response (up to 100KHz) is plotted below.

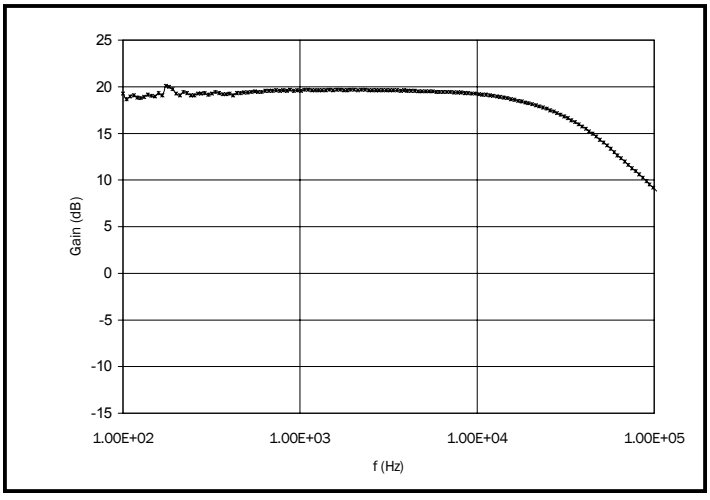
Applications Information (Cont.)



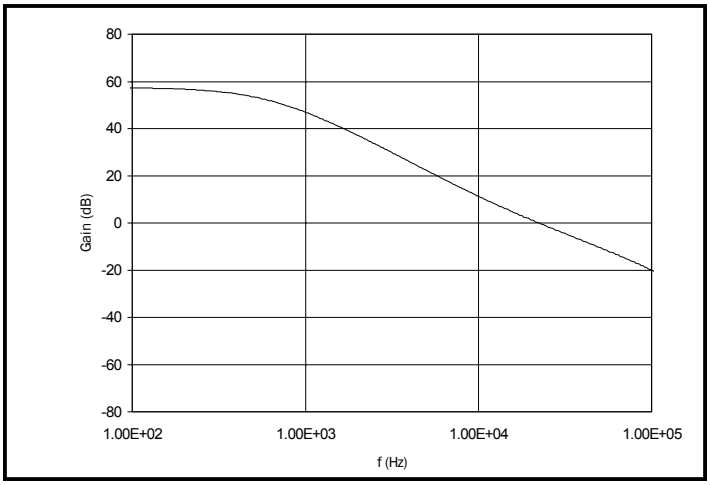


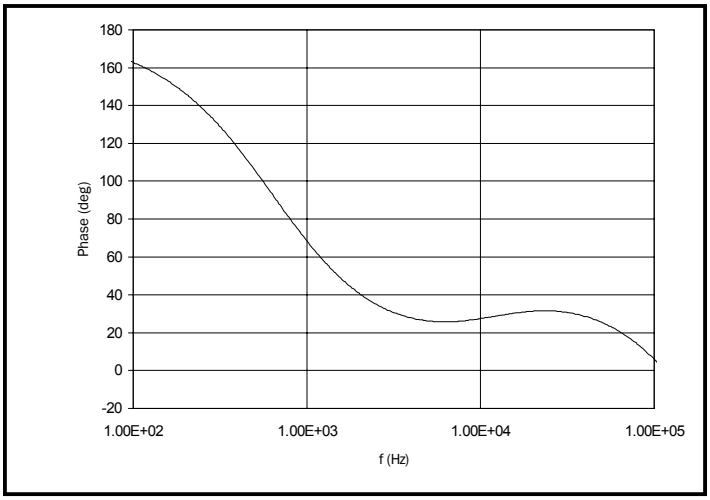


Measured feedback gain & phase responses (up to 100KHz) is plotted below.



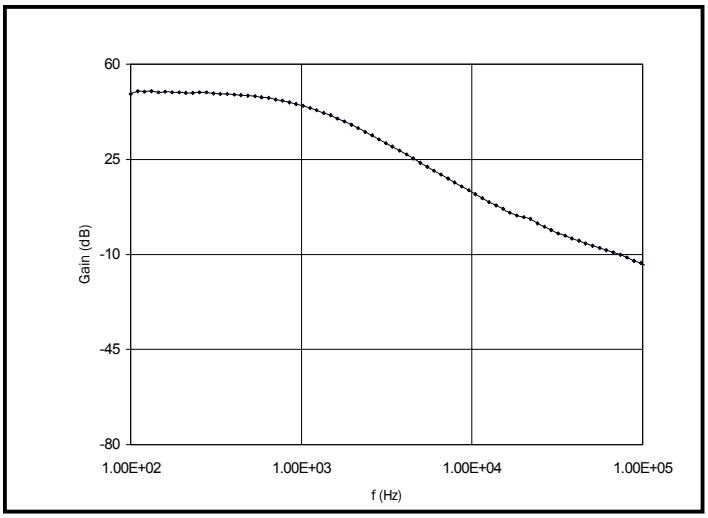
Simulated overall gain & phase responses (up to 100KHz) is plotted below.





Applications Information (Cont.)

Measured overall gain & phase response of the single-pole compensation using SC1403 is plotter below.



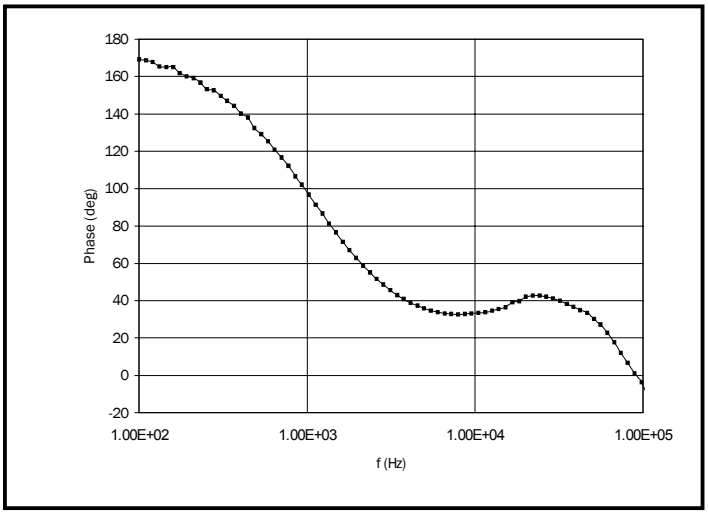


Table I. Recommended compensation cap for different output capacitance.

Output Cap	Recommended Compensation Cap Value
< = 180µF	100pF
> 180µF & <1000µF	200pF
>1000µF	330pF

Table I. is useful only if the following ESR condition is satisfied.

$$f_0 = \frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_0}$$

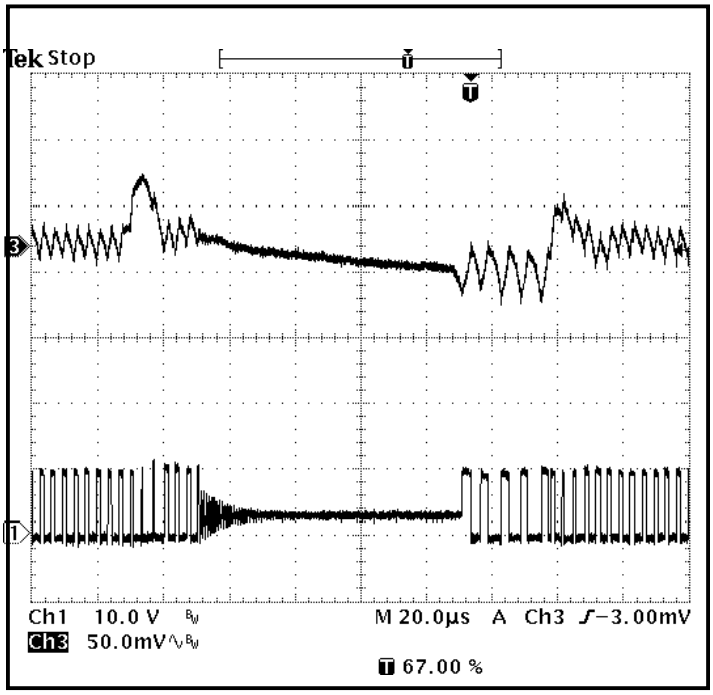
fo > 50KHz

where Resr is the equivalent ESR of the total output caps.

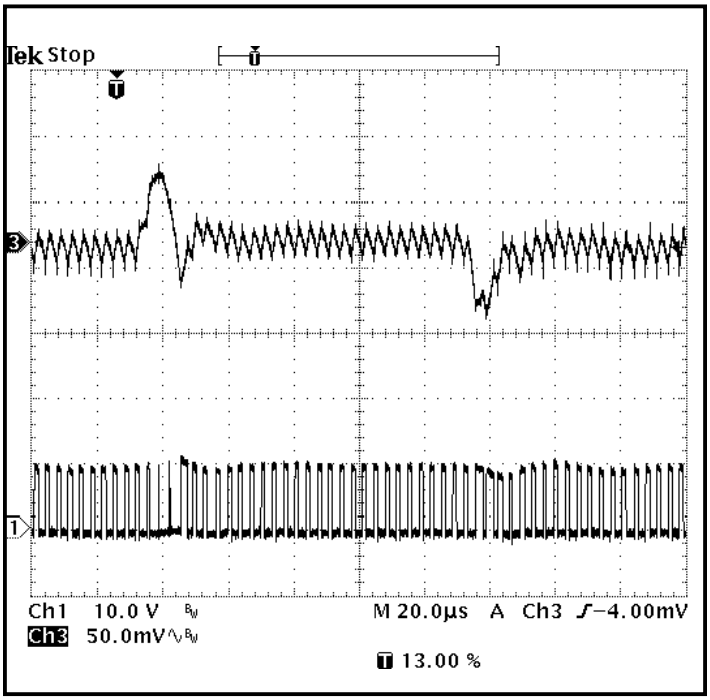
Transient responses of the switcher using single-pole compensation are shown below. The load steps from 0A to 3A and 3A to 6A. The applied di/dt is 2.5A/usec

Typical Characteristics

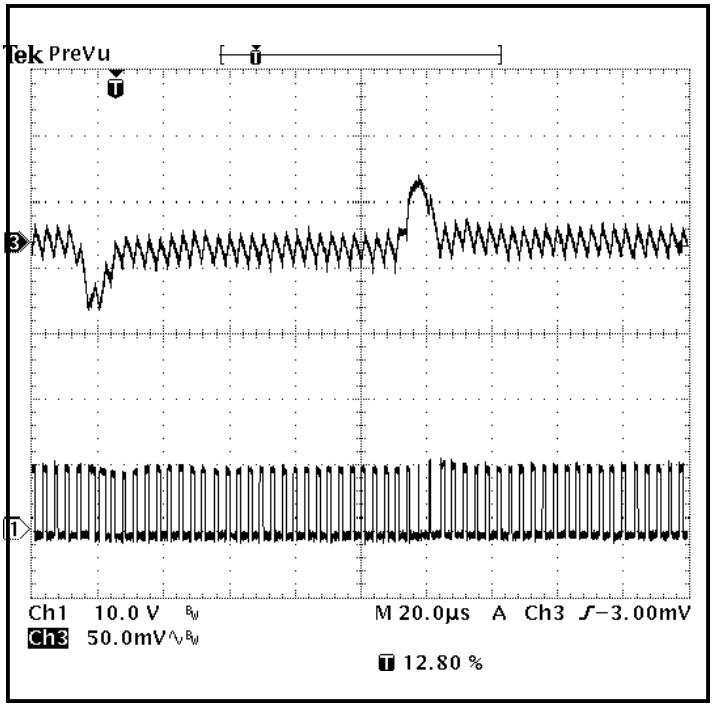
Condtions: (PSAVE enabled)
Vin = 10V, ILoad= 0A to 3A
Vout = 3.3V



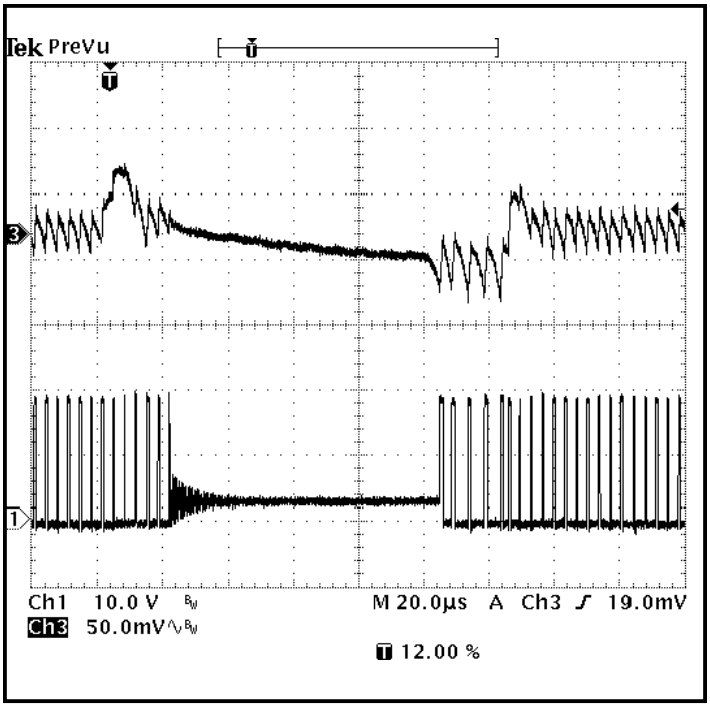
Condtions: (PSAVE disabled)
Vin = 10V, ILoad= 0A to 3A
Vout = 3.3V



Condtions:
Vin = 10V, ILoad= 3A to 6A
Vout = 3.3V

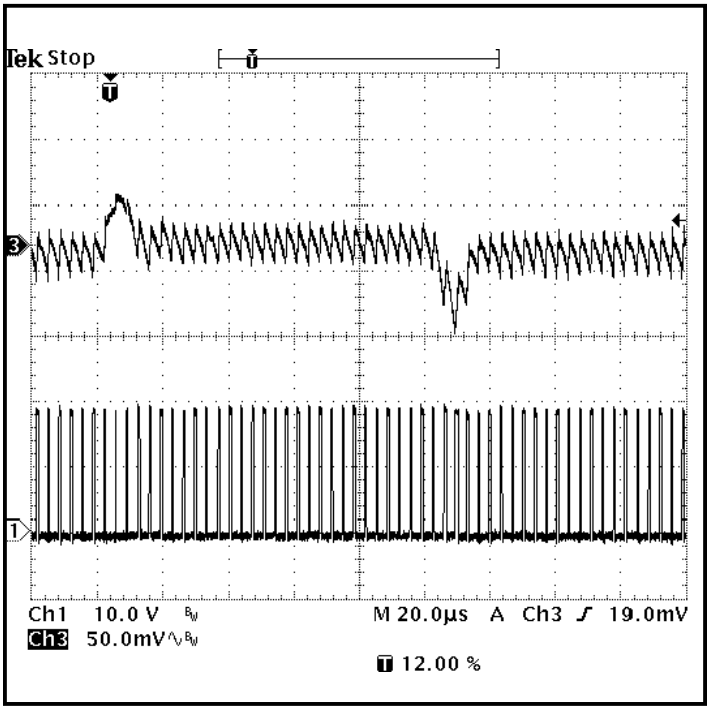


Condtions: (PSAVE enabled)
Vin = 19V, ILoad= 0A to 3A
Vout = 3.3V

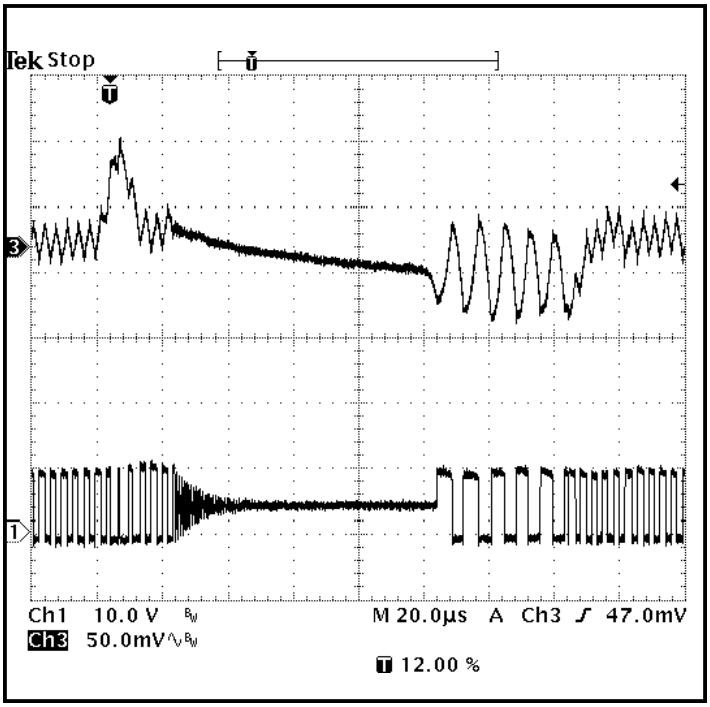


Typical Characteristics (Cont.)

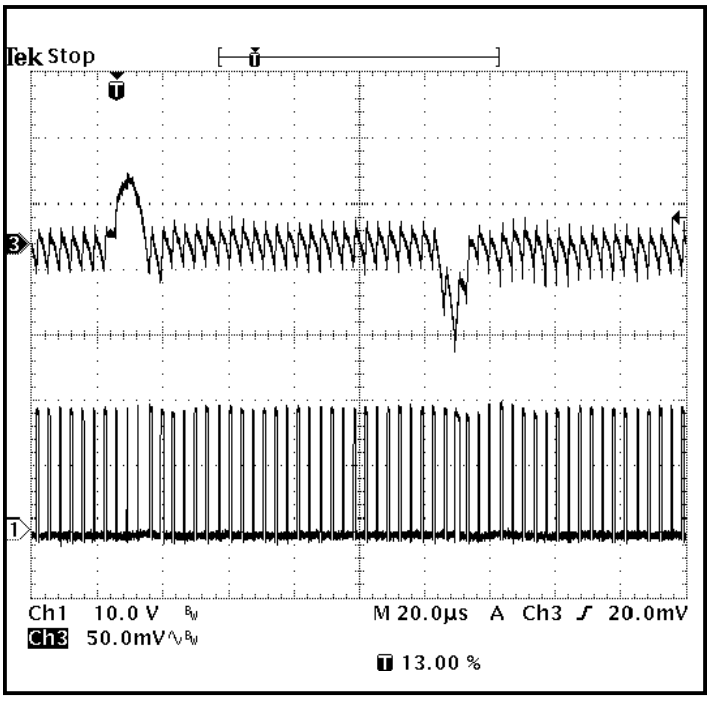
Condtions: (PSAVE disabled)
Vin = 19V, ILoad= 0A to 3A
Vout = 3.3V



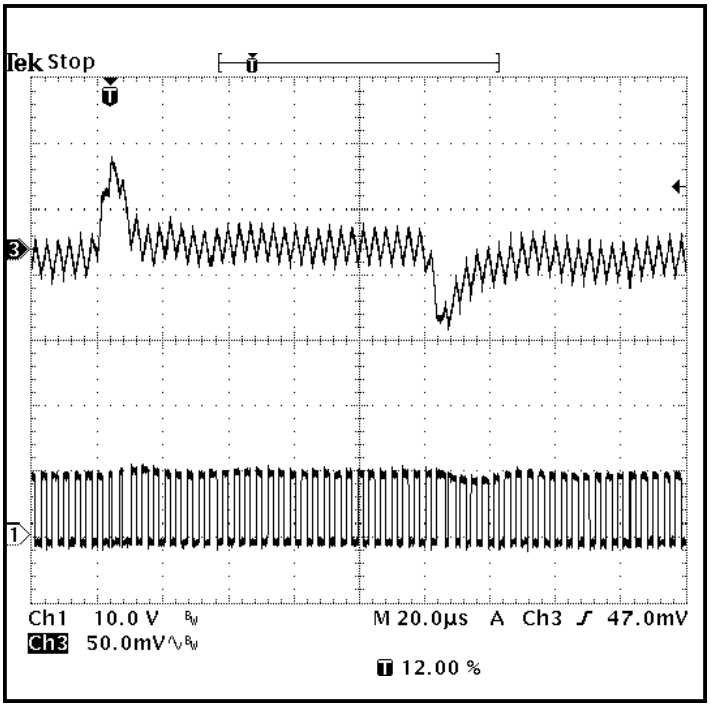
Condtions: (PSAVE enabled)
Vin = 10V, ILoad= 0A to 3A
Vout = 5.0V



Condtions:
Vin = 19V, ILoad= 3A to 6A
Vout = 3.3V

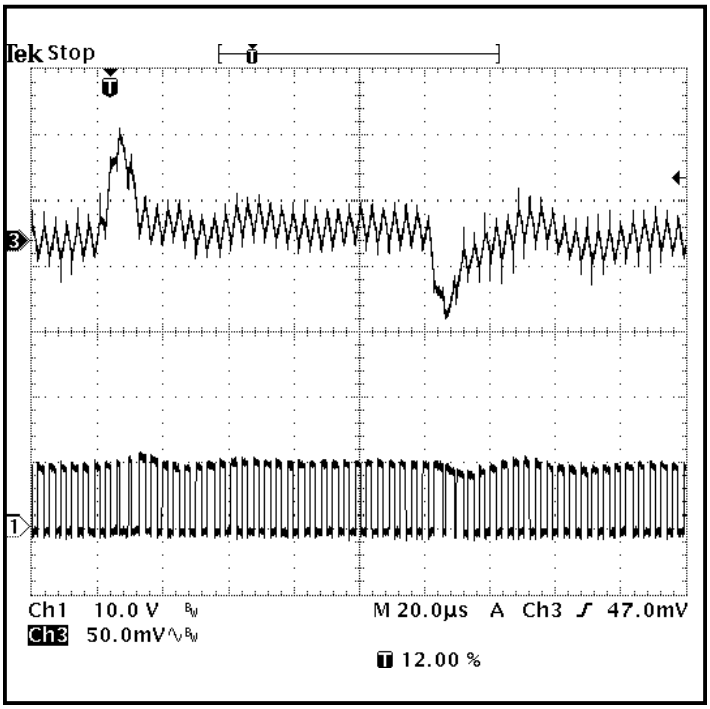


Condtions: (PSAVE disabled)
Vin = 10V, ILoad= 0A to 3A
Vout = 5.0V

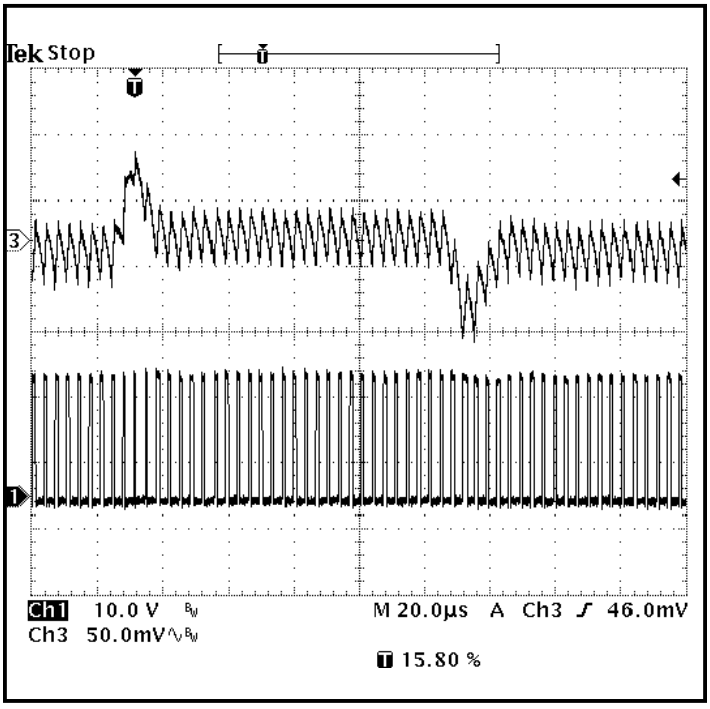


Typical Characteristics (Cont.)

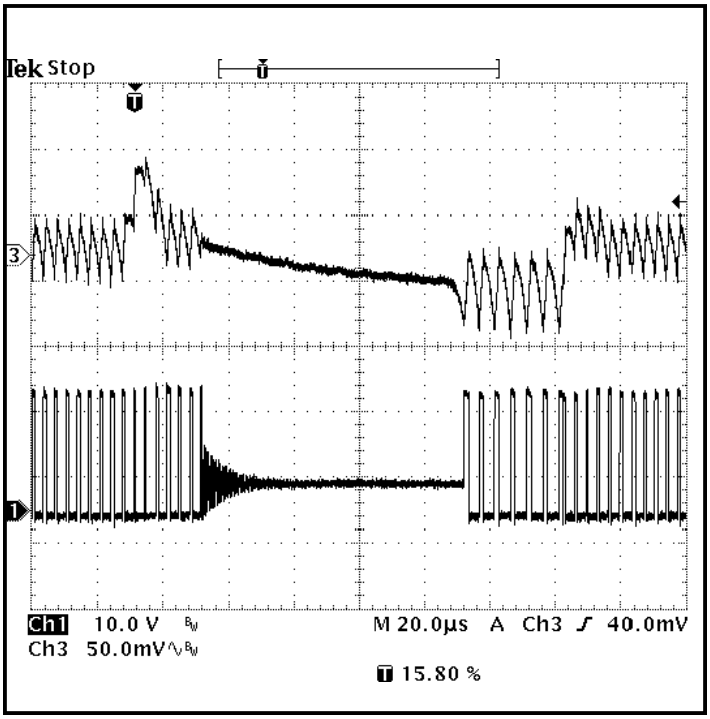
Condtions:
Vin = 10V, ILoad= 3A to 6A
Vout = 5.0V



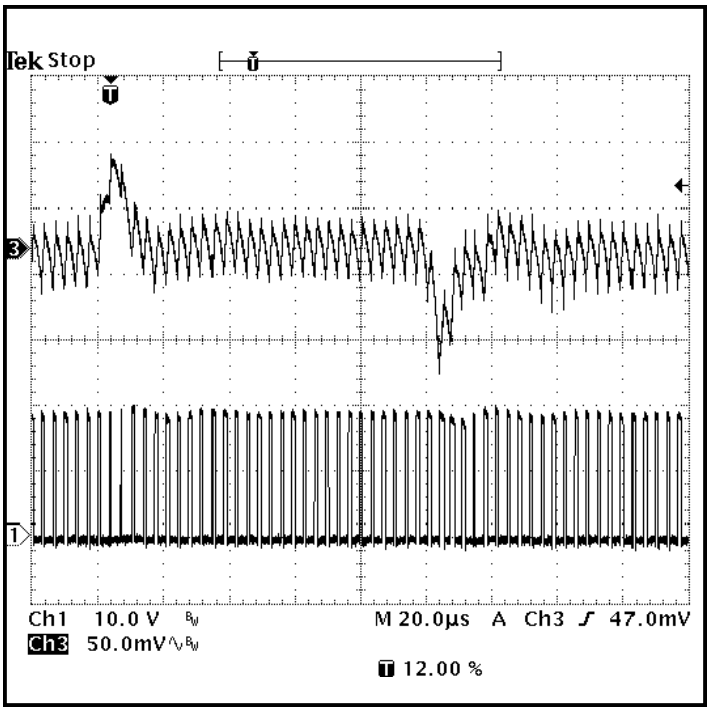
Condtions: (PSAVE disabled)
Vin = 19V, ILoad= 0A to 3A
Vout = 5.0V



Condtions: (PSAVE enabled)
Vin = 19V, ILoad= 0A to 3A
Vout = 5.0V



Condtions:
Vin = 19V, ILoad= 3A to 6A
Vout = 5.0V



Applications Information

Input Capacitor Selection

Input bulk capacitor is selected based on the input RMS current requirement of the converter.

The input RMS ripple current can be calculated as follows:

$$I_{RMS} = \sqrt{V_{OUT} \cdot (V_{IN} - V_{OUT})} \cdot \frac{I_{out}}{V_{IN}}$$

The worst case input RMS current occurs at 50% duty cycle and therefore under this condition the Irms current can be approximated by

$$I_{RMS} = \frac{I_{LOAD}}{2}$$

Therefore, for a maximum load current of 6A, the input capacitor should be able to handle 3A of ripple current. For the reference circuit design, there are two such regulators that operate out-of-phase. Therefore, 3A ripple current is the most these two converters will see under the normal steady state operating condition. For the combined two regulators, one SMT OS-CON 47uF, 25V is used. The maximum allowable ripple current for the cap is rated 3.5A rms @ 100KHz, 45 °C. Considering the derating at higher ambient temperature and higher operating frequency, two additional MLC caps are also used (Vishay MLC, 12uF, 25V, Y5V, size 2225).

Choosing Synchronous MOSFET and Schottky diode

Since this is a buck topology, the voltage and current ratings of the synchronous MOSFET is the same as the main switching MOSFET. It makes sense cost-volume-wise to use the same MOSFET for the main switch as for the synchronous MOSFET. Therefore, STS12NF30L is used again in the design for synchronous MOSFET. To improve overall efficiency, an external schottky diode is used in parallel to the synchronous MOSFET. The freewheeling current is going into the schottky diode instead of the body diode of the synchronous MOSFET, which usually has very high forward drop and slow transient behavior. It is really important when laying out the board, to place both the synchronous MOSFET and Schottky diode close to each other to reduce the current ramp-up and ramp-down time due to parasitic inductance between the channel of the MOSFET and the Schottky diode. The current rating of the Schottky diode can be determined by the following equation,

$$I_{F\_AVG} = I_{LOAD} \cdot \frac{100n}{Ts} = 0.2A$$

where 100nsec is the estimated time between the MOSFET turning off and the Schottky diode taking over and Ts = 3.33uS. Therefore a Schottky diode with a forward current of 0.5A is sufficient for this design.

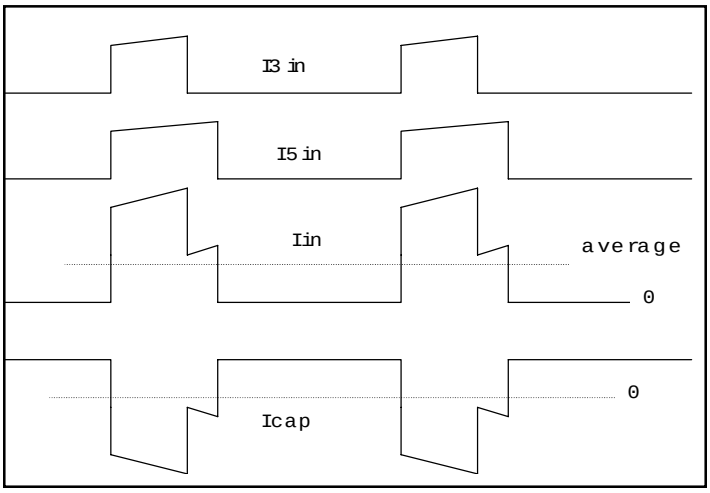
External Feedback Design

In order to optimize the ripple voltage during Power Save mode, it is strongly recommended to use external voltage dividers (R10 and R9 for 5V power train; R8 and R11 for 3.3V power train) to achieve the required output voltages. In addition, a 56pF (C22 for 5V and C21 for 3.3V) cap is recommended connecting from the output to both feedback pins (pin # 3 and #12). The signal to noise ratio is therefore increased due to the added zeroes.

Input Capacitor Selection/Out-of-phase Switching

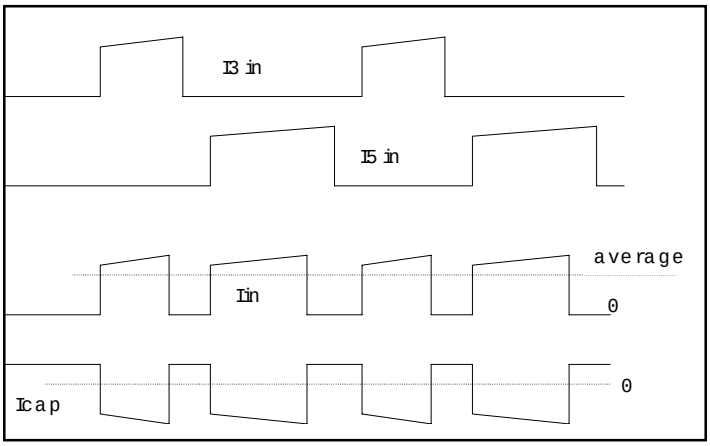
The SC1403 uses out-of-phase switching between the two converters to reduce input ripple current, enabling the use of smaller, cheaper input capacitors when compared to in-phase switching. The two approaches are shown in the following figures. The first figure shows in-phase switching: I3in is the input current drawn by the 3.3V converter, I5in is the input current drawn by the 5V converter. The two converters start each switching cycle simultaneously, resulting in a significant amount of overlap. This overlap increases the peak current. The total input current to the converter is the third trace Iin, which shows how the two currents add together. The fourth trace shows the current flowing in and out of the input capacitors.

In-phase Switching

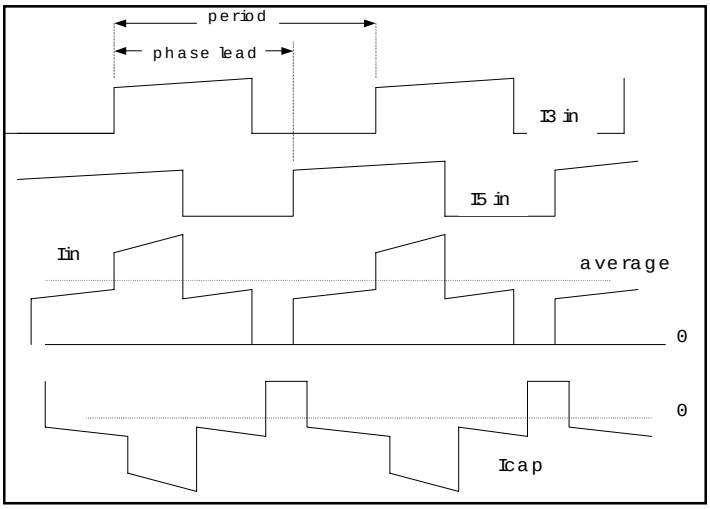


The next figure shows out-of-phase switching. Since the 3.3V and 5V converters are spaced apart, there is no resulting overlap. This results in a two benefits; the peak current is reduced and the frequency content is higher, both of which make filtering easier. The third trace shows the total input current, and the fourth trace shows the current in and out of the input capacitors. The RMS value of this current is significantly lower than the in-phase case and allows for smaller capacitors due to reduced RMS current ratings.

Out-of-phase Switching



As the input voltage is reduced, the duty cycle of both converters increases. For inputs less than 8.3 volts it is impossible to prevent overlap when producing 3.3V and 5V outputs, regardless of the phase relationship between the converters. This can be seen in the following figure.



From an input filter standpoint it is desirable to make the minimize the overlap, but it is also desirable to keep the turn-on and turn-off transitions of the two converters separated in time, otherwise the two converters may affect each other due to switching noise. The SC1403 implements this by changing the phase relationship between the converter depending on the input voltage.

Input voltage	Phase lead from 3V converter rising edge to 5V converter rising edge
Vin > 9.6 V	41% of switching period
9.6V > Vin > 6.7V	59% of switching period
6.7 > Vin	64% of switching period

Vin > 9.6V: 3.3V turn-on leads 5V turn-on by 41% of the switching period. With Vin > 9.6V it is always possible to achieve no overlap, which minimizes the input ripple current. At Vin = 9.6V there is no overlap, but the 3.3V turn-on is nearing the 5V turn-off converter.

6.7 < Vin < 9.6V: 3.3V turn-on leads 5V turn-on by 59% of the period. To prevent the 3V turn-on from coinciding with the 5V turn-off (which could affect either output), the 5V pulse is delayed in time slightly such that the 3V turn-on occurs before the 5V turn-off. This creates a small overlap between the 3V turn-on and the 5V turn-off, with a resulting slight increase in RMS input ripple, but this is preferred since it greatly reduces noise problems caused by simultaneous transitions. Note that at Vin = 6.7, the 3V turn-off is nearing the 5V turn-on.

Vin < 6.7 volts: 3.3V turn-on leads 5V turn-on by 64% of the period. The 5V turn-on is delayed slightly more to add separation between the 3V turn-off and 5V turn-on. This leads to more overlap, but at this point overlap is unavoidable.

Input ripple current calculations: The following equations provide quick approximations for input ripple current:

D3 = 3.3V duty cycle = 3.3/Vin
D5 = 5V duty cycle = 5/Vin
I3 = 3.3V load current
I5 = 5V load current

Dovl = overlapping duty cycle of the 3V and 5V pulses, which varies according to input voltage:

Vin > 9.6V:	Dovl = 0
9.6V > Vin > 6.7V:	Dovl = D5 - 0.41
6.7V > Vin	Dovl = D5 - 0.36

$Iin = D3 \cdot I3 + D5 \cdot I5$ (average current drawn from Vin)

$(Isw\_rms)^2 = Dovl \cdot (I3 + I5)^2 + (D3 - Dovl) \cdot I3^2 + (D5 - Dovl) \cdot I5^2$

Isw_rms = rms current flowing into 3V and 5V SMPS

$Irms\_cap = \sqrt{Isw\_rms^2 + Iin^2}$

The worst-case ripple current varies by application. For the case of I3 = I5 = 6A, the worst-case ripple occurs at Vin = 7.5V, at which point the rms capacitor ripple current is 4.2 amps. To handle this the reference design uses 4 paralleled ceramic capacitors, (Murata GRM32NF51E106Z, 10 uF 25V, size 1210). Each capacitor is rated at 2.2 Amps, allowing for derating at higher temperatures.

Operation below 6V input

The SC1403 will operate below 6V input voltage with careful design, but there are limitations. The first limitation is the maximum available duty cycle from the SC1403, which limits the obtainable output voltage. The design should minimize all circuit losses through the system in order to deliver maximum power to the output.

A second limitation with operation below 6V is transient response. When load current increases rapidly, the output voltage drops slightly; the feedback loop normally increases duty cycle briefly to bring the output voltage back up. If duty cycle is already near the maximum limit, the duty cycle cannot increase enough to meet the demand, and the output voltage sags more than normal. This problem can not be solved by changing the feedback compensation, it is a function of the input voltage, duty cycle, and inductor and capacitor values.

If an application requires 5V output from an input voltage below 6V, the following guidelines should be used:

1 - Set the switching frequency to 200 kHz (Tie SYNC to GND). This increases the maximum duty cycle compared to 300 kHz operation.

2 - Minimize the resistance in the power train. Select MOSFETs, inductor, and current sense resistor to provide the lowest resistance as is practical.

3 - Minimize the pcb resistance for all traces carrying high current. This includes traces to the input capacitors, MOSFETS and diodes, inductor, current sense resistor, and output capacitor.

4 - Minimize the resistance between the SC1403 circuit and the power source (battery, battery charger, AC adaptor).

5 - Use low ESR capacitors on the input to prevent the input voltage dropping during on-time.

6 - If large load transients are expected, high capacitance and low ESR capacitors should be used on both the input and output.

Overvoltage Test

Measuring the overvoltage trip point can be problematic. Any buck converter with synchronous MOSFETS can act as a boost converter, sending energy from output to input. In some cases the energy sent to the input is enough to drive the input voltage beyond normal levels, causing input overvoltage. To prevent this, enable the SC1403 PSAVE# feature, which effectively disables the low side MOSFET drive so that little energy, if any, is transferred back to the input.

Semtech recommends the following circuit for measuring the overvoltage trip point. D1 prevents the output voltage from damaging lab supply 1. R1 limits the amount of energy that can be cycled from the output to the input. R2 absorbs the energy that might flow from output to input, and D2 protects lab supply from possible damage. The ON5 signal is monitored to indicate when overvoltage occurs.

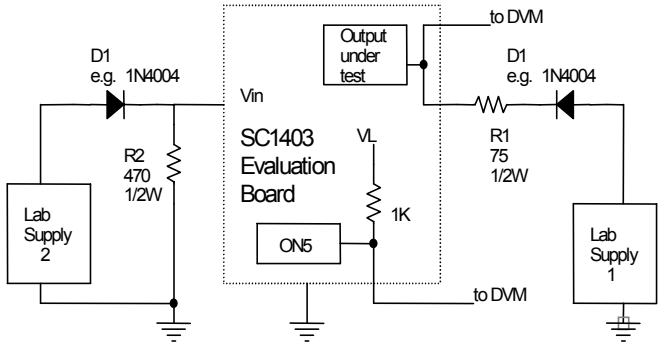
Initial conditions:

Both lab supplies set to zero volts
No load connected to 3V or 5V
PSAVE# enabled (PSAVE# tied to GND)
ON5, ON3 both enabled
DVMs monitoring ON5 and the output under test.
Oscilloscope probe connected to Phase Node
of the output under test (not strictly required).

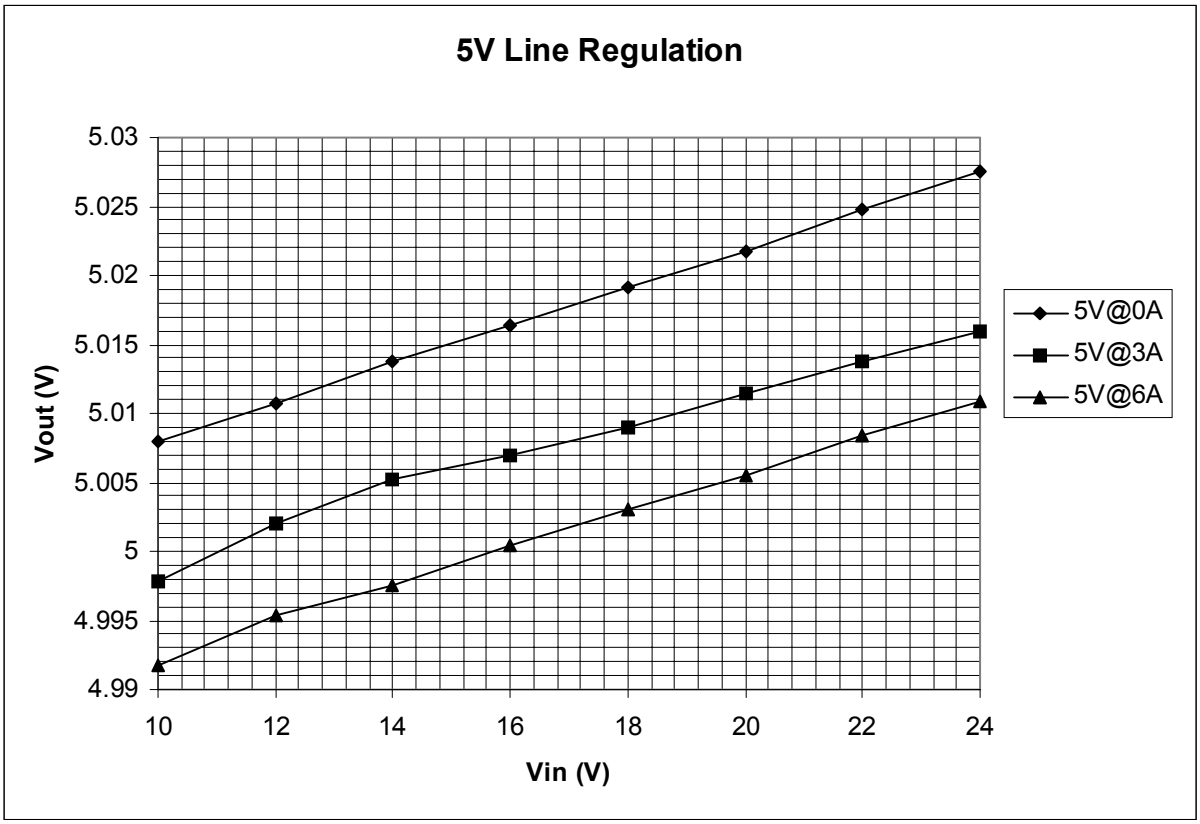
Set lab supply 2 to provide 10V at the SC1403 input. The phase node of the output being tested should show some switching activity. The ON5 pin should be above 4V.

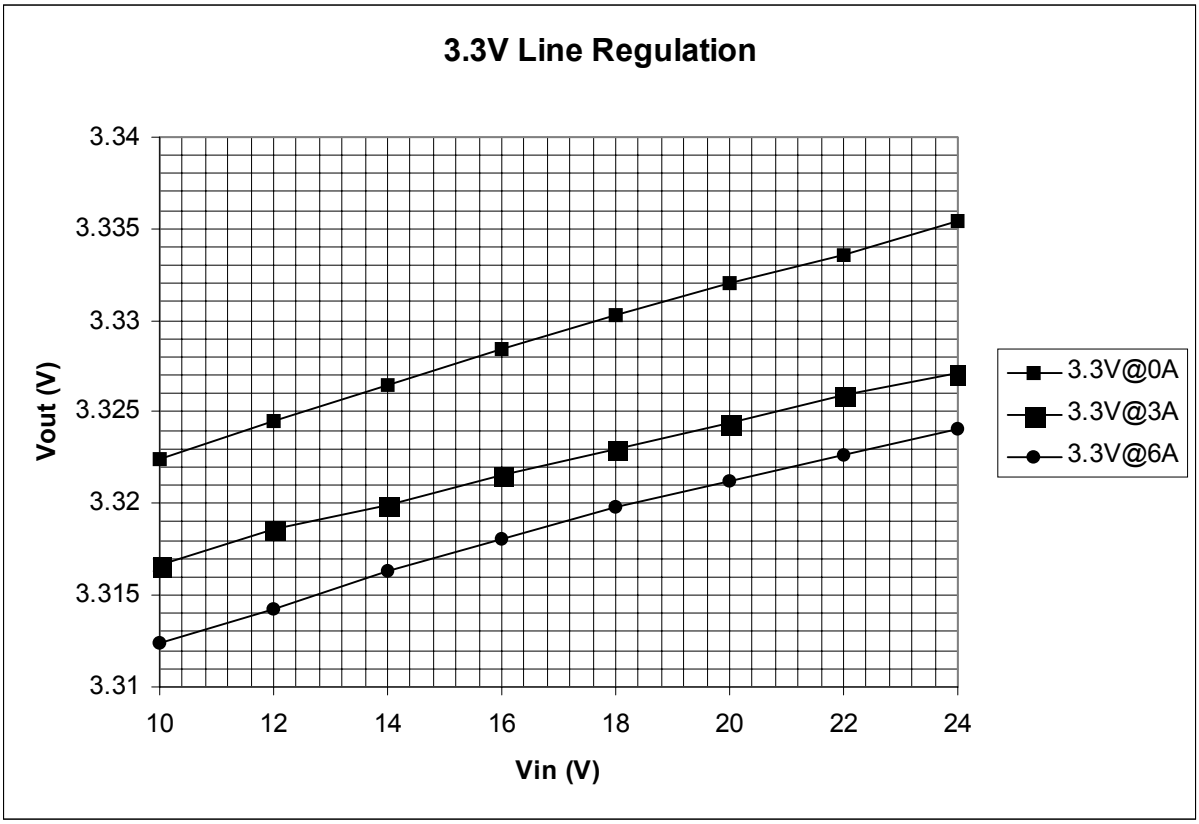
Slowly increase lab supply 1 until the output under test rises slightly above it's normal DC level. As the input lab supply 1 increases, switching activity at the phase node will cease. The ON5 pin should remain above 4V.

Increase lab supply 1 in very small increments, monitoring both ON5 and the output under test. The overvoltage trip point is the highest voltage seen at the output before ON5 pulls low (approximately 0.3V). Do not record the voltage seen at the output after ON5 has pulled low; when ON5 pulls low, the current flowing in D1 changes, corrupting the voltage seen at the output.

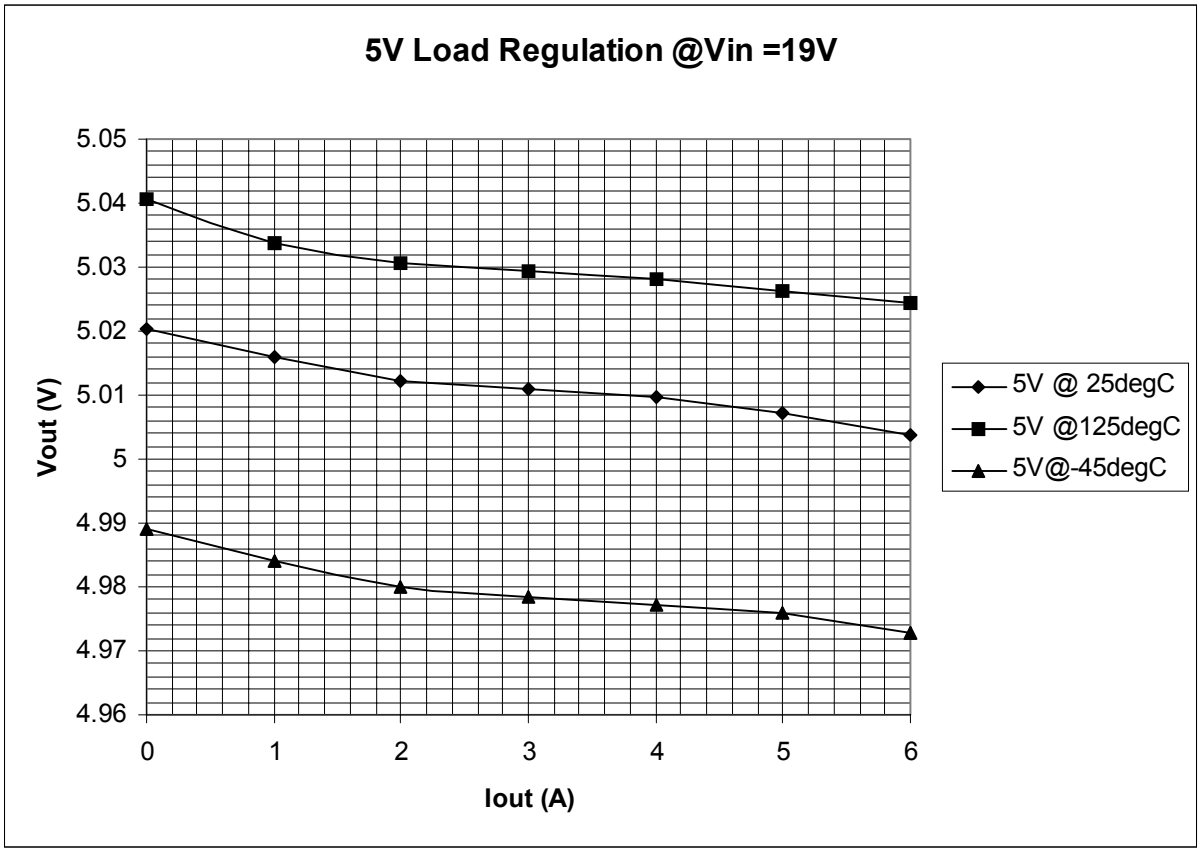


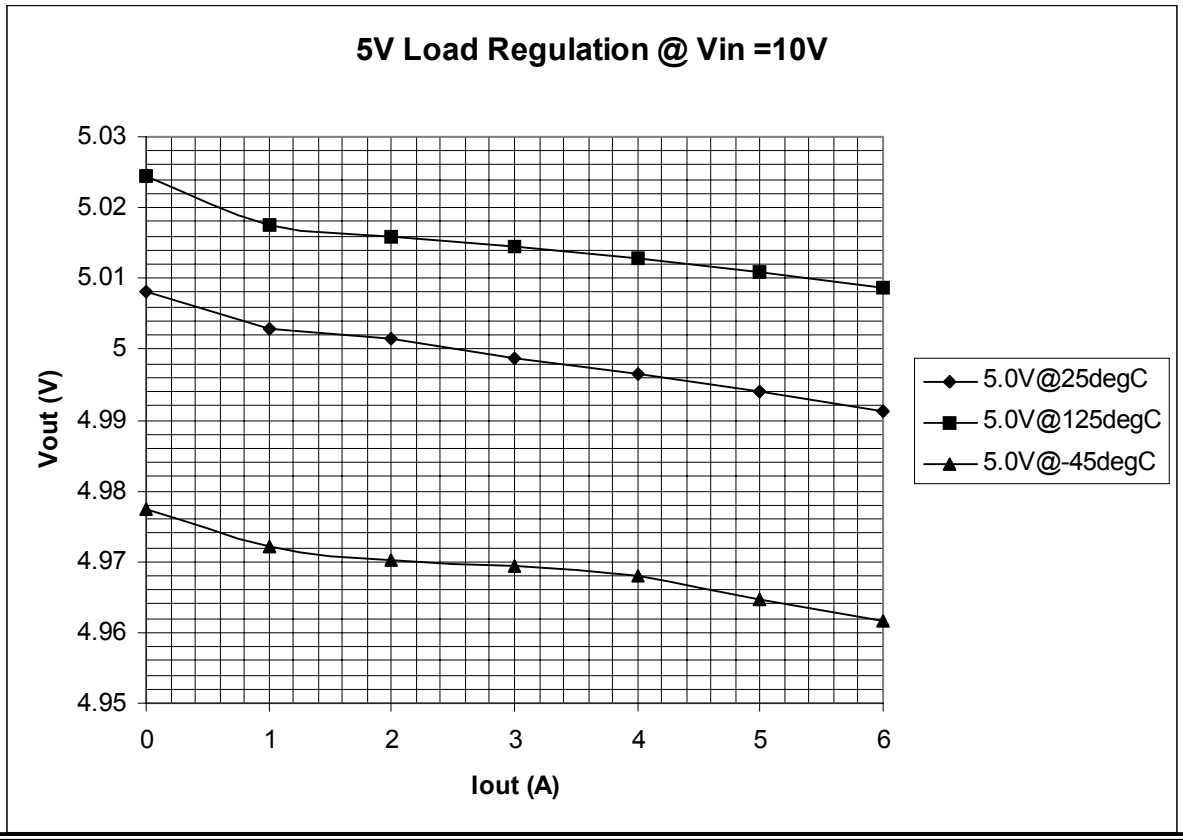
Typical Characteristics

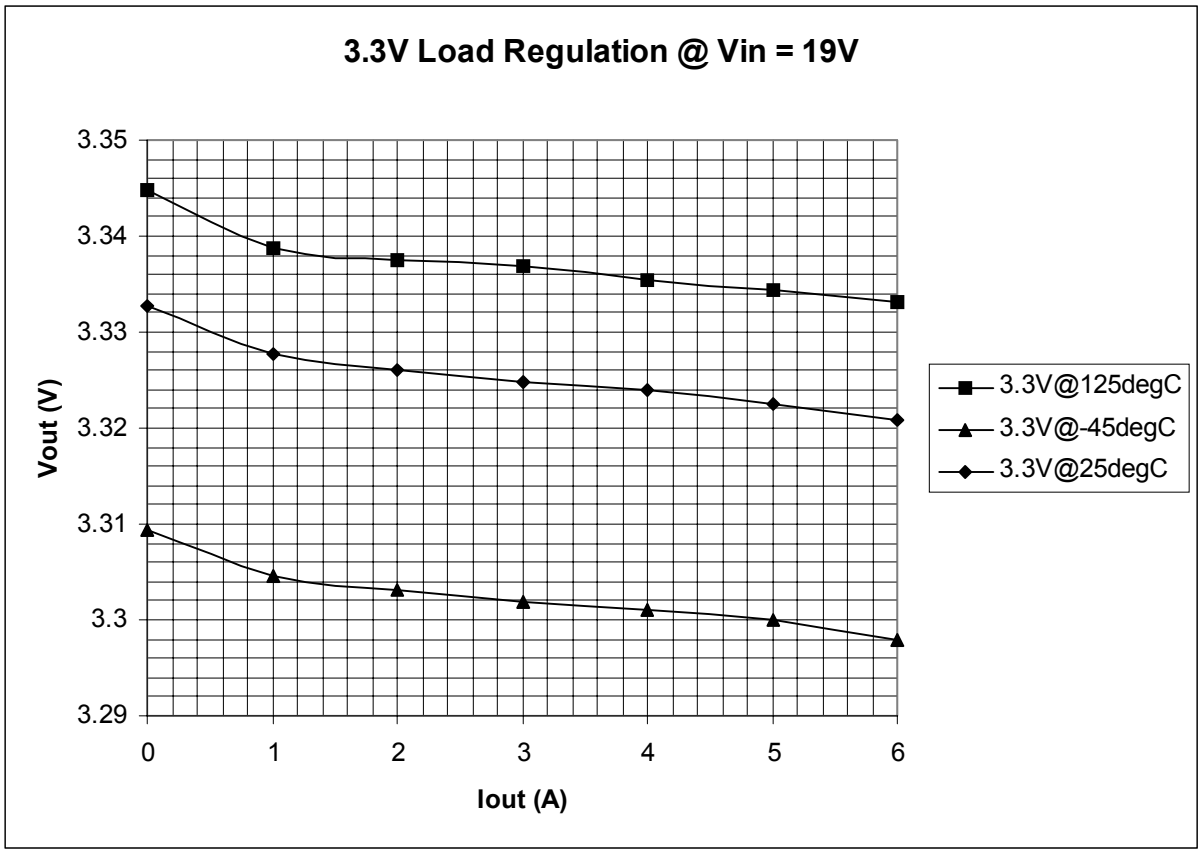


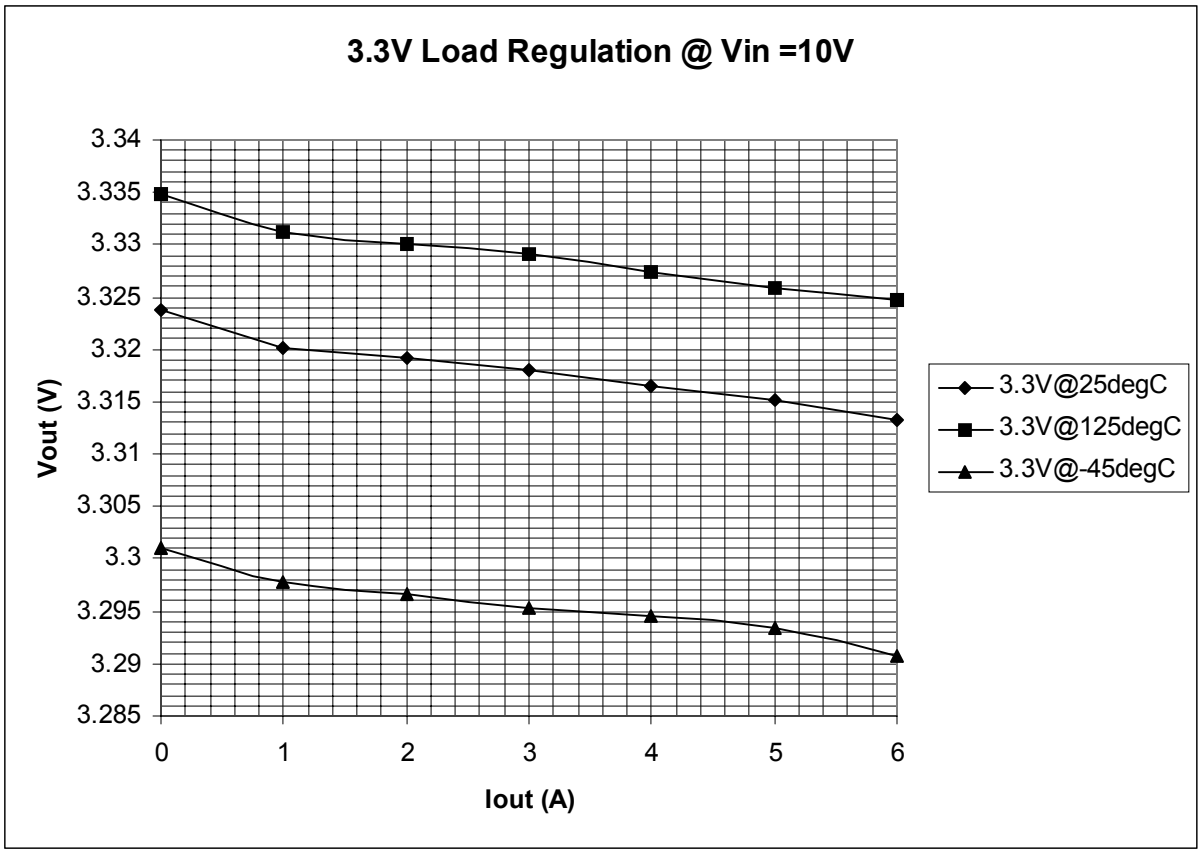


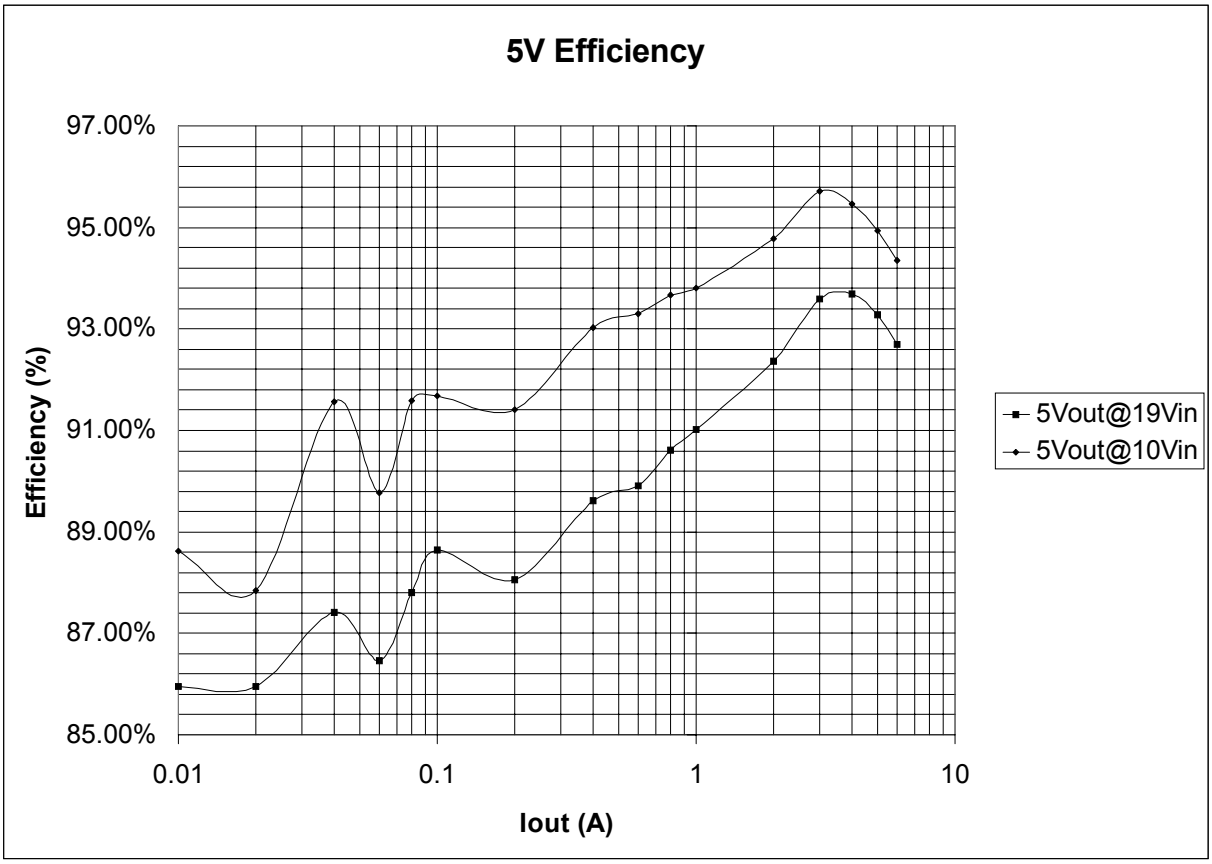
Typical Characteristics (Cont.)

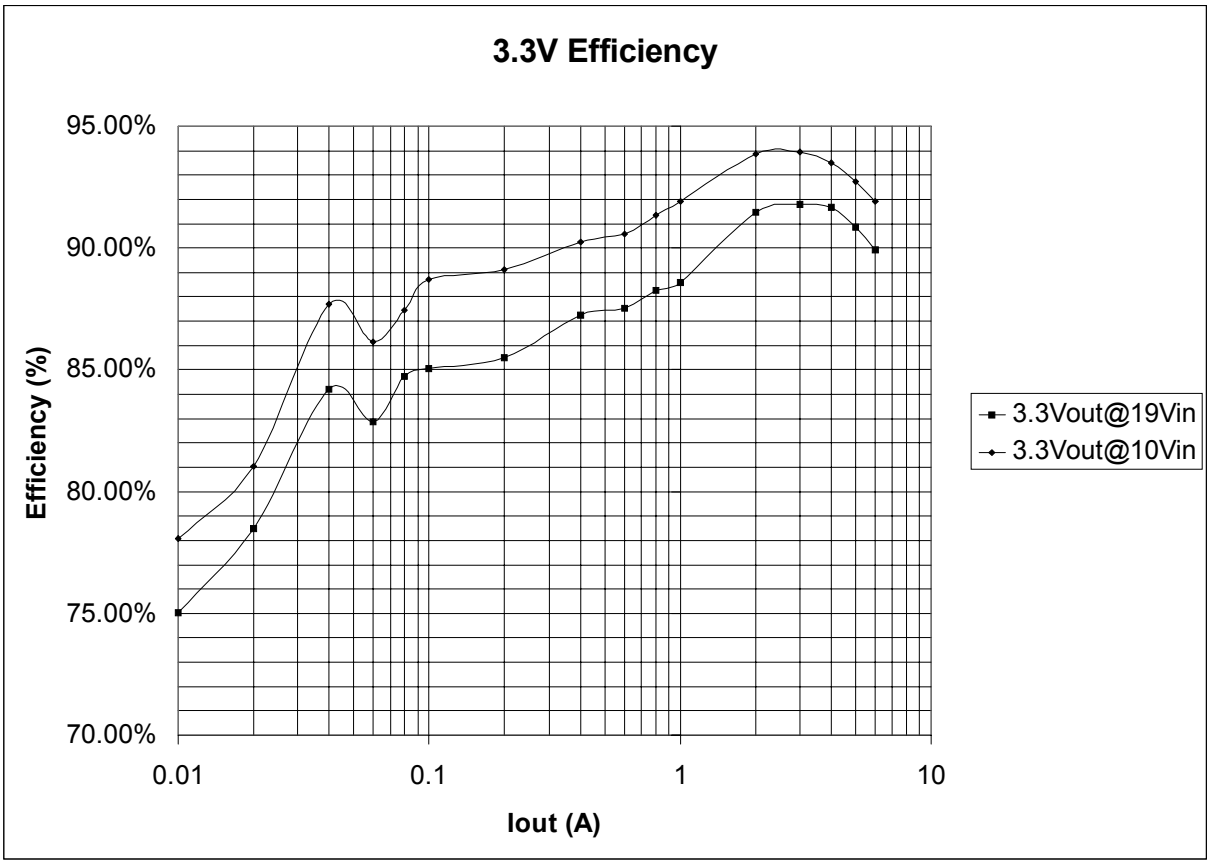




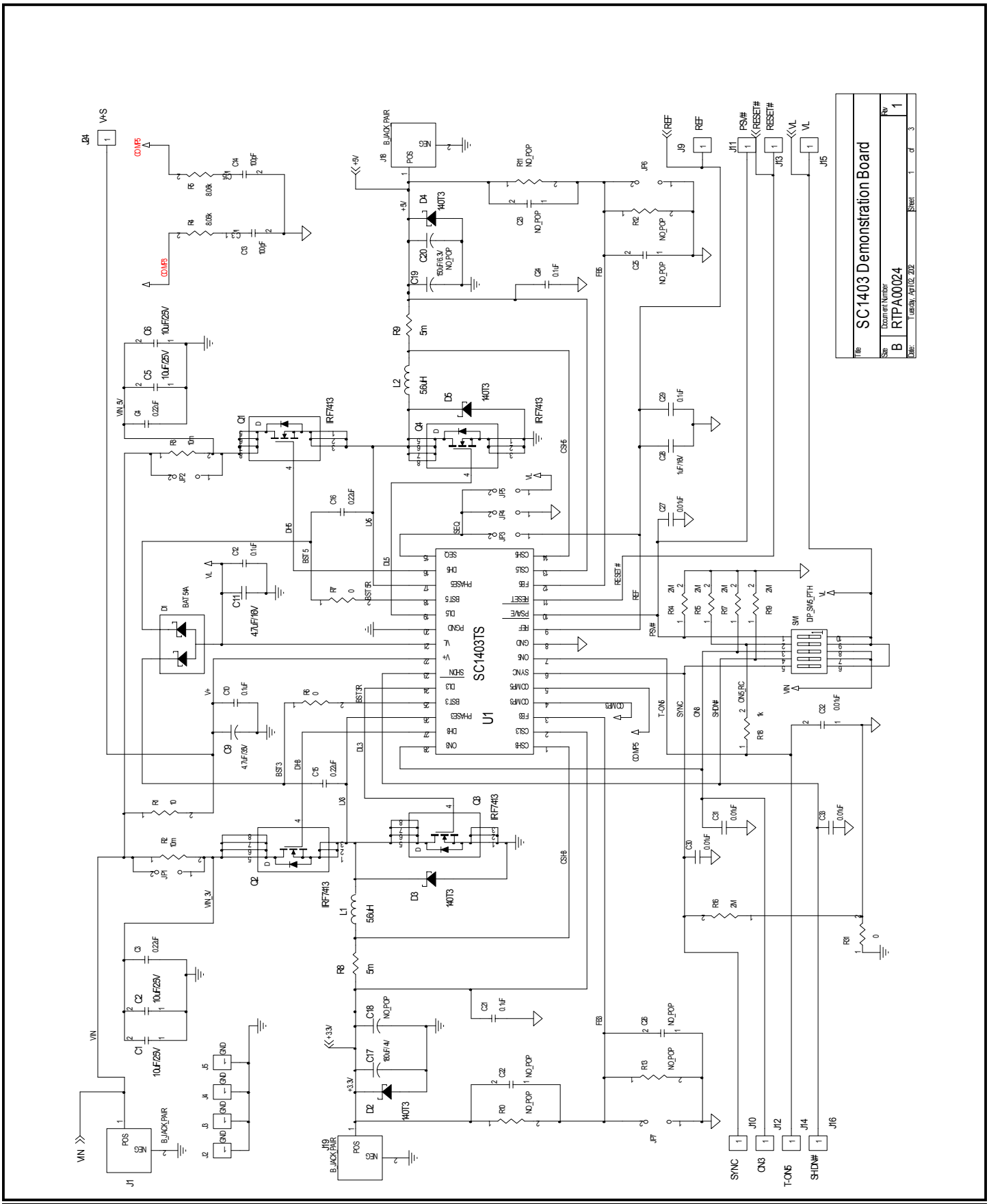

3.3V Load Regulation @ Vin = 19V
Vout (V)
3.35
3.34
3.33
3.32
3.31
3.3
3.29
0
1
2
3
4
5
6
Iout (A)
3.3V@125degC
3.3V@-45degC
3.3V@25degC


3.3V Load Regulation @ Vin =10V
Vout (V)
3.34
3.335
3.33
3.325
3.32
3.315
3.31
3.305
3.3
3.295
3.29
3.285
0
1
2
3
4
5
6
Iout (A)
3.3V@25degC
3.3V@125degC
3.3V@-45degC


5V Efficiency
97.00%
95.00%
93.00%
91.00%
89.00%
87.00%
85.00%
Efficiency (%)
0.01
0.1
1
10
Iout (A)
5Vout@19Vin
5Vout@10Vin


3.3V Efficiency
95.00%
90.00%
85.00%
80.00%
75.00%
70.00%
Efficiency (%)
0.01
0.1
1
10
Iout (A)
3.3Vout@19Vin
3.3Vout@10Vin

Evaluation Board Schematic



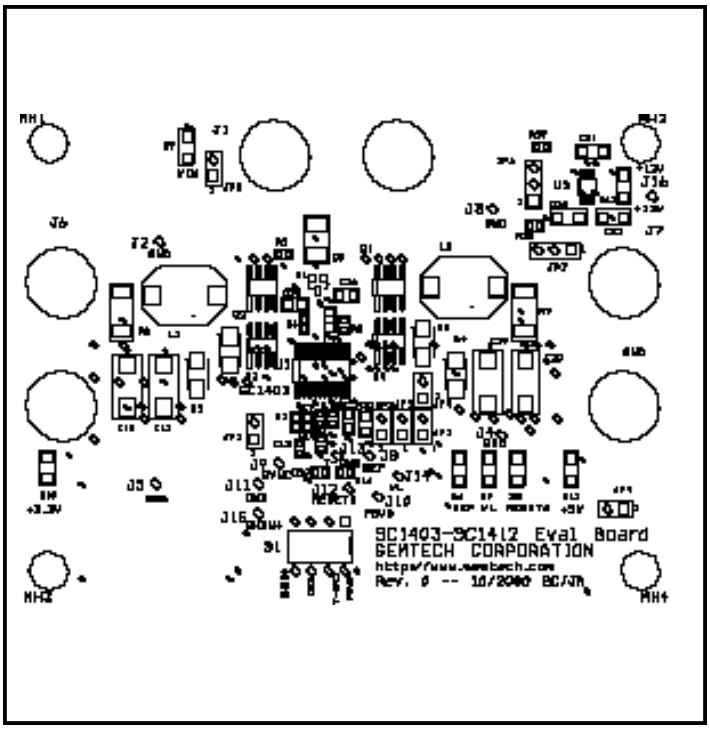
Evaluation Board Bill of Materials

Item	Quanity	Designation	Part Number	Description	Manufacturer	Device
1	1	C25	ECJ3FB1C105	1uF, 16V	Panasonic	1206
2	1	C17	EEF-UE0G181R	180uF, 4V	Panasonic	D_Case_7343
3	1	C19	EEF-UE0J151R	150uF, 6.3V	Panasonic	D_Case_7343
4	2	C28, C29	ECJ2FB1A105K	1uF, 10V	Panasonic	805
5	1	D1	BAT54A	30V, 200ma, dual C_Anode	Zetex	SOT-23
6	4	D2,D3,D4,D5	MBRS140T3	40V, 1A Schottky	Motorola	SMB
7	7	D6, D7, D8, D9, D10, D11, D12	APTR3216	Surface mount LED	Kingbright	1206
8	7	JP1, JP2, JP3, JP4, JP5, JP8, JP9		2 Pin Berg Connector	Berg	
9	2	JP6, JP7,		3Pin Berg Connector	Berg	
10	3	J1, J6, J7		Banana Jack Pair		
11	13	J2, J3, J4, J5, J8, J10, J11, J12, J13, J14, J15,2J9		Test Points		
12	2	L1, L2	SSLI306T-5R6M-S	SMT Inductor 5.6uH	Yageo/Act	
13	4	Q1, Q2, Q3, Q4	IRF7413	30V N-channel MOSFET	International Rectifier	SO8
14	3	Q5, Q6, Q7,	MMBF170LT1	500mA, 60V N-channel FET	On-Semiconductor	SOT23
15	1	R1	Any	10ohm	Any	603
16	2	R4, R5	Any	0ohm	Any	603
17	2	R6, R7	WSL2512R0055FB43	5.5mohm	Vishay Dale	2512
18	4	R14, R12, R15, R17	Any	2Megohm	Any	603
19	2	R28, R16	Any	1Kohm	Any	603
20	4	R21, R23, R25, R26	Any	2.37ohm	Any	603
21	2	R18, R19	Any	10Kohm	Any	603
22	1	SW1	BD04	4-position Dip Switch	C & K	
23	1	U1	SC1403TS	Mobile PWM Controller with VCS	SEMTECH	TSSOP28
24	1	U3	SC1412	Regulated Charge Pump with 120mA Output	SEMTECH	MSOP10

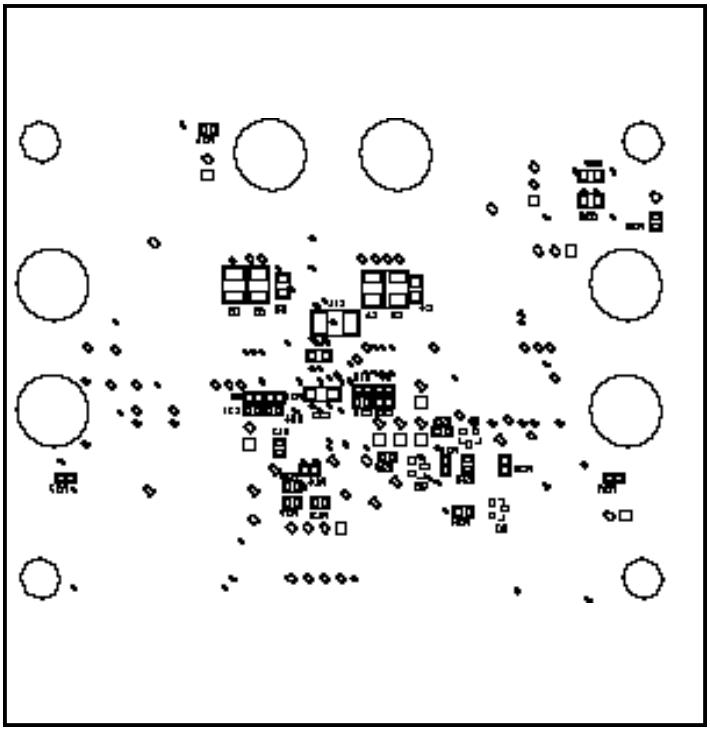
Evaluation Board Bill ofMaterials

Item	Quantity	Designator	Part Number	Description	Manufacturing	Device
25	4d	C1,C2,C5,C6	GRM230Y5V106Z025	10uF, 25V	Murata	1210
26	1d	C11		4.7uF, 20V		B_case
27	5d	C10, C12, C26, C33	ECJ-2YB1H104K	0.1uF,50V, X7R	Panasonic	805
28	2d	C7, C8	ECJ-2YB1H101K	100pF, 50V, X7R	Panasonic	603
29	4d	C3, C4, C15, C16	ECJ-2VF1H224Z	0.22uF,50V, Y5V	Panasonic	805
30	2d	C13, C14	ECJ1VC1H47K	4700pF, 50V	Panasonic	603
31	3d	C30, C31, C32		10uF, 16V		1206
32	1d	C27	ECJ1VB1C104K	0.01uF,50V	Panasonic	603
33	1d	C25	ECJ3FB1C105	1uF, 16V	Panasonic	1206
34	2d	R22, R24	Any	20Kohm	Any	603
35	2d	R2, R3	Any	8.06Kohm	Any	603
36	1d	R29	Any	300ohm	Any	603
37	1d	R27	Any	130ohm	Any	603
38	1d	R13	Any	100Kohm	Any	603

Top Assembly



Bottom Assembly



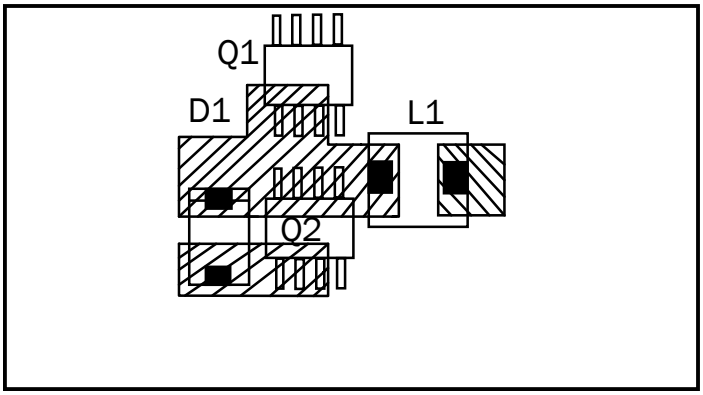
Layout Guidelines

As with any high frequency switching regulator design, a good PCB layout is very essential in order to achieve optimum noise, efficiency, and stability performance of the converter. Before starting to layout the PCB, a careful layout strategy is strongly recommended. See the PCB layout in the SC1403 Evaluation Kit manual for example. In most applications, we recommend to use FR4 with 4 or more layers and at least 2 oz copper (for output current up to 6A). Use at least one inner layer for ground connection. And it is always a good practice to tie signal ground and power ground at one single point so that the signal ground is not easily contaminated. Also be sure that high current paths have low inductance and resistance by making trace widths as wide as possible and lengths as short as possible. Properly decouple lines that pull large amounts of current in short periods of time. The following step by step layout strategy should be used in order to fully utilize the potential of SC1403.

Step #1. Power train components placement.

a. Power train arrangement.

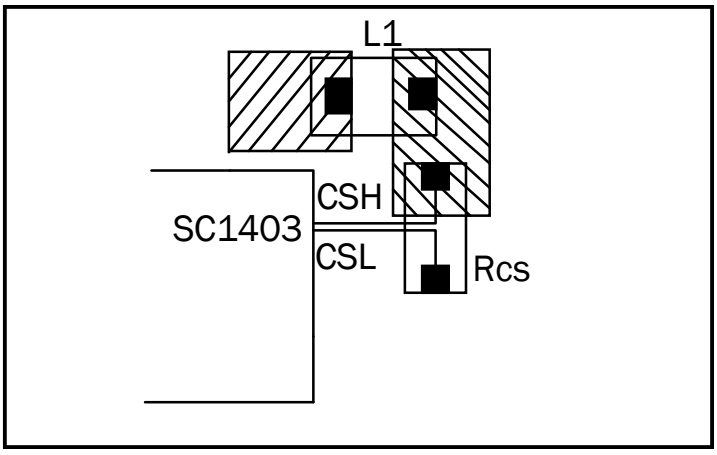
Place power train components first. The following figure shows the recommended power train arrangement. Q1 is the main switching FET, Q2 is the synchronous Rectifier FET, D1 is the Schottky diode and L1 is the output inductor. The phase node, where the source of



upper switching FET and the drain of the synchronous rectifier meets, since it switches at very high rate of speed, is generally the largest source of common-mode noise in the converter circuit. It should be kept to a minimum size consistent with its connectivity and current carrying requirements. Also place the Schottky diode as close to the phase node as possible to minimize the trace inductance, therefore reduce the efficiency loss due to the current ramp-up and down time. This becomes extremely important when converter needs to handle high di/dt requirement.

b. Current Sense.

Minimize the length of current sense signal trace. Keep it less than 15mm. Kevin connection should be used and try to keep the traces parallel to each other and have them close to each other as much as possible. Even though SC1403 implements Virtual Current Sense scheme, output signal is sampled by the SC1403 to determine the PSAVE threshold. See the following figure for Kelvin connection for current sense signal hook up.



c. Gate Drive.

SC1403 has built-in gate drivers capable of sinking/sourcing 1A pk-pk. Upper gate drive signals are noisier than the lower ones. Therefore, place them away from sensitive analog circuitries. Make sure the lower gate traces are as close as possible to the IC pins and both upper and lower gate traces as wide as possible.

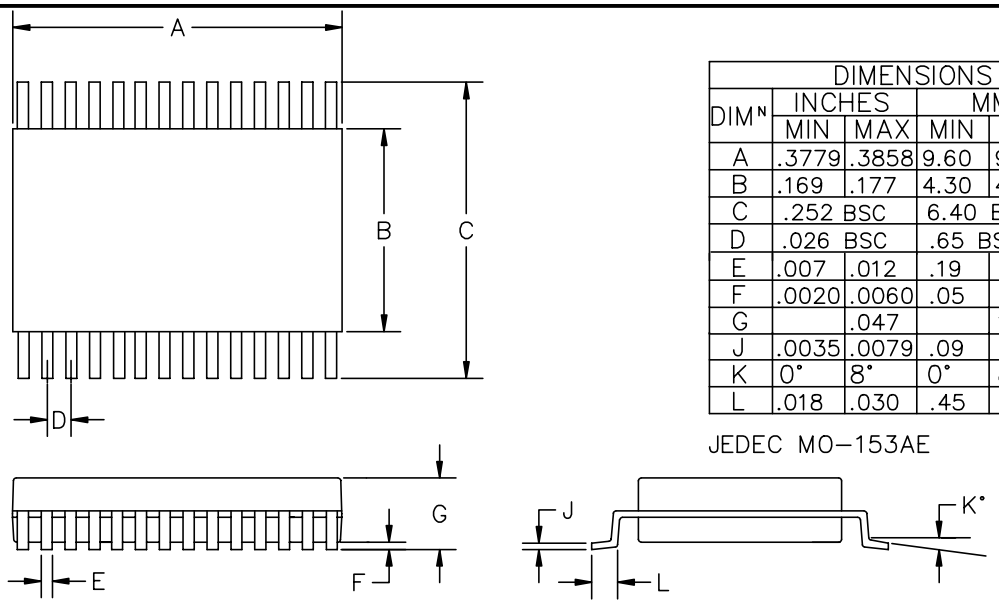
Step #2: PWM controller placement (pins) and signal ground island.

Connect all analog grounds to a separate solid copper island plane, which connects to the SC1403's GND pin. This includes REF, FB3, FB5, COMP3, COMP5, SYNC, ON3, ON5, PSV# and RESET#.

Step #3: Ground plane arrangement.

There are several ways to tie the different grounds together. Analog Ground, Power Ground for the input side and Power Ground for the output side. Since this is a buck topology converter, the output is relatively quieter than the input side. That is where we choose to tie the analog ground to the power ground through a 0Ω resistor. The power ground for the input side and the power ground for the output side is the same ground and they can be tied together using internal planes.

Outline Drawing - TSSOP-28



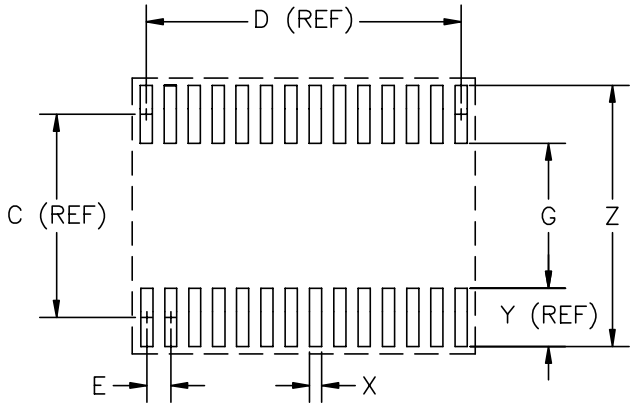
DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3779	.3858	9.60	9.80	[2]
B	.169	.177	4.30	4.50	[2]
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0020	.0060	.05	.15	—
G		.047		1.20	—
J	.0035	.0079	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—

JEDEC MO-153AE

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-28



DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.218	—	5.53	REF
D	—	.333	—	8.45	REF
E	—	.026	—	0.65	BSC
G	.155	—	3.947	—	—
X	—	.013	—	0.323	—
Y	—	.062	—	1.583	REF
Z	—	.280	—	7.113	—

[2] GRID PLACEMENT COURTYARD IS 18 X 15 ELEMENTS (9mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804