19-2362; Rev 1; 3/02

MAXIM

2.5Gbps, Low-Power, +3.3V Clock Recovery and Data Retiming IC

General Description

The MAX3875A is a compact, low-power clock recovery and data retiming IC for 2.488Gbps SDH/SONET applications. The fully integrated phase-locked loop recovers a synchronous clock signal from the serial NRZ data input, which is retimed by the recovered clock. Differential PECL-compatible outputs are provided for both clock and data signals, and an additional 2.488Gbps serial input is available for system loopback diagnostic testing. The device also includes a TTL-compatible loss-of-lock ($\overline{LOL}$) monitor.

The MAX3875A is designed for both section-regenerator and terminal-receiver applications in OC-48/STM-16 transmission systems. Its jitter performance exceeds all of the SONET/SDH specifications.

This device operates from a single +3.3V to +5.0V supply over a -40°C to +85°C temperature range. The typical power consumption is only 400mW with a +3.3V supply. It is available in a 32-pin TQFP package, as well as in die form.

Applications

SDH/SONET Receivers and Regenerators

Add/Drop Multiplexers

Digital Cross-Connects

2.488Gbps ATM Receiver

Digital Video Transmission

SDH/SONET Test Equipment

Features

- **Exceeds ANSI, ITU, and Bellcore SONET/SDH Regenerator Specifications**
- **400mW Power Dissipation (at +3.3V)**
- **Clock Jitter Generation: 0.003UI$_{RMS}$**
- **Single +3.3V or +5V Power Supply**
- **Fully Integrated Clock Recovery and Data Retiming**
- **Additional High-Speed Input Facilitates System Loopback Diagnostic Testing**
- **Tolerates >2000 Consecutive Identical Digits**
- **Loss-of-Lock Indicator**
- **Differential PECL-Compatible Data and Clock Outputs**

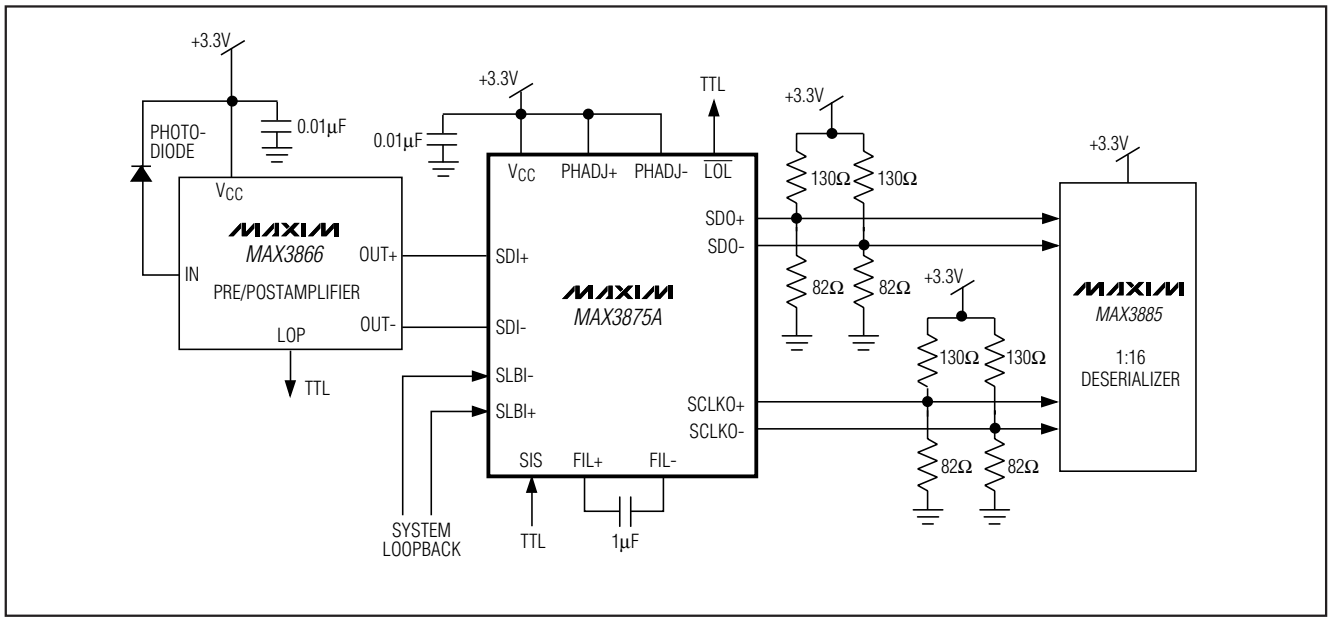
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3875AEHJ	-40°C to +85°C	32 TQFP
MAX3875AE/D	-40°C to +85°C	Dice*

** Dice are designed to operate over this range, but are tested and guaranteed at T_A = +25°C only. Contact factory for availability.*

Pin Configuration appears at end of data sheet.

Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.5V to +7.0V
Input Voltage Levels
(SDI+, SDI-, SLBI+, SLBI-) ..... (V_{CC} - 0.5V) to (V_{CC} + 0.5V)
Input Current Levels (SDI+, SDI-, SLBI+, SLBI-) ..... ±10mA
PECL Output Voltage
(SDO+, SDO-, SCLKO+, SCLKO-) ..... (V_{CC} + 0.5V)
PECL Output Current, (SDO+, SDO-, SCLKO+, SCLKO-) 56mA
Voltage at $\overline{LOL}$, SIS, PHADJ+, PHADJ-,
FIL+, FIL- ..... -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
TQFP (derate 16.1mW/°C above +85°C) 1.0W
Operating Temperature Range
MAX3875EHJ ..... -40°C to +85°C
Operating Junction Temperature (die) ..... -55°C to +150°C
Storage Temperature Range ..... -60°C to +160°C
Processing Temperature (die) ..... +400°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	Excluding PECL output termination		122	167	mA
Differential Input Voltage (SDI±, SLBI±)	V_{ID}	Figure 1	50		800	mV_{P-P}
Single-Ended Input Voltage (SDI±, SLBI±)	V_{IS}		V_{CC} - 0.4		V_{CC} + 0.2	V
Input Termination to V_{CC} (SDI±, SLBI±)	R_{IN}			45		Ω
PECL Output High Voltage (SDO±, SCLKO±)	V_{OH}	T_A = 0°C to +85°C	V_{CC} - 1.025		V_{CC} - 0.88	V
		T_A = -40°C	V_{CC} - 1.085		V_{CC} - 0.88	
PECL Output Low Voltage (SDO±, SCLKO±)	V_{OL}	T_A = 0°C to +85°C	V_{CC} - 1.81		V_{CC} - 1.62	V
		T_A = -40°C	V_{CC} - 1.83		V_{CC} - 1.555	
TTL Input High Voltage (SIS)	V_{IH}		2.0			V
TTL Input Low Voltage (SIS)	V_{IL}				0.8	V
TTL Input Current (SIS)			-10		+10	µA
TTL Output High Voltage ($\overline{LOL}$)	V_{OH}		2.4		V_{CC}	V
TTL Output Low Voltage ($\overline{LOL}$)	V_{OL}				0.4	V

Note 1: Dice are tested at T_A = +25°C only.

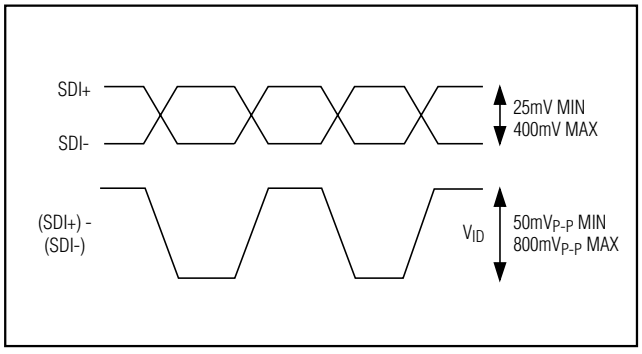


Figure 1. Input Amplitude

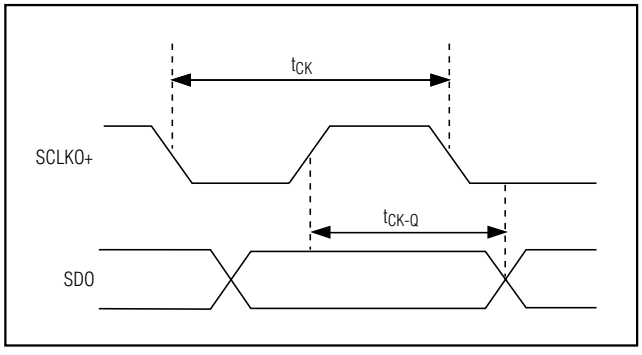


Figure 2. Output Clock-to-Q Delay

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at +3.3V and T_A = +25°C.) (Note 2)

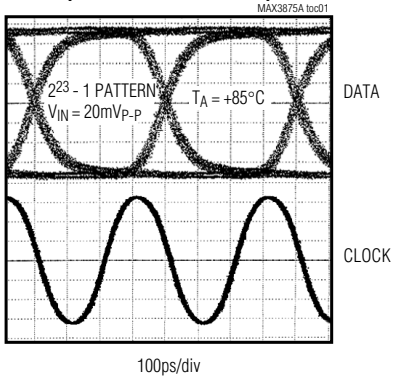
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Output Clock Rate				2.488		Gbps
Clock-to-Q Delay		Figure 2	110		290	ps
Jitter Peaking	J_P	f ≤ 2MHz			0.1	dB
Jitter Transfer Bandwidth	J_{BW}			1.1	2.0	MHz
Jitter Tolerance		f = 70kHz	1.91	3.6		UI_{P-P}
		f = 100kHz	1.76	2.75		
		f = 1MHz	0.41	0.67		
		f = 10MHz (Note 3)	0.21	0.45		
Jitter Generation	J_{GEN}	Jitter BW = 12kHz to 20MHz		0.003	0.006	UI_{RMS}
				0.026	0.056	UI_{P-P}
Clock Output Edge Speed		20% to 80%		70		ps
Data Output Edge Speed		20% to 80%		108		ps
Tolerated Consecutive Identical Digits				2000		bits
Input Return Loss (SDI±, SLBI±)		100kHz to 2.5GHz		-17		dB
		2.5GHz to 4.0GHz		-15		

Note 2: AC characteristics are guaranteed by design and characterization.
Note 3: See *Typical Operating Characteristics* for worst-case distribution.

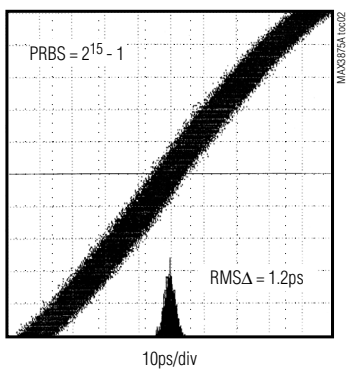
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

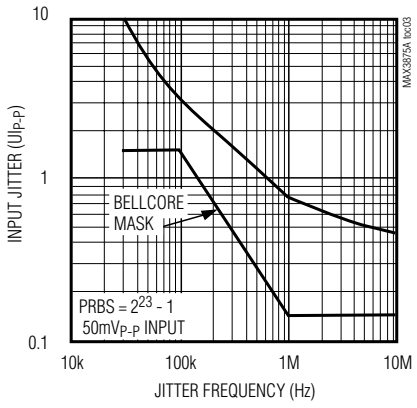
RECOVERED DATA AND CLOCK (DIFFERENTIAL OUTPUT)



RECOVERED CLOCK JITTER



JITTER TOLERANCE



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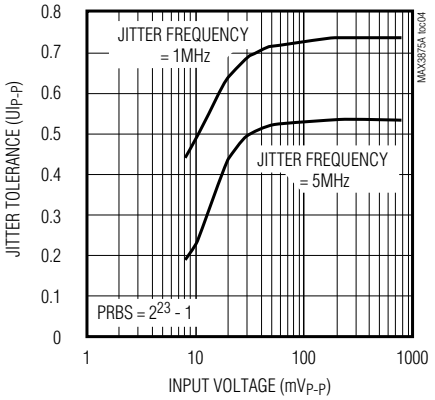
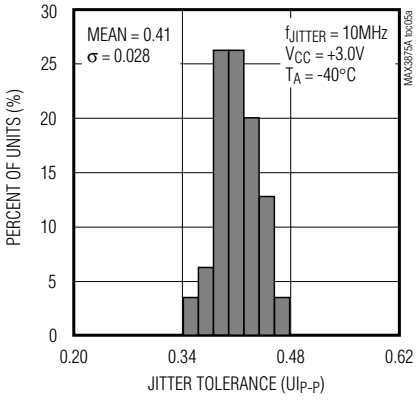
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

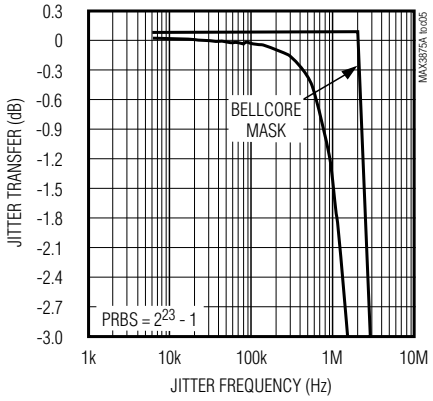
JITTER TOLERANCE vs. INPUT VOLTAGE



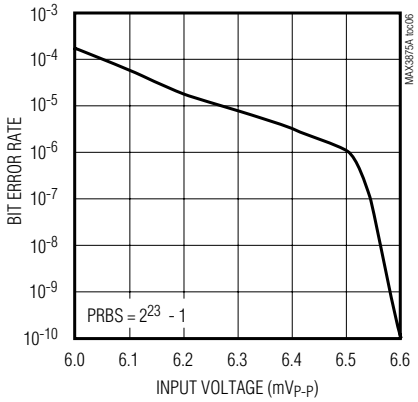
DISTRIBUTION OF JITTER TOLERANCE



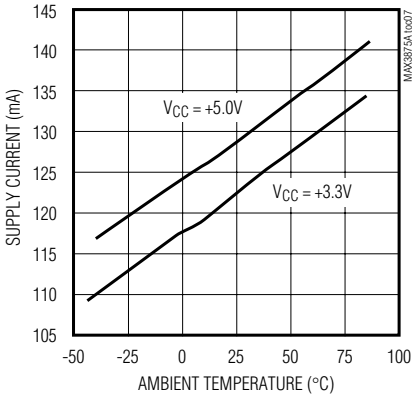
JITTER TRANSFER



BIT ERROR RATE vs. INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 2, 8, 9, 10, 16, 26, 29, 32	GND	Supply Ground
3, 6, 11, 14, 15, 17, 20, 21, 24	V_{CC}	Positive Supply Voltage
4	SDI+	Positive Data Input. 2.488Gbps serial data stream.
5	SDI-	Negative Data Input. 2.488Gbps serial data stream.
7	SIS	Signal Input Selection, TTL. Low for normal data input. High for system loopback input.
12	SLBI+	Positive System Loopback Input. 2.488Gbps serial data stream.
13	SLBI-	Negative System Loopback Input. 2.488Gbps serial data stream.
18	SCLKO-	Negative Serial Clock Output, PECL, 2.488GHz. SDO- is clocked out on the falling edge of SCLKO-.

Pin Description (continued)

PIN	NAME	FUNCTION
19	SCLKO+	Positive Serial Clock Output, PECL, 2.488GHz. SDO+ is clocked out on the rising edge of SCLKO+.
22	SDO-	Negative Data Output, PECL compatible, 2.488Gbps
23	SDO+	Positive Data Output, PECL compatible, 2.488Gbps
25	$\overline{LOL}$	Loss-of-Lock Output, TTL, PLL loss-of-lock monitor, active low (internal 10kΩ pull-up resistor)
27	PHADJ-	Negative Phase-Adjust Input. Used to optimally align internal PLL phase. Connect to V_{CC} if not used.
28	PHADJ+	Positive Phase-Adjust Input. Used to optimally align internal PLL phase. Connect to V_{CC} if not used.
30	FIL-	Negative Filter Input. PLL loop filter connection. Connect a 1.0µF capacitor between FIL+ and FIL-.
31	FIL+	Positive Filter Input. PLL loop filter connection. Connect a 1.0µF capacitor between FIL+ and FIL-.

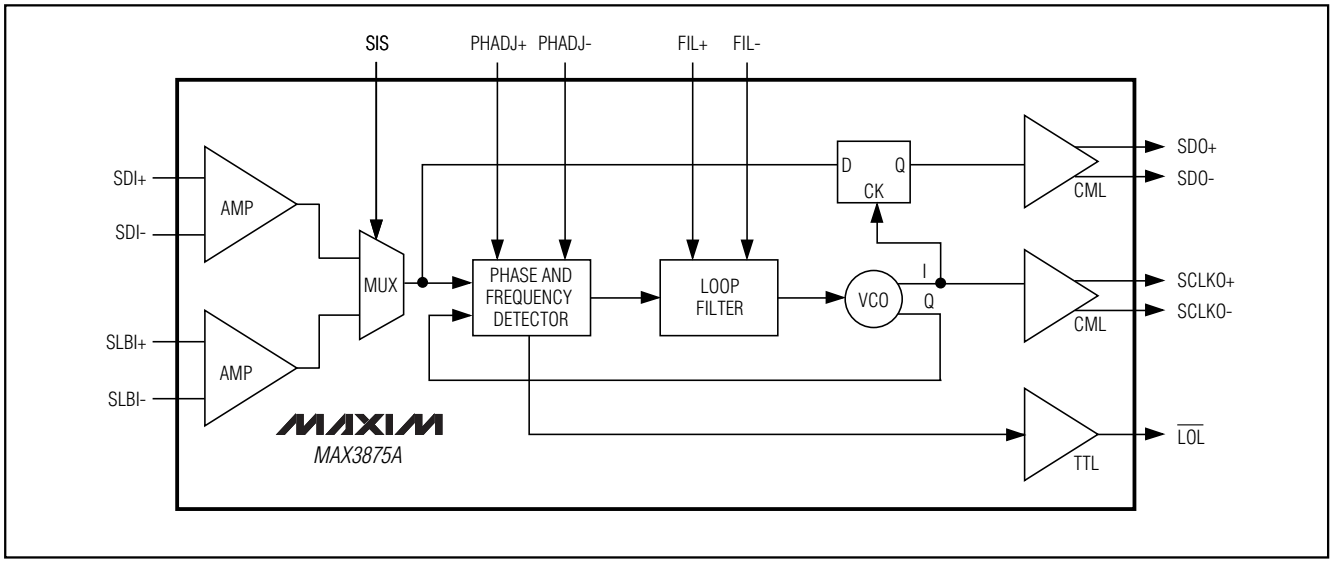


Figure 3. Functional Diagram

Detailed Description

The MAX3875A consists of a fully integrated phase-locked loop (PLL), input amplifier, data retiming block, and PECL output buffer (Figure 3). The PLL consists of a phase/frequency detector (PFD), a loop filter, and a voltage-controlled oscillator (VCO).

This device is designed to deliver the best combination of jitter performance and power dissipation by using a fully differential signal architecture and low-noise design techniques.

Input Amplifier

Input amplifiers are implemented for both the main data and system loopback inputs. These amplifiers accept a differential input amplitude from $50mV_{P-P}$ up to $800mV_{P-P}$. The bit error rate is better than 1×10^{-10} for input signals as small as 10mVp-p, although the jitter tolerance performance will be degraded. For interfacing with PECL signal levels, see *Applications Information*.

Phase Detector

The phase detector incorporated in the MAX3875A produces a voltage proportional to the phase difference between the incoming data and the internal clock. Because of its feedback nature, the PLL drives the error voltage to zero, aligning the recovered clock to the center of the incoming data eye for retiming. The external phase adjust pins (PHADJ+, PHADJ-) allow the user to vary the internal phase alignment.

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Frequency Detector

The digital frequency detector (FD) aids frequency acquisition during start-up conditions. The frequency difference between the received data and the VCO clock is derived by sampling the in-phase and quadrature VCO outputs on both edges of the data input signal. Depending on the polarity of the frequency difference, the FD drives the VCO until the frequency difference is reduced to zero. Once frequency acquisition is complete, the FD returns to a neutral state. False locking is completely eliminated by this digital frequency detector.

Loop Filter and VCO

The phase detector and frequency detector outputs are summed into the loop filter. An external capacitor, C_F, is required to set the PLL damping ratio. Refer to *Design Procedure* for guidelines on selecting this capacitor.

The loop filter output controls the on-chip LC VCO running at 2.488GHz. The VCO provides low phase noise and is trimmed to the correct frequency. Clock jitter generation is typically $1.2ps_{RMS}$ within a jitter bandwidth of 12kHz to 20MHz.

Loss-of-Lock Monitor

A loss-of-lock ($\overline{LOL}$) monitor is incorporated in the MAX3875A frequency detector. A loss-of-lock condition is signaled immediately with a TTL low. When the PLL is frequency locked, $\overline{LOL}$ switches to TTL high in approximately 800ns.

Note that the $\overline{LOL}$ monitor is only valid when a data stream is present on the inputs to the MAX3875A. As a result, $\overline{LOL}$ does not detect a loss-of-power condition resulting from a loss of the incoming signal.

Design Procedure

Setting the Loop Filter

The MAX3875A is designed for both regenerator and receiver applications. Its fully integrated PLL is a classic second-order feedback system, with a loop bandwidth (f_L) fixed at 1.1MHz. The external capacitor, C_F, can be adjusted to set the loop damping. Figures 4 and 5 show the open-loop and closed-loop transfer functions.

The PLL zero frequency, f_Z, is a function of external capacitor C_F, and can be approximated according to:

$$f_Z = \frac{1}{2\pi(60)\,C_F}$$

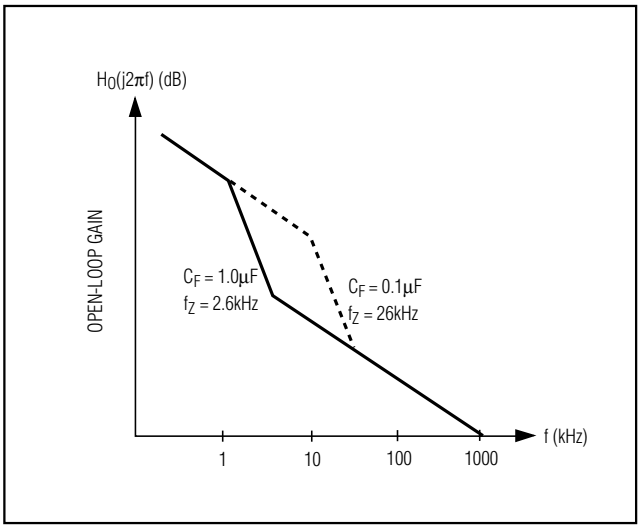

Figure 4. Open-Loop Transfer Function

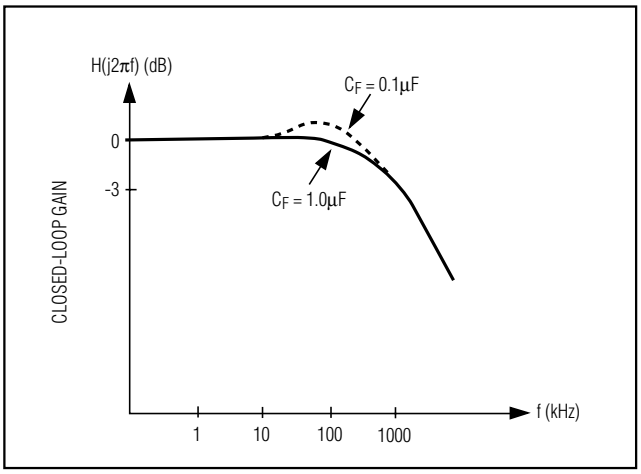

Figure 5. Closed-Loop Transfer Function

For an overdamped system (f_Z/f_L) < 0.25, the jitter peaking (M_P) of a second-order system can be approximated by:

$$M_P = 20\log\left(1+\frac{f_Z}{f_L}\right)$$

For example, using C_F = 0.1µF results in a jitter peaking of 0.2dB. Reducing C_F below 0.01µF may result in PLL instability. The recommended value for C_F = 1.0µF to guarantee a maximum jitter peaking of less than 0.1dB. C_F must be a low TC, high-quality capacitor of type X7R or better.

Input and Output Terminations

The MAX3875A's digital outputs (SDO+, SDO-, SCLKO+, SCLKO-) are designed to interface with PECL signal levels. It is important to bias these ports appropriately. A circuit that provides a Thevenin equivalent of 50Ω to V_{CC} - 2V can be used with fixed impedance transmission lines for proper termination. To ensure best performance, the differential outputs must have balanced loads. The input termination can be driven differentially, or can be driven single-ended by externally biasing SDI- or SLBI- to the center of the voltage swing.

Jitter Tolerance and Input Sensitivity Trade-Offs

When the received data amplitude is higher than 50mV$_{P-P}$, the MAX3875A provides a typical jitter tolerance of 0.45UI at jitter frequencies greater than 10MHz. The SDH/SONET jitter tolerance specification is 0.15UI, leaving a jitter allowance of 0.3UI for receiver preamplifier and postamplifier design.

The BER is better than 1 x 10^{-10} for input signals greater than 10mV$_{P-P}$. At 10mV$_{P-P}$, jitter tolerance will be degraded, but will still be above the SDH/SONET requirement. The user can make a trade-off between jitter tolerance and input sensitivity according to the specific application. Refer to the *Typical Operating Characteristics* for Jitter Tolerance and BER vs. Input Amplitude graphs.

Applications Information

Consecutive Identical Digits (CID)

The MAX3875A has a low phase and frequency drift in the absence of data transitions. As a result, long runs of consecutive zeros and ones can be tolerated while maintaining a BER of 1 x 10^{-10}. The CID tolerance is tested using a 2^{13} - 1 PRBS, substituting a long run of zeros to simulate the worst case. A CID tolerance of 2000 bits is typical.

Phase Adjust

The internal clock is aligned to the center of the data eye. For specific applications this sampling position can be shifted using the PHADJ inputs to optimize BER performance. The PHADJ inputs operate with differential input voltages up to ±1.5V. A simple resistor-divider with a bypass capacitor is sufficient to set these levels. When the PHADJ inputs are not used, they should be tied directly to V_{CC}.

System Loopback

The MAX3875A is designed to allow system loopback testing. The user can connect a serializer output in a transceiver directly to the SLBI+ and SLBI- inputs of the MAX3875A for system diagnostics. To select the SLBI± inputs, apply a TTL logic high to the SIS pin.

PECL Input Levels

When interfacing with differential PECL input levels, it is important to attenuate the signal while still maintaining 50Ω termination (Figure 6). AC coupling is also required to maintain the input common-mode level.

Layout

The MAX3875A's performance can be significantly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductance and using fixed-impedance transmission lines on the data and clock signals. Power-supply decoupling should be placed as close to V_{CC} as possible. Take care to isolate the input from the output signals to reduce feedthrough.

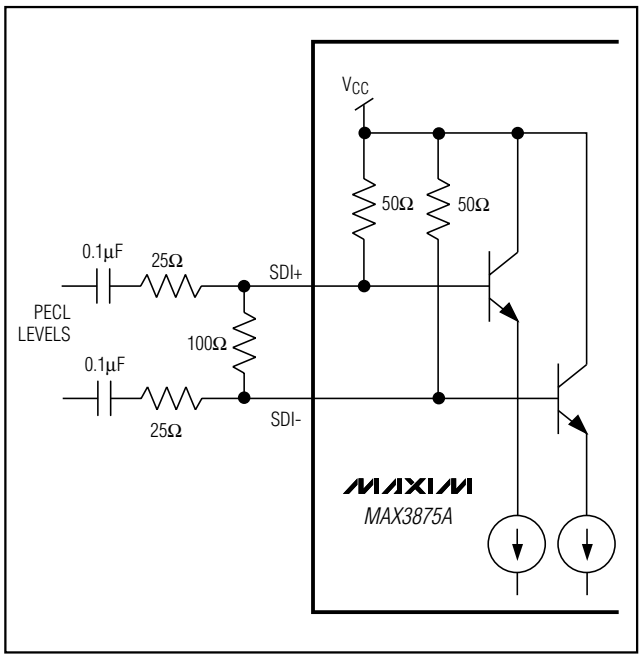

Figure 6. PECL Input Interface

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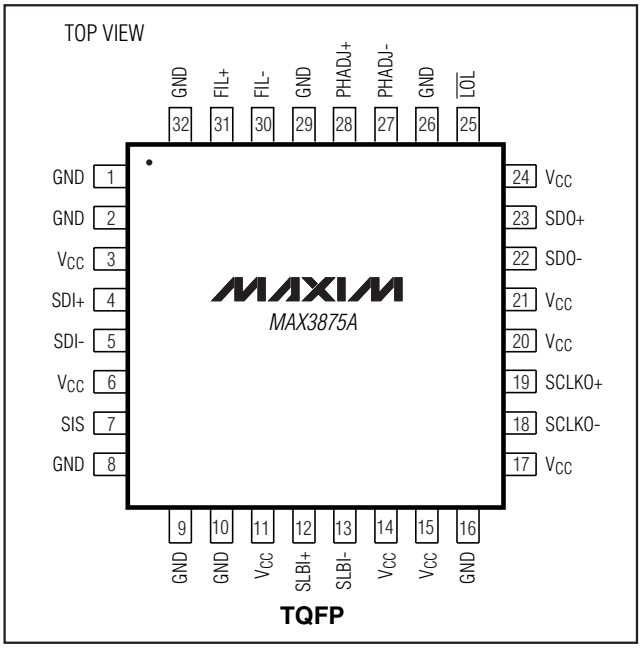
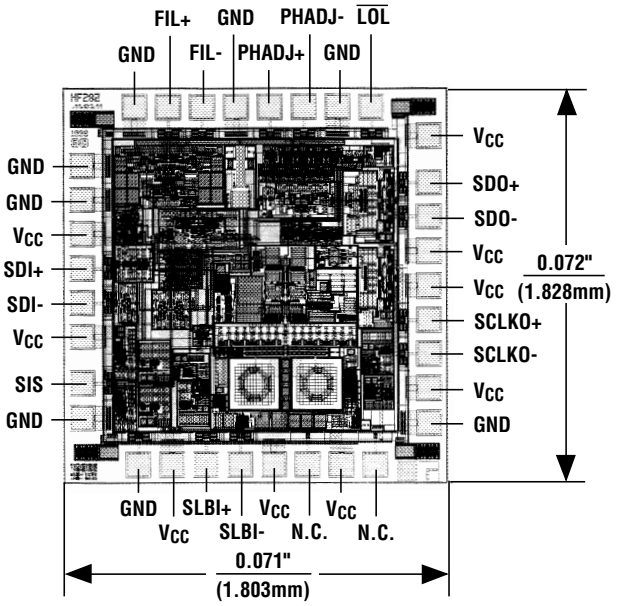
Pin Configuration



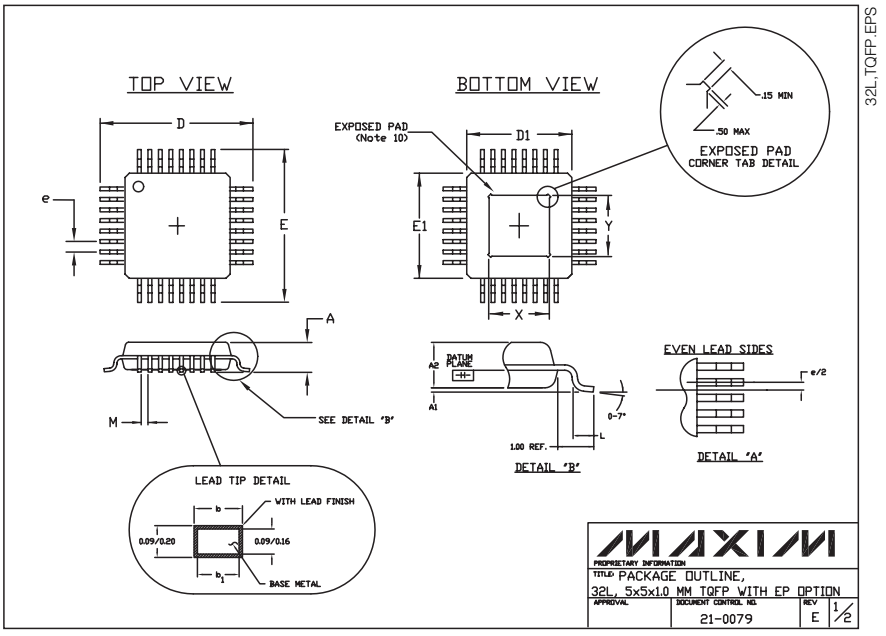
Chip Topography



TRANSISTOR COUNT: 1515

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



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