

FEATURES

- **Excellent DC Specifications**
- **Low Noise** $0.65 \mu\text{V}_{\text{p-p}}$ Typ
- **Low Drift (TCV_{OS})** $8 \mu\text{V}/^\circ\text{C}$ Max
- **Silicon-Nitride Passivation**
- **125°C Tested Dice Available**
- **"Premium" 741 Replacement**
- **Available in Die Form**

ORDERING INFORMATION [†]

$T_A = +25^\circ\text{C}$ $V_{\text{OS MAX}}$ (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	
0.5	OP02AJ*	OP02AZ*	—	MIL
2.0	OP02J/883	OP02Z	—	MIL
2.0	OP02CJ	OP02CZ	OP02CP	COM
5.0	—	—	OP02DP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[†] Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

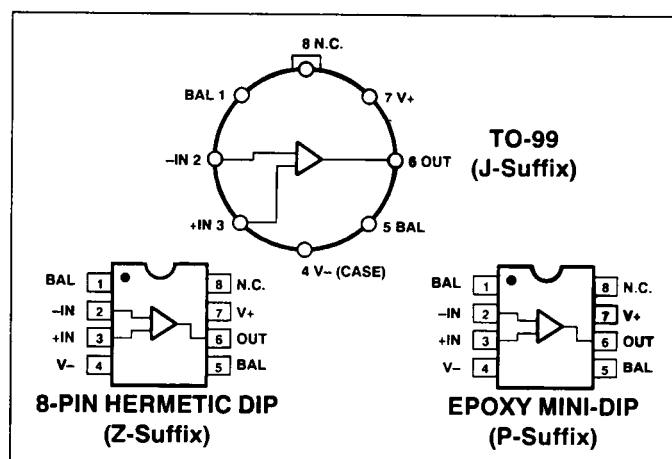
GENERAL DESCRIPTION

This high-performance general-purpose operational amplifier provides significant improvements over industry-standard and "premium" 741 types while maintaining pin-for-pin

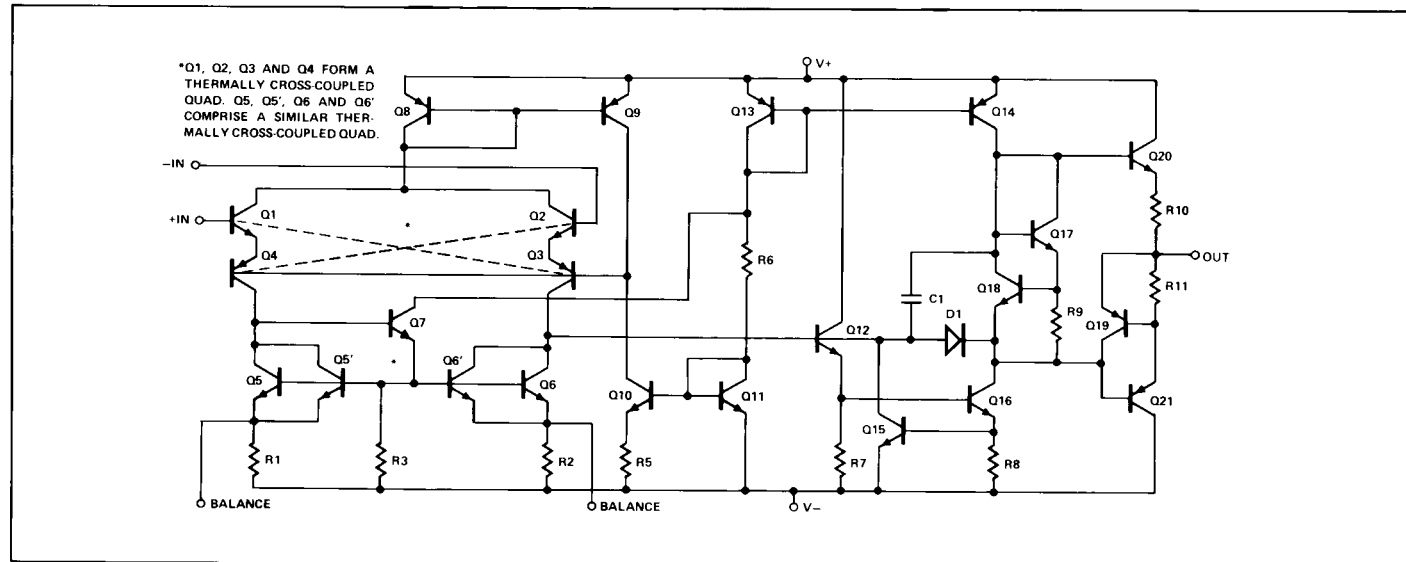
compatibility, ease of application, and low cost. Key specifications, such as V_{OS} , I_{OS} , I_{B} , CMRR, PSRR, and A_{VO} are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise." A thermally-symmetrical input-stage design provides low input offset voltage drift and insensitivity to output load conditions.

The OP-02 is a direct replacement for the 741. It is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low-drift or low-noise selected types.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



OP-02

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
OP-02A, OP-02	−55°C to +125°C
OP-02C, OP-02D	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature (T_J)	−65°C to +150°C

PACKAGE TYPE	θ_{JA} (Note 2)	θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin Plastic DIP (P)	110	50	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CerDIP and P-DIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02A			OP-02C			OP-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.5	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	2	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	30	—	20	50	—	30	100	nA
Input Resistance-Differential-Mode	R_{IN}	(Note 2)	3.4	5.7	—	2.0	5.2	—	1	3.5	—	M Ω
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption	P_d	$V_O = 0V$	—	40	70	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	25	—	—	25	—	—	25	—	nV/ $\sqrt{Hz}$
		$f_O = 100Hz$	—	22	—	—	22	—	—	22	—	
		$f_O = 1000Hz$	—	21	—	—	21	—	—	21	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA $_{p-p}$
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	pA/ $\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/ μs
Large-Signal Bandwidth		$V_O = 20V_{p-p}$ (Notes 1, 4)	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 3)	1	1.3	—	1	1.3	—	1	1.3	—	MHz
Risetime	t_r	$A_{VCL} = +1$ $V_{IN} = 50mV$ (Note 1)	—	200	350	—	200	350	—	200	350	ns
Overshoot	OS	(Note 1)	—	5	10	—	5	10	—	5	10	%

NOTES:

1. Sample tested.
2. Guaranteed by input bias current.
3. Guaranteed by maximum risetime.
4. Guaranteed by minimum slew rate.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02A			OP-02			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.5	1	—	1.4	3	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1	5	—	2	10	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	75	—	15	150	$pA/^\circ C$
Input Bias Current	I_B		—	30	60	—	40	100	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	95	—	80	95	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

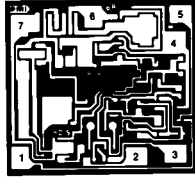
PARAMETER	SYMBOL	CONDITIONS	OP-02C			OP-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1.4	10	—	5	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	15	250	—	70	500	$pA/^\circ C$
Input Bias Current	I_B		—	25	100	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	90	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 10	± 13	—	V

NOTE:

1. Sample tested.

OP-02

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.047 × 0.043 inch, 2021 sq. mils
(1.19 × 1.09 mm, 1.30 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. NULL
6. OUTPUT
7. V₊

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-02N, OP-02G and OP-02GR devices; $T_A = 125^\circ C$ for OP-02NT and OP-02GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02NT LIMIT	OP-02N LIMIT	OP-02GT LIMIT	OP-02G LIMIT	OP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	1	0.5	3	2	5	mV MAX
Input Offset Current	I_{OS}		5	3	6	5	25	nA MAX
Input Bias Current	I_B		50	30	60	50	200	nA MAX
Input Voltage Range	IVR		± 13	± 13	± 13	± 13	± 13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	85	80	80	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	60	100	100	150	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 12	± 12	± 12	± 12	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	25	50	25	V/mV MIN
Power Consumption	P_d	$V_O = 0V$	—	90	—	90	90	mW MAX

NOTE:

For $25^\circ C$ characteristics of NT and GT devices, see N and G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

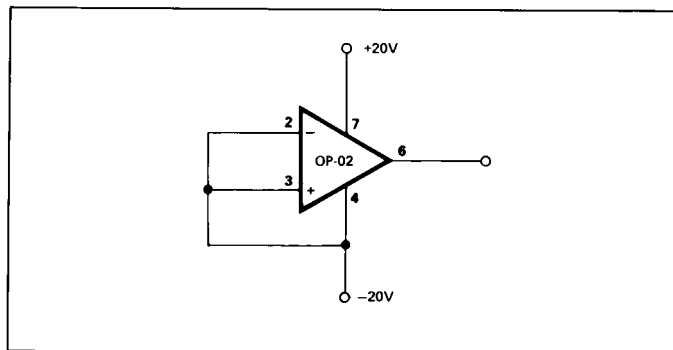
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02NT OP-02N TYPICAL	OP-02GT OP-02G TYPICAL	OP-02GR TYPICAL	UNITS
Input Resistance Differential-Mode	R_{IN}		5.7	5.2	3.5	M Ω
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.65	0.65	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	25 22 21	25 22 21	25 22 21	nV/ $\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	12.8	12.8	12.8	pA _{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	1.4 0.7 0.4	1.4 0.7 0.4	1.4 0.7 0.4	pA/ $\sqrt{Hz}$
Slew Rate	SR		0.5	0.5	0.5	V/ μs
Large-Signal Bandwidth		$V_O = 20V_{p-p}$	8	8	8	kHz
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	1.3	1.3	1.3	MHz
Risetime	t_r	$A_V = +1$ $V_{IN} = 50mV$	200	200	200	ns
Overshoot	OS		15	15	15	%
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 500\Omega$ (Note 1)	2	4	8	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		7.5	15	30	pA/ $^\circ C$

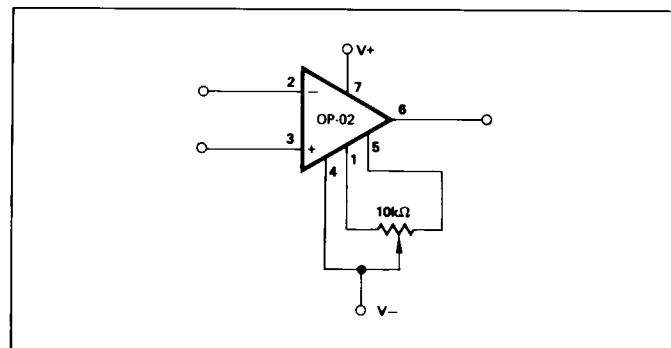
NOTE:

1. Sample tested.

BURN-IN CIRCUIT

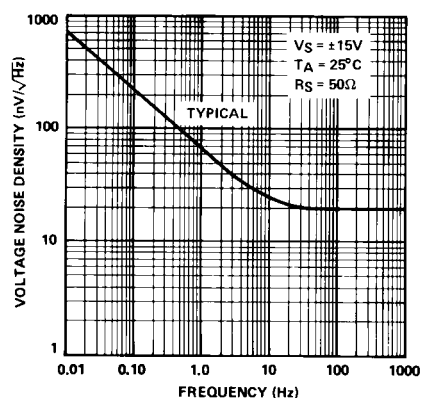


OFFSET NULLING CIRCUIT

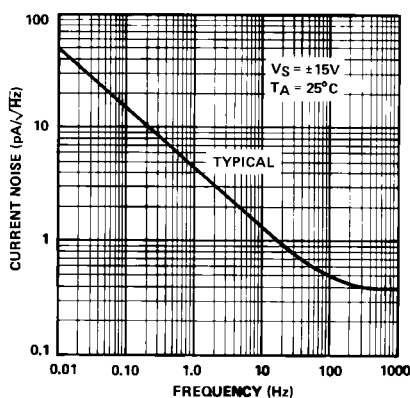


TYPICAL PERFORMANCE CHARACTERISTICS

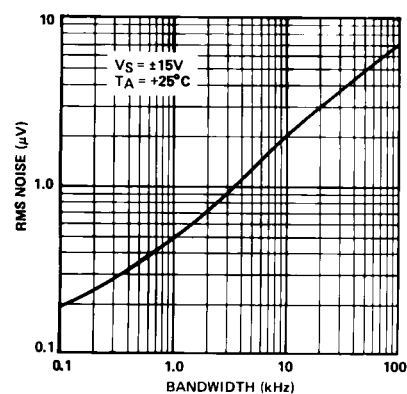
**INPUT SPOT NOISE
VOLTAGE vs FREQUENCY**



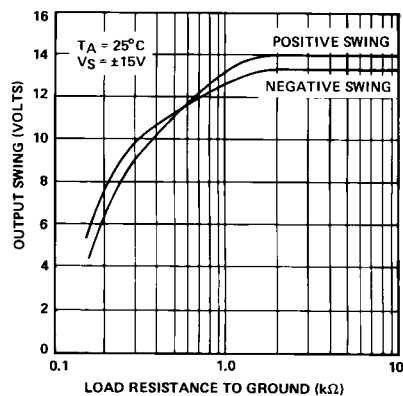
**INPUT SPOT NOISE
CURRENT vs FREQUENCY**



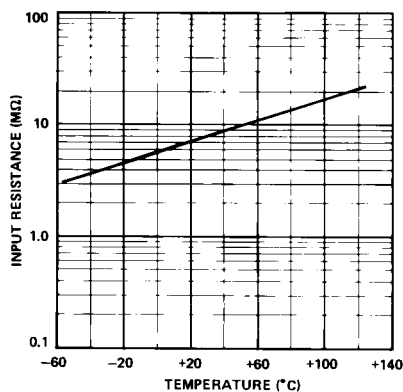
**INPUT WIDEBAND NOISE vs
BANDWIDTH (0.1Hz TO
FREQUENCY INDICATED)**



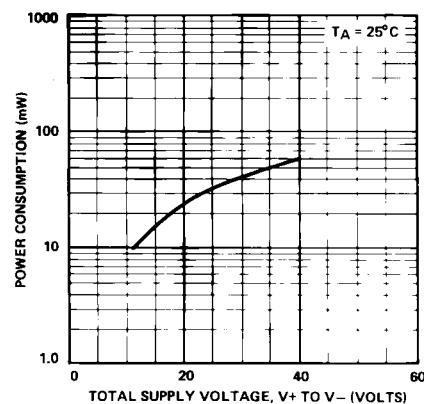
**OUTPUT VOLTAGE vs
LOAD RESISTANCE**



**DIFFERENTIAL
INPUT RESISTANCE
vs TEMPERATURE**



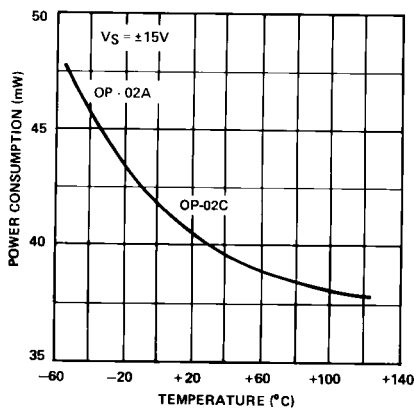
**POWER CONSUMPTION
vs POWER SUPPLY**



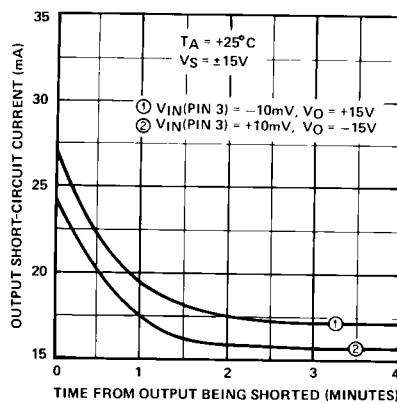
OP-02

TYPICAL PERFORMANCE CHARACTERISTICS

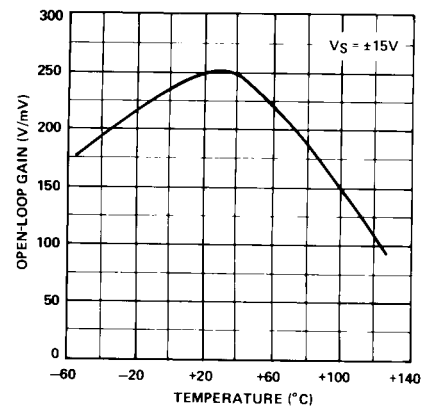
**POWER CONSUMPTION
vs TEMPERATURE**



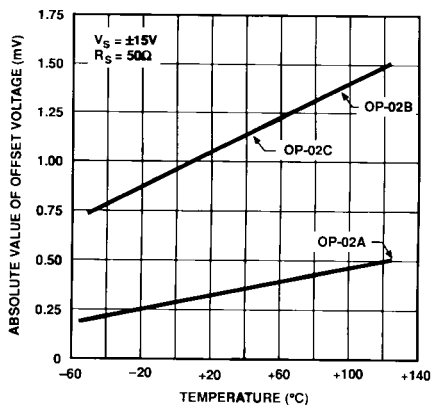
**OUTPUT SHORT-CIRCUIT
CURRENT vs TIME**



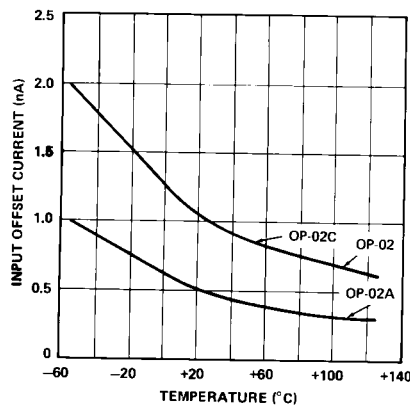
**OPEN-LOOP GAIN
vs TEMPERATURE**



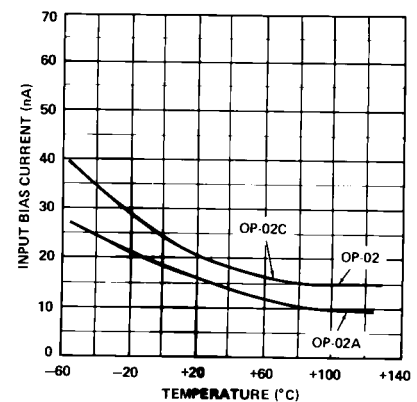
**UNTRIMMED OFFSET VOLTAGE
vs TEMPERATURE**



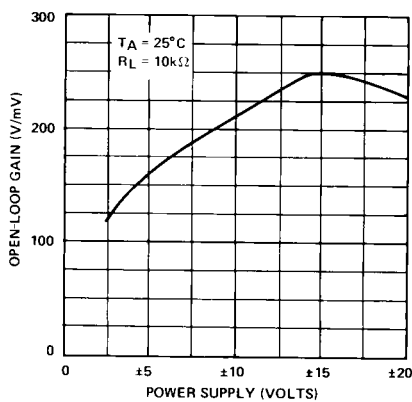
**INPUT OFFSET CURRENT
vs TEMPERATURE**



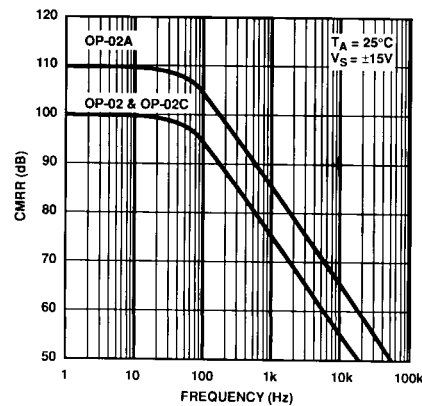
**INPUT BIAS CURRENT
vs TEMPERATURE**



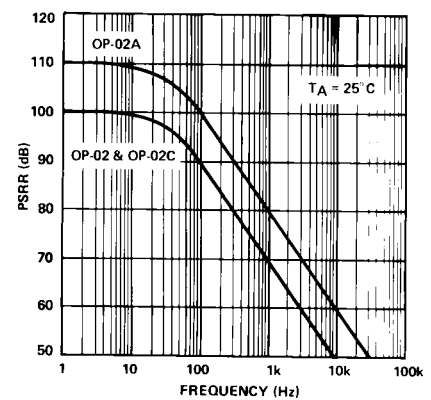
**OPEN-LOOP GAIN vs
POWER SUPPLY VOLTAGE**



CMRR vs FREQUENCY

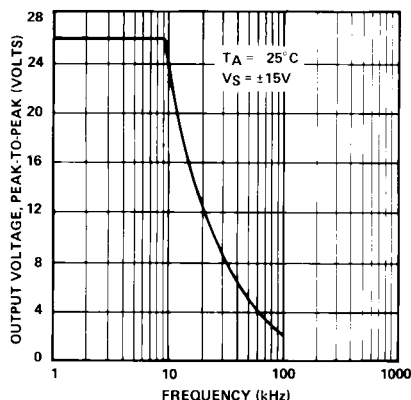


PSRR vs FREQUENCY

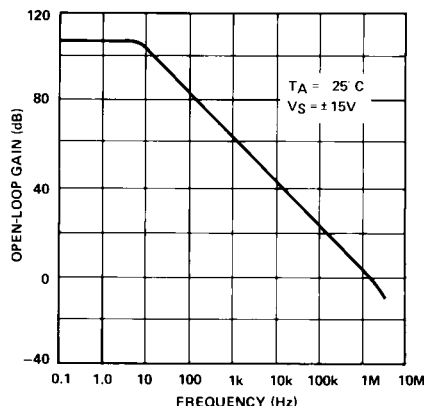


TYPICAL PERFORMANCE CHARACTERISTICS

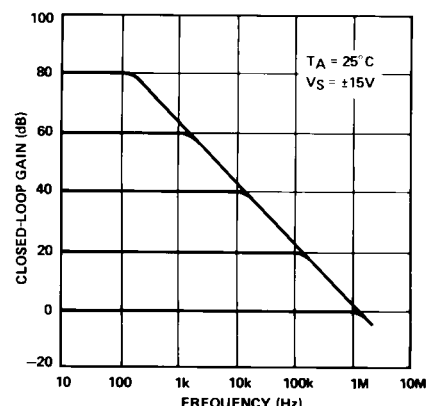
**MAXIMUM UNDISTORTED
OUTPUT vs FREQUENCY**



**OPEN-LOOP
FREQUENCY RESPONSE**

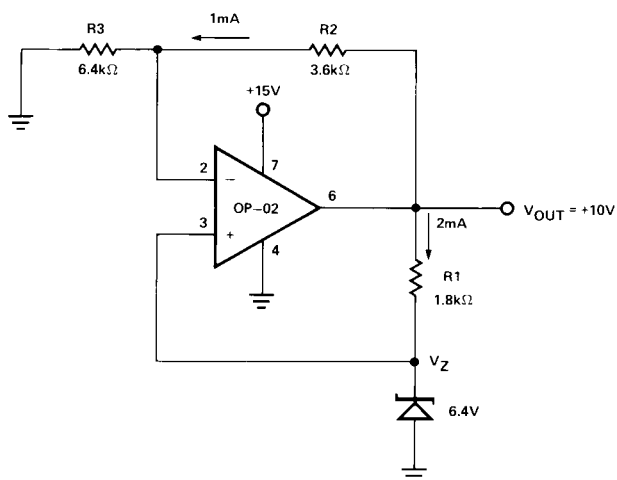


**CLOSED-LOOP RESPONSE
FOR VARIOUS GAIN
CONFIGURATIONS**



TYPICAL APPLICATIONS

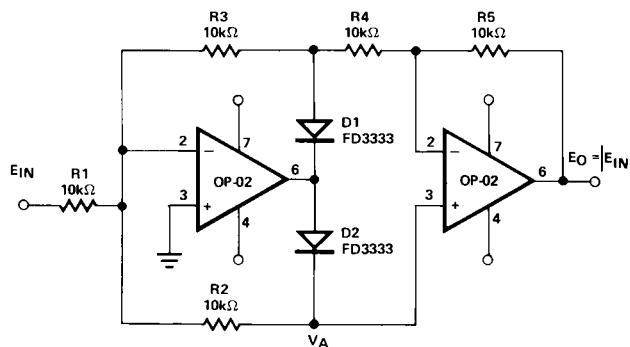
HIGH-STABILITY VOLTAGE REFERENCE



$$V_{OUT} = \left(1 + \frac{R_2}{R_3}\right) V_Z$$

FOR $R_2 = 3.6k\Omega$ AND
 $R_3 = 6.4k\Omega$,
 $V_{OUT} = 1.5625V_Z$
 IF $V_Z = 6.4V$, THEN
 $V_{OUT} = +10V$

ABSOLUTE VALUE CIRCUIT



DESIGN EQUATIONS

POSITIVE INPUT

1. $V_A = 0$, D2 OFF, D1 ON
2. $E_O = \left(\frac{-E_{IN}R_3}{R_1}\right) \cdot \left(\frac{-R_5}{R_4}\right) = E_{IN} \frac{R_3 R_5}{R_1 R_4}$
3. With $R_1 = R_3 = R_4 = R_5$: $E_O = E_{IN}$
4. VOS error included: $E_O = E_{IN} + 2V_{OS}$

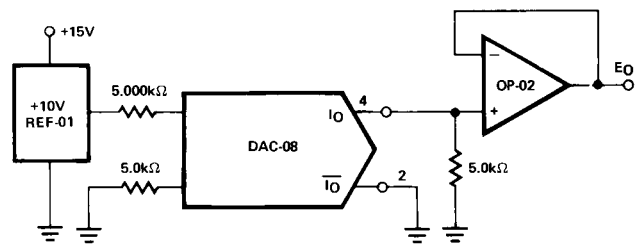
NEGATIVE INPUT

1. D1 OFF, D2 ON
2. $\frac{-E_{IN}}{R_1} = \frac{V_A}{R_2} + \frac{V_A}{R_3 + R_4}$
3. $E_O = V_A \left(1 + \frac{R_5}{R_3 + R_4}\right)$
4. With $R_3 = R_4 = R_5$: $E_O = 1.5V_A$
5. $E_O = -\frac{(R_2)(R_3 + R_4)(1.5)E_{IN}}{R_1(R_2 + R_3 + R_4)}$
6. With $R_1 = R_2 = R_3 = R_4$: $E_O = -E_{IN}$
7. VOS error included:
 $E_O = -E_{IN} + 1.5V_{OS2} - 0.5V_{OS1}$
8. For both inputs: $E_O = +|E_{IN}|$

OP-02

TYPICAL APPLICATIONS

DAC-08 OUTPUT AMPLIFIER



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC) CONNECT NON-INVERTING INPUT OF OP-AMP TO I_O (PIN 2), CONNECT I_O (PIN 4) TO GROUND.

INPUT/OUTPUT TABLE

	B1	B2	B3	B4	B5	B6	B7	B8	I _O mA	E _O
FULL-SCALE -1 LSB	1	1	1	1	1	1	1	1	1.992	-9.960
FULL-SCALE -2 LSB	1	1	1	1	1	1	1	0	1.984	-9.920
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.008	-5.040
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	-5.000
HALF-SCALE -LSB	0	1	1	1	1	1	1	1	0.992	-4.960
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	0.0008	-0.040
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	0.000