CMOS Analog Switches

(Obsolete for non-hermetic. Use DG303B as pin-for-pin replacements.)

FEATURES

- Analog Signal Range: ±15 V
- Fast Switching—t_{ON}: 150 ns
- Low On-Resistance—$r_{DS(on)}$: 30 Ω
- Single Supply Operation
- Latch-up Proof
- CMOS Compatible

BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

DESCRIPTION

The DG303A_MIL is a monolithic CMOS switch in a DPST configuration for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power consumption are required.

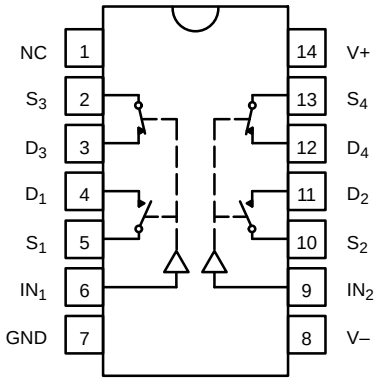
Designed on the Vishay Siliconix PLUS-40 CMOS process, these switches are latch-up proof, and are designed to block up to 30 V peak-to-peak when off. An epitaxial layer prevents latchup.

In the on condition the switches conduct equally well in both directions (with no offset voltage) and minimize error conditions with their low on-resistance.

Featuring low power consumption (3.5 mW typ) these switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, these devices are CMOS and quasi TTL compatible. Single supply operation is allowed by connecting the V– rail to 0 V.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG303A
CerDIP and Sidebraze



Top View

TRUTH TABLE		
Logic	**SW_1, SW_2**	**SW_3, SW_4**
0	OFF	ON
1	ON	OFF

Logic “0” ≤ 0.8 V
Logic “1” ≥ 4 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
–55 to 125°C	14-Pin CerDIP	DG303AAK
		DG303AAK/883
		JM38510/11604BCA
	14-Pin Sidebraze	JM38510/11604BCC

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–
V+ . . . . . 44 V
GND . . . . . 25 V
Digital Inputs[NO TAG], V_S, V_D . . . . . (V–) –2 V to (V+) +2V or 30 mA, whichever occurs first
Current, Any Terminal . . . . . 30 mA
Continuous Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) . . . . . 100 mA

Storage Temperature (A Suffix) . . . . . –65 to 150°C
Power DissipationNO TAG
14-Pin CerDIP[NO TAG] . . . . . 825 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. Derate 6.5 mW/°C above 25°C
c. Derate 11 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

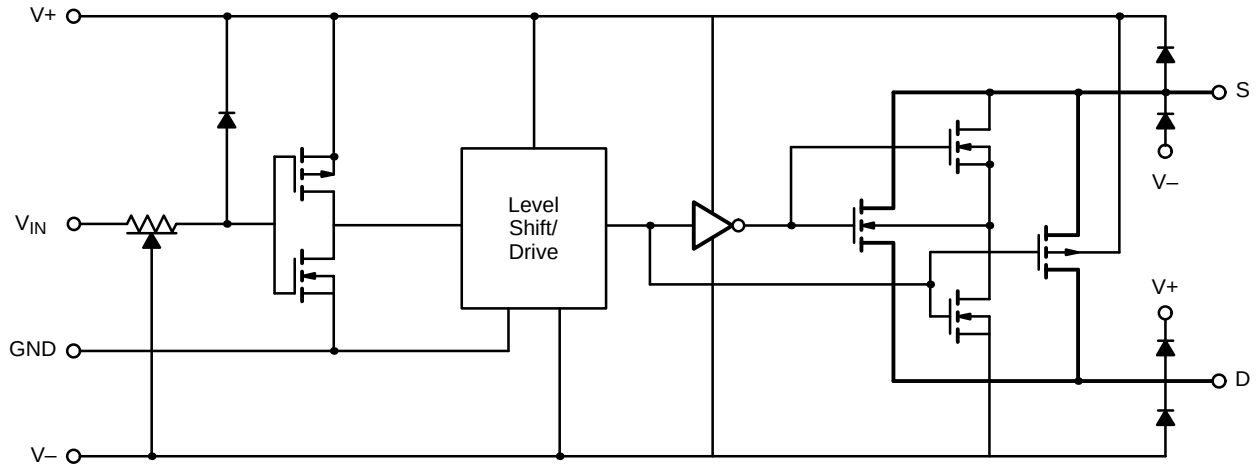


FIGURE 1.

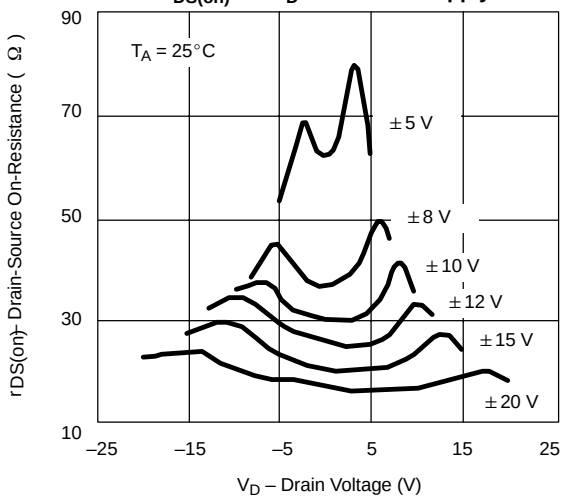
SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V– = –15 V V_{IN} = 0.8 V or V_{IN} = 4 V[f]	Temp[b]	Limits –55 to 125°C Min[d]	Typ[c]	Max[d]	Unit
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = –10 mA	Room Full		30	50 75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Hot	–1 –100	±0.1	1 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Hot	–1 –100	±0.1	1 100	nA
Drain On Leakage Current	$I_{D(on)}$	V_D = V_S = ±14 V	Room Hot	–1 –100	±0.1	1 100	nA
Digital Control							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Full	–1 –1	–0.001		µA
		V_{IN} = 15 V	Room Full		0.001	1 1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Room Full	–1 –1	–0.001		µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	See Figure NO TAG	Room		150	300	ns
Turn-Off Time	t_{OFF}	See Figure NO TAG	Room		130	250	ns
Break-Before-Make Time	t_{OPEN}	303A Only Figure NO TAG	Room		50		ns
Charge Injection	Q	C_L = 1 nF, R_{gen} = 0 Ω V_{gen} = 0 V, Figure NO TAG	Room		8		pC
Source-Off Capacitance	$C_{S(off)}$	V_S, V_D = 0 V, f = 1 MHz	Room		14		pF
Drain-Off Capacitance	$C_{D(off)}$	V_S, V_D = 0 V, f = 1 MHz	Room		14		pF
Channel-On Capacitance	$C_{D(on)}$	V_S, V_D = 0 V, f = 1 MHz	Room		40		pF
Input Capacitance	C_{in}	f = 1 MHz, V_{IN} = 0 V	Room		6		pF
		f = 1 MHz, V_{IN} = 15 V	Room		7		pF
Off-Isolation	OIRR	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz	Room		62		dB
Crosstalk (Channel-to-Channel)	X_{TALK}	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz	Room		74		dB
Power Supplies							
Positive Supply Current	I+	V_{IN} = 4 V (One Input) All Others = 0 V	Room Full		0.23	0.5 1	mA
Negative Supply Current	I–	V_{IN} = 4 V (One Input) All Others = 0 V	Room Full	–10 –100	–0.001		µA
Positive Supply Current	I+	V_{IN} = 0.8 V (All Inputs)	Room Full		0.001	10 100	µA
Negative Supply Current	I–	V_{IN} = 0.8 V (All Inputs)	Room Full	–10 –100	–0.001		µA

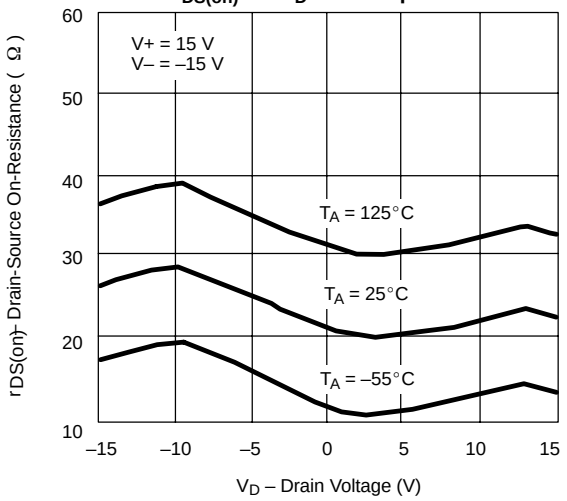
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

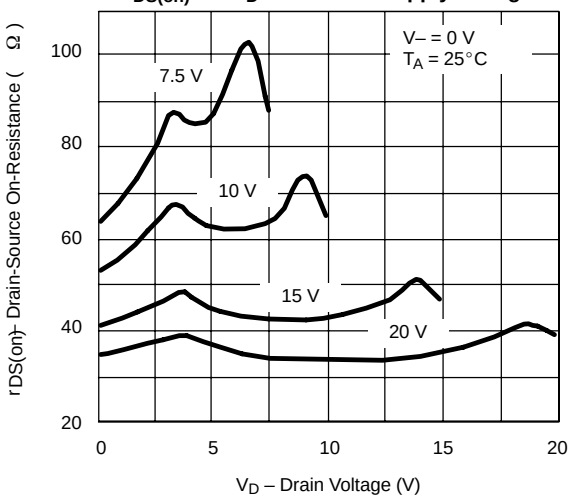
$r_{DS(on)}$ vs. V_D and Power Supply



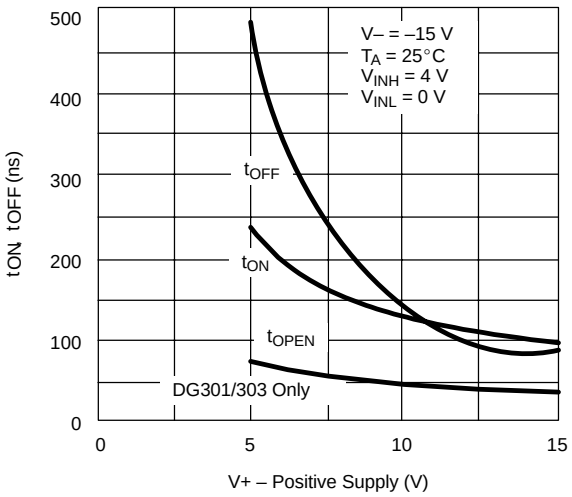
$r_{DS(on)}$ vs. V_D and Temperature



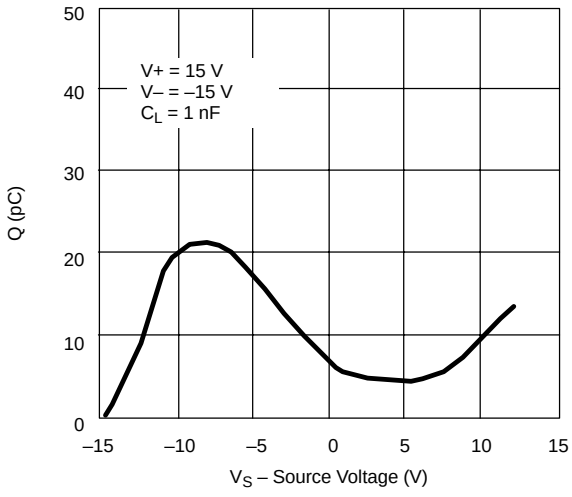
$r_{DS(on)}$ vs. V_D and Power Supply Voltage



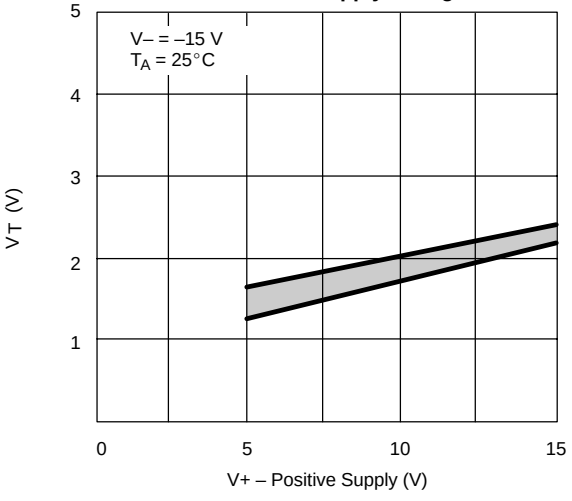
Switching Time and Break-Before-Make Time vs. Positive Supply Voltage



Charge Injection vs. Analog Voltage



Input Switching Threshold vs. Positive Supply Voltage



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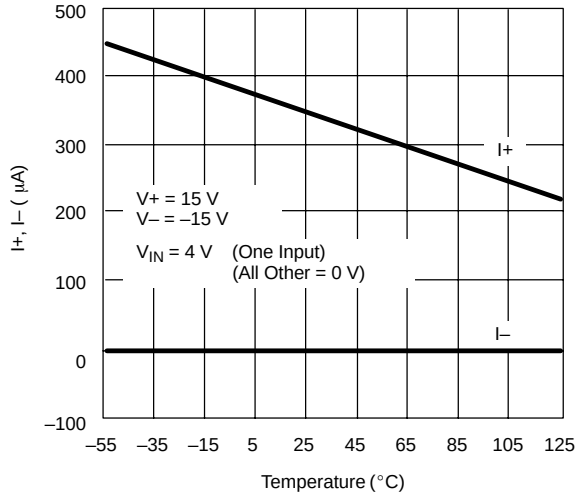
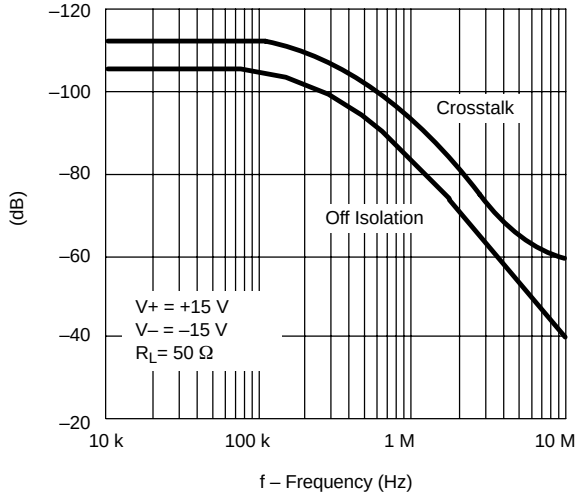
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

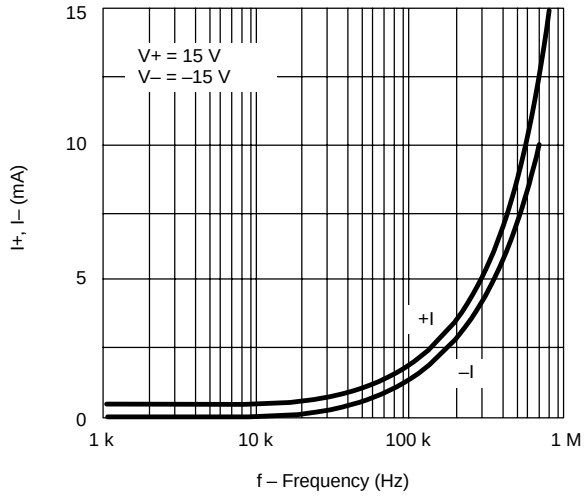
Supply Current vs. Temperature



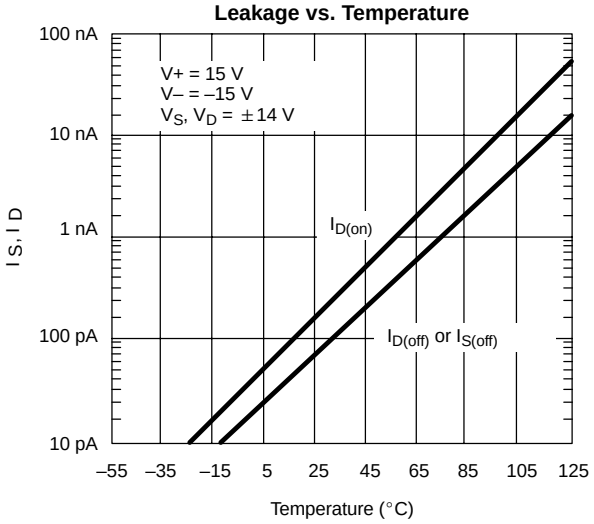
Off Isolation and Crosstalk vs. Frequency



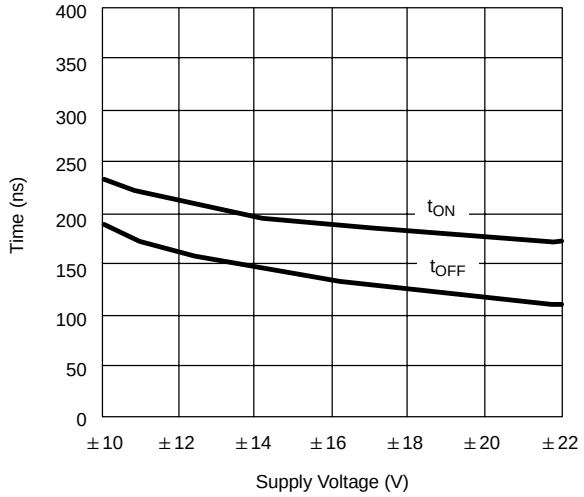
Supply Curents vs. Switching Frequency



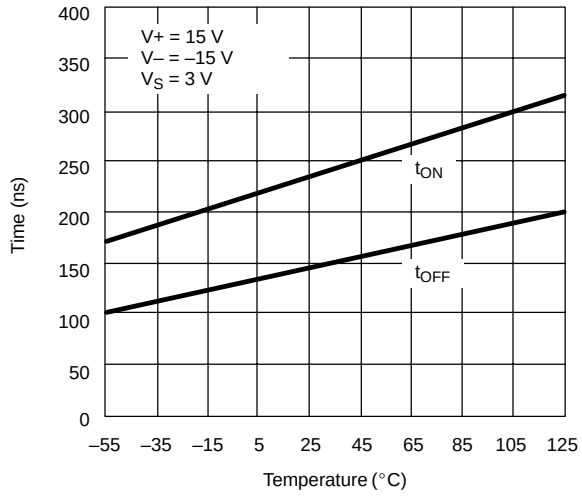
Leakage vs. Temperature



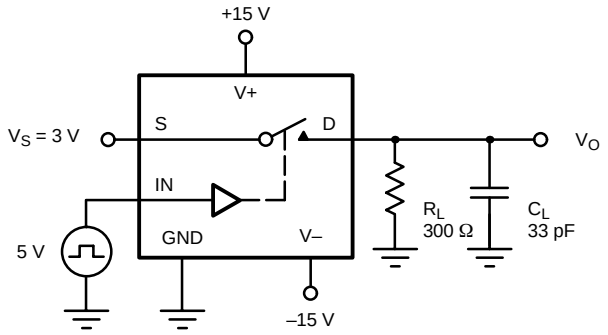
Switching Time vs. Power Supply Voltage



Switching Time vs. Temperature



TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

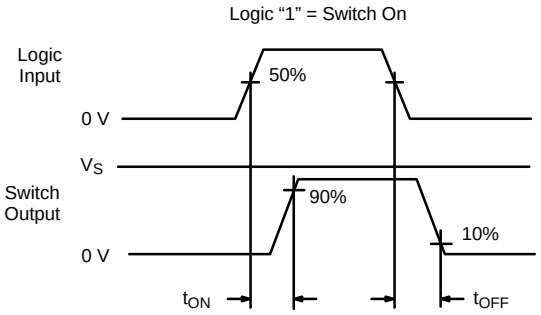
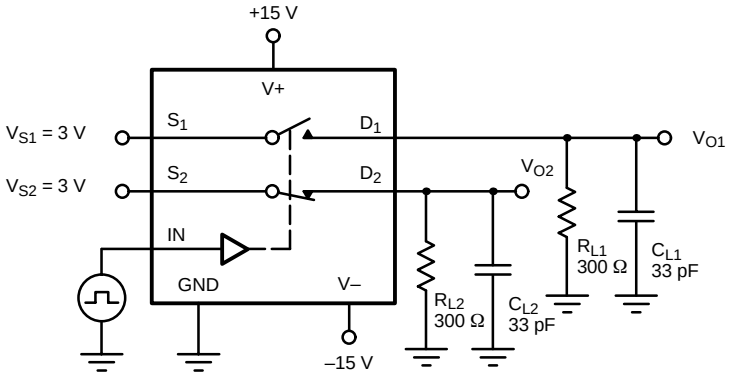


FIGURE 2. Switching Time



C_L (includes fixture and stray capacitance)

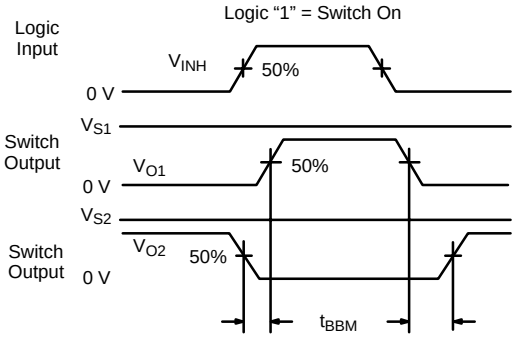
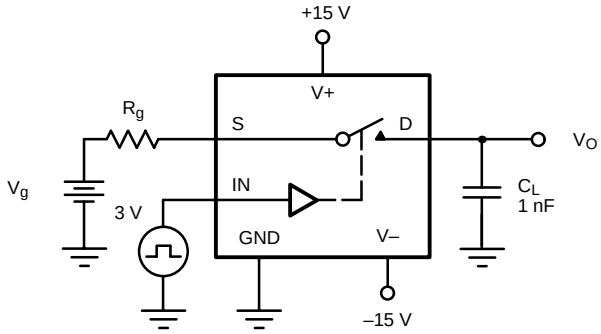


FIGURE 3. Break-Before-Make SPDT



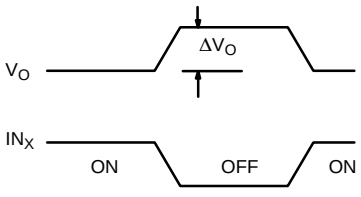


FIGURE 4. Charge Injection

APPLICATION HINTS[NO TAG]

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	GND Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	–15	0	4/0.8	–15 to 15
20	–20	0	4/0.8	–20 to 20
15	0	0	4/0.8	0 to 15

Note:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.