Back END IC

SAA7158

FEATURES

- Line Flicker Reduction (LFR) by means of MEDIAN filtering
- Vertical zoom
- Digital colour transient improvement
- Digital luminance peaking
- Movie phase detection
- 4:4:4 YUV data throughput selectable, standard is 4:1:1 Y/U/V
- D/A conversion
- UART interface.

GENERAL DESCRIPTION

Application Environment

The Back END IC (abbreviated as BENDIC) is designed to cooperate with an 8051 type of microprocessor, the ECO3 (SAA4951) memory controller and Texas Instruments TMS4C2970 memories, but other configurations may be applicable. Fig.1 shows the block diagram of the feature box. The nominal clock frequency of the IC is 27 MHz or 32 MHz, with a maximum of 36 MHz.

The system supports the digital Y/U/V bus for selection of different video signal sources. The Y/U/V bus and the BENDIC data input are fully synchronous with respect to the clock signal. A line reference signal BLN for timing control purposes has to be provided by external elements which always controls the system timing, independent of active signal sources or desired functions.

Analog Characteristics

The BENDIC contains 3 independent, high speed digital to analog converters for luminance and colour difference signal processing and conversion. The resolution of the two DA converters for the colour difference signals is 8 bit. The luminance peaking up to 6 dB at high frequencies widens the resolution of the luminance channel. To avoid aliasing effects due to time discrete amplitude limiting the resolution of 9-bit is offered for the luminance conversion. All output stages provide high performance output stages for driving lines with low impedance line termination.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	4.5	5.5	V
	analog supply voltage	4.75	5.25	V
T_{amb}	operating ambient temperature	0	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7158WP	68	PLCC	plastic	SOT188

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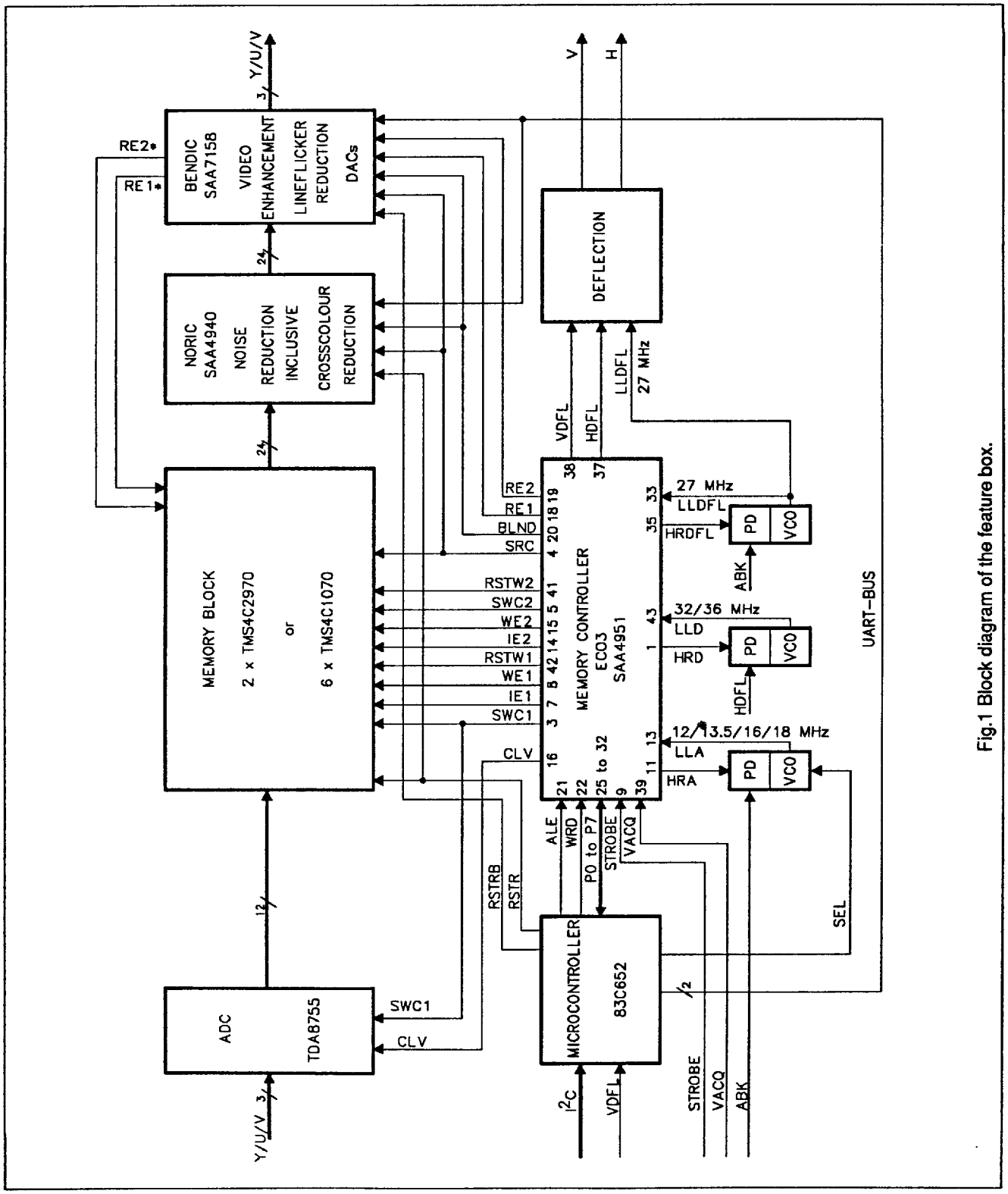

Fig.1 Block diagram of the feature box.

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PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
TEST1/AP	1	input	action pin for testing; to be connected to V_{SS}
Y0-0	2	3-state output	feedback_data to second memory, Y bit 0
Y0-1	3	3-state output	feedback_data to second memory, Y bit 1
Y0-2	4	3-state output	feedback_data to second memory, Y bit 2
Y0-3	5	3-state output	feedback_data to second memory, Y bit 3
Y0-4	6	3-state output	feedback_data to second memory, Y bit 4
Y0-5	7	3-state output	feedback_data to second memory, Y bit 5
V_{DD1}	8	supply	positive digital supply voltage (+5 V)
V_{SS1}	9	ground	digital ground
Y0-6	10	3-state output	feedback_data to second memory, Y bit 6
Y0-7	11	3-state output	feedback_data to second memory, Y bit 7
UV0-0	12	3-state output	feedback_data to second memory, UV bit 0
UV0-1	13	3-state output	feedback_data to second memory, UV bit 1
UV0-2	14	3-state output	feedback_data to second memory, UV bit 2
UV0-3	15	3-state output	feedback_data to second memory, UV bit 3
TEST2/SP	16	input	shift pin for testing; to be connected to Vss
RE2_OUT	17	output	redirected read enable to memory 2
RE1_OUT	18	output	redirected read enable to memory 1
RSTR	19	input	memory read, µP interface and movie detection reset
RE2_IN	20	input	input for read enable to memory 2
RE1_IN	21	input	input for read enable to memory 1
BLN	22	input	blanking signal
µPCL	23	input	clock for interface with 8051 UART, mode 0
µPDA	24	in/output	data for interface with 8051 UART, mode 0
V_{SS2}	25	ground	digital ground
CLK	26	input	master clock, nominal 27 (32) MHz
V_{DD2}	27	supply	positive digital supply voltage (+5 V)
V1-0/Y2-0	28	input	V data, bit 0 in 4:4:4; Y data second memory, bit 0
V1-1/Y2-1	29	input	V data, bit 1 in 4:4:4; Y data second memory, bit 1
V1-2/Y2-2	30	input	V data, bit 2 in 4:4:4; Y data second memory, bit 2
V1-3/Y2-3	31	input	V data, bit 3 in 4:4:4; Y data second memory, bit 3
V1-4/Y2-4	32	input	V data, bit 4 in 4:4:4; Y data second memory, bit 4
V1-5/Y2-5	33	input	V data, bit 5 in 4:4:4; Y data second memory, bit 5
V1-6/Y2-6	34	input	V data, bit 6 in 4:4:4; Y data second memory, bit 6
V1-7/Y2-7	35	input	V data, bit 7 in 4:4:4; Y data second memory, bit 7
U1-0/UV2-0	36	input	U data, bit 0 in 4:4:4; UV data second memory, bit 0
U1-1/UV2-1	37	input	U data, bit 1 in 4:4:4; UV data second memory, bit 1
U1-2/UV2-2	38	input	U data, bit 2 in 4:4:4; UV data second memory, bit 2
U1-3/UV2-3	39	input	U data, bit 3 in 4:4:4; UV data second memory, bit 3
V_{SS3}	40	ground	digital ground
U1-4/UV1-0	41	input	U data, bit 4 in 4:4:4; UV data first memory, bit 0
U1-5/UV1-1	42	input	U data, bit 5 in 4:4:4; UV data first memory, bit 1
U1-6/UV1-2	43	input	U data, bit 6 in 4:4:4; UV data first memory, bit 2
U1-7/UV1-3	44	input	U data, bit 7 in 4:4:4; UV data first memory, bit 3
Y1-0	45	input	Y data first memory, bit 0
Y1-1	46	input	Y data first memory, bit 1
Y1-2	47	input	Y data first memory, bit 2

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SYMBOL	PIN	TYPE	DESCRIPTION
Y1-3	48	input	Y data first memory, bit 3
Y1-4	49	input	Y data first memory, bit 4
Y1-5	50	input	Y data first memory, bit 5
Y1-6	51	input	Y data first memory, bit 6
Y1-7	52	input	Y data first memory, bit 7
V_{SUB}	53	analog ground	substrate pin; connect to analog ground (V_{SSA})
RFHY	54	analog input	connect C = 100 nF to analog ground (V_{SSA})
RFLY	55	analog input	connect to analog ground (V_{SSA})
RFLC	56	analog input	connect to analog ground (V_{SSA})
RFHC	57	analog input	connect C = 100 nF to analog ground (V_{SSA})
V_{DDA4}	58	analog supply	analog supply voltage for reference ladders of the three DA converters and for current sources of the output buffers
CUR	59	analog input	current input for analog output buffers (0.4 mA from V_{DDA4} = 5 V); connect with R = 15 kΩ
V_{DDA3}	60	analog supply	analog supply voltage for output buffer AY
AY	61	analog output	analog luminance Y output
V_{SSA3}	62	analog ground	analog ground for output buffer AY
V_{DDA2}	63	analog supply	analog supply voltage for output buffer AU
AU	64	analog output	analog (B–Y) or –(B–Y) output
V_{SSA2}	65	analog ground	analog ground for output buffer AU
V_{SSA1}	66	analog ground	analog ground for output buffer AV
AV	67	analog output	analog (R–Y) or –(R–Y) output
V_{DDA1}	68	supply	analog supply voltage for output buffer AV

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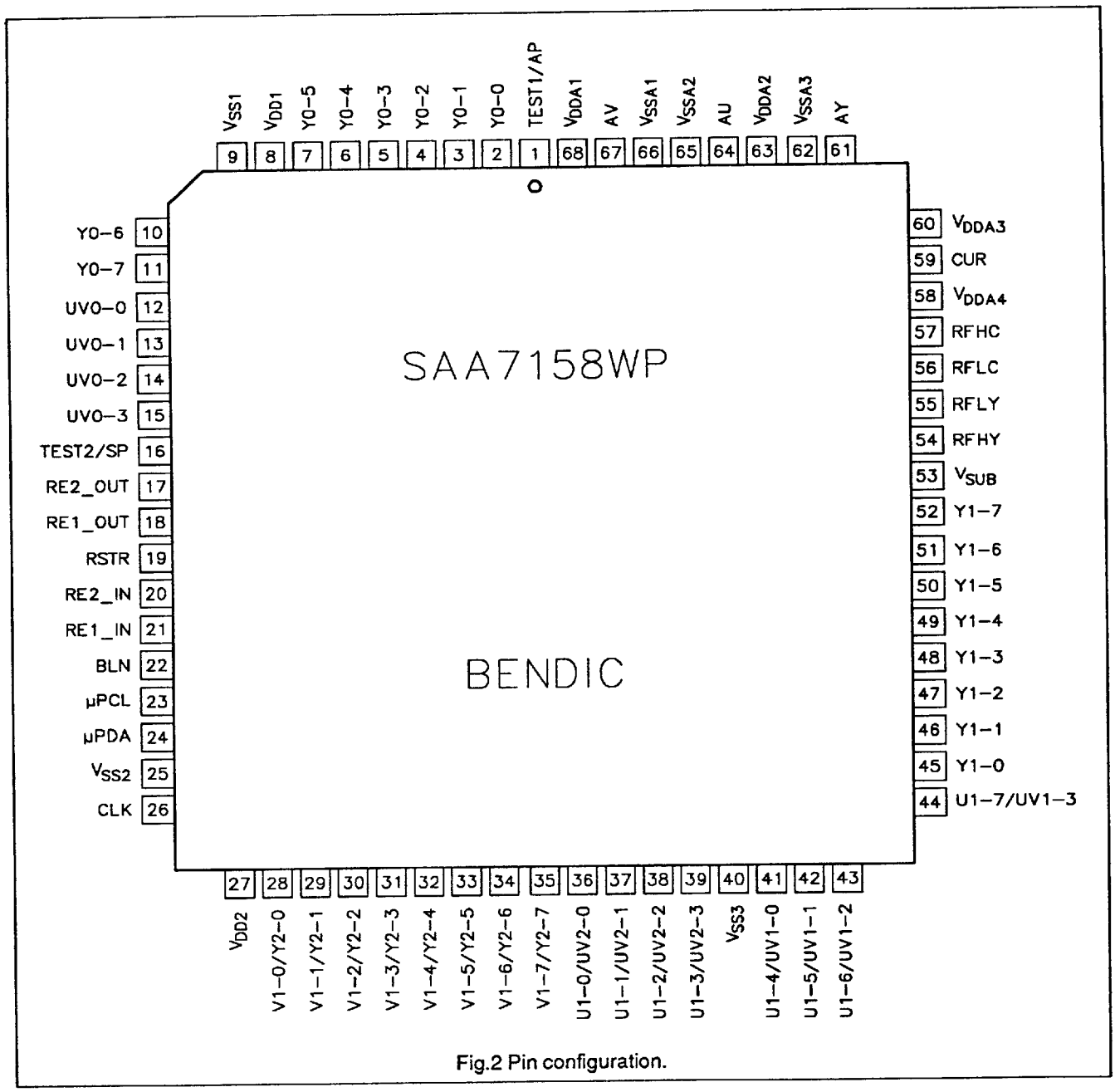

Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

Block Diagram

The BENDIC will be produced in a CMOS double metal process. It is possible to feed the BENDIC with 8-bit wide luminance and chrominance signals Y/U/V in 4:1:1 mode from the digital Y/U/V bus and to run it in a bypass mode with Y/U/V in 4:4:4 mode without any bandwidth reduction.

The BENDIC contains the processing functions as depicted in Fig.3.

Following functions are available:

Datapath:

- 1H - 4:1:1 line memory, 852 words by 8-bits luminance + 4-bits multiplexed chrominance
- REFORMATTER to get 8-bit wide UV from the Y/U/V bus format
- MIX UV and MIX Y to interpolate between actual and 1H-delayed input signals, programmable for realization of vertical zoom
- MEDIAN filter in luminance processing path for line flicker reduction
- MOVIE PHASE DETECT for supporting line flicker reduction control
- PEAKING for luminance channel
- UPSAMPLING and DCTI for chrominance transient improvement
- HOLD/GREY/BLANK blocks for blanking and grey level insertion
- RE PROCESSING controls read enable for first and second memory, outputs are programmable for different applications
- Data switches for field select, mix/median select, 4:1:1/4:4:4 select
- DAC blocks for digital to analog conversion of Y, U, V video signals
- REGISTER with 3-state control for direct output of Y/U/V 1 input to memories.

Control:

- µP INTERFACE for the control of BENDIC functions, including zoom control
- TIMING CONTROL and TEST as support blocks.

All video data signal processing inside the BENDIC is phaselinear and nonrecursive (except line delay in recirculation mode).

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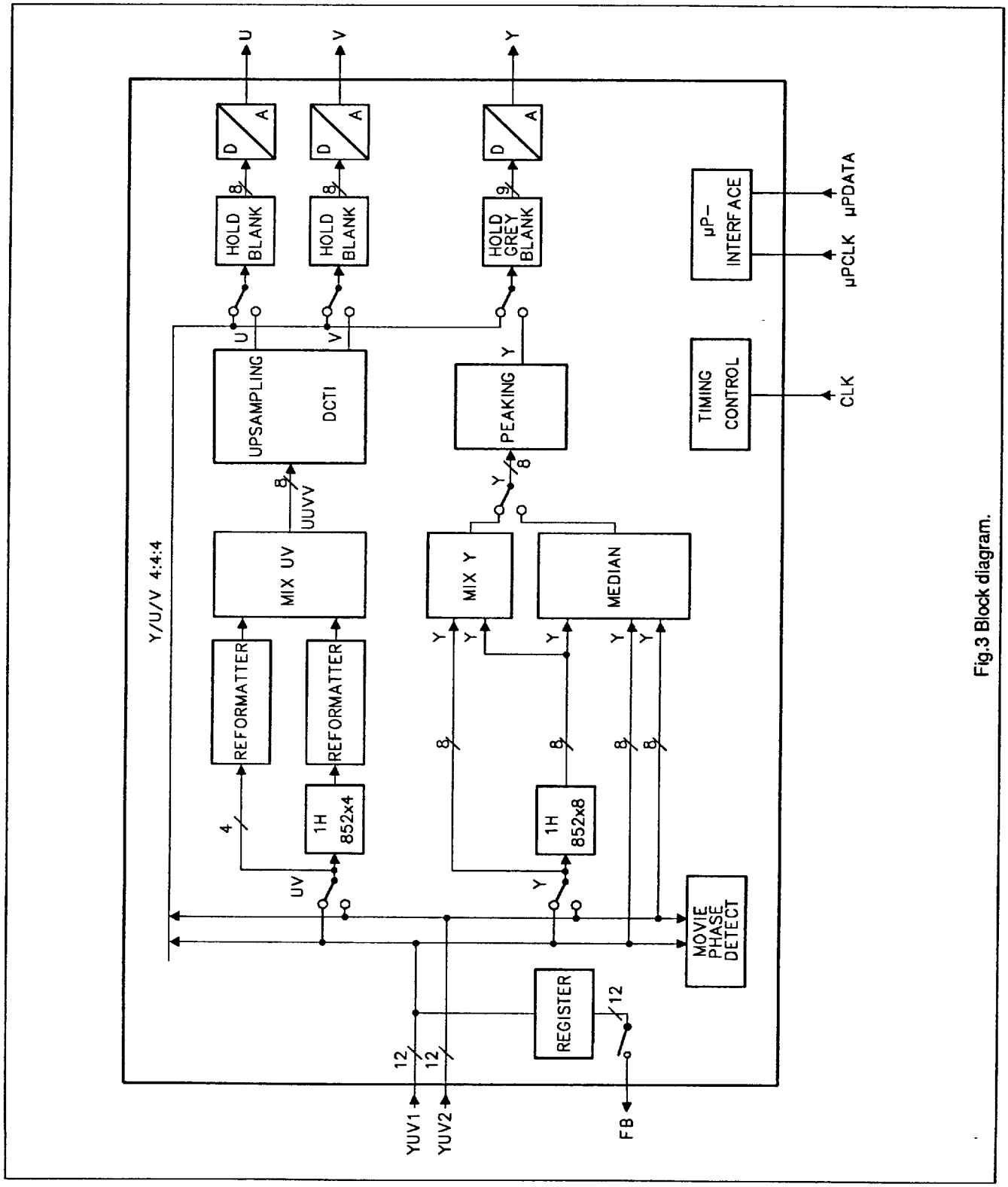

Fig.3 Block diagram.

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Data Path Signal processing

• 1H - 4:1:1 line memory, 852 words by 8-bits luminance + 4-bits multiplexed chrominance

The Y/U/V line memory is organized as 852 x 12 bits. It works as a shift register with recirculation mode if desired. The line start is synchronized to RE, and if there are more than 852 words to be stored it will stop and hold.

• REFORMATTER to get 8-bit wide UV from the Y/U/V bus format

The reformatter changes the 4:1:1 format of UV signals into a sequential 8-bit U and V data stream with a sampling rate of half the master clock.

• MIX UV and MIX Y to interpolate between actual and 1H-delayed input signals, programmable for realization of vertical zoom

The function of the MIX-blocks is to interpolate between two input sources A and B (original signal and 1H-delayed signal). Possible interpolation coefficients are $\{1 \text{ or } \frac{3}{4} \text{ or } \frac{1}{2} \text{ or } \frac{1}{4} \text{ or } 0\} \times (A - B) + B$.

• MEDIAN filter in luminance processing path for line flicker reduction

The median filter consists of two different median filters working in parallel with full clock rate. Filters for up and downsampling are implemented with an 8-bit output.

• MOVIE PHASE DETECT for supporting line flicker reduction control

A pixel by pixel luminance level comparison is made on the active video of two consecutive fields from the memory. The absolute difference of the 4 most significant bits of each pixel from the two fields is added to the accumulated value of the current field in a register. The highest significant two bytes thereof are transferred during field blanking period with rising edge of RSTR signal into a register that can be read via the µP interface. After reading the register will be cleared.

• PEAKING for luminance channel

The H-peaking of the luminance channel compensates the bandwidth reduction caused by various components of the TV signal processing chain. Because of the possibility to convert over and undershoots it is even possible to precompensate the si-amplitude attenuation of the D/A converter by 6 dB. The absolutely phaselinear filters can be programmed: frequency response, amplitude of the high frequency signals and degree of coring is controlled via the µP interface. Frequency responses c. f. separate application sheet.

• UPSAMPLING and DCTI for chrominance transient improvement

After upsampling of U and V, in the DCTI block the U and V signals are processed with a look-backwards/look-forwards device. The chrominance signal values are stored in a 26 tap pixel delay line. Controlled by a multiplexer select signal K the values are read from the pixel delay line into the output registers of DCTI. The calculation of the K signal is done within this block. To determine the number of steps to look back and forwards the following relation is used:

$$\frac{d}{dt}\left\{\left|\frac{dU}{dt}\right| + \left|\frac{dV}{dt}\right|\right\}.$$

U and V are processed serially with the same circuitry. The final upsampling towards the master clock for D/A conversion is part of the algorithm and done by linear interpolation between two adjacent taps of choice. It is controlled by the K signal too.

• HOLD/GREY/BLANK blocks for blanking and grey level insertion

The function of these blocks is to insert desired levels for Y, U and V, where no active video is present. BLANKing is performed during line and field blanking period indicated by BLN. GREY is performed where RE indicates that the memory is not read out, and pixel repetition is switched off by the µP interface; the grey value comes via the µP interface. HOLD is performed if pixel repetition is selected by the µP interface; the last value of Y, U and V is kept until RE is active again.

• RE PROCESSING controls read enable for first and second memory

Here the output signals RE1 and RE2 are shifted by adding a programmable delay of 5, 6, 7 or 8 clock pulses with respect to the input signals. In addition RE1 will be influenced in case of zoom.

• data switches for field select, mix/median select, 4:1:1/4:4:4 select

The switches shown in the block diagram Fig.3 are controlled via the µP interface and allow control of the data streams inside the BENDIC.

• DAC blocks for digital to analog conversion of Y, U, V video signals

The D/A conversion is performed in the DAC blocks. The converters consist of the resistor strings to be connected externally and three buffers with a 25 Ω serial resistor at the output built in. To get 75 Ω impedance externally three 50 Ω resistors have to be used near the pins. The capacitive load at the outputs should not exceed 30 pF.

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• REGISTER with 3-state control for direct output of Y/U/V 1 input to memories

The 3-state switch with internal register is supplied for the feedback data to the second memory. The feedback bus is a copy of the field1 bus, but with 4 clockpulses delay. 3-state control is done via µP interface.

The control signals

CLK
Line locked clock of maximal 36 MHz.
This is the system clock. Within the BENDIC the CLK signal is distributed to the different blocks.

BLN
Blanking NOT signal.
This signal marks the horizontal and vertical blanking and defines with its rising edge the start phase of the UV 4:1:1 format. A programmable delay of 0, 1, 2 or 3 clock pulses shifts the internal pulse with respect to the input.

RE1_in
Read enable memory 1 signal.
This signal is generated by the memory controller and its HIGH state determines the read enable on the first memory bank, after it is processed by BENDIC for the ZOOM mode and fine shift of the edges.

RE2_in
Read enable memory 2 signal.
This signal is generated by the memory controller and its HIGH state determines the read enable on the second memory bank, including a fine shift of the edges.
note:
RE1_in and RE2_in are processed in the BENDIC to:
– external signals: RE1_out and RE2_out
– RE with correct internal delay to match datapath delays, is used to define the edges between video and side panels (grey insertion or pixel repetition).

RSTR
Reset signal
This signal is transferred (asynchronous with CLK) by e. g. a microprocessor to reset the communication between the microprocessor and the BENDIC. CLK has to be present in this case. In a typical application, RSTR is an active HIGH pulse, issued only in the vertical blanking period. During RSTR HIGH-state, the 'feedback_data' lines are switched to 3-state, temporarily overruling the mode that has been set by the microprocessor. By this provision, RSTR can be used to prevent data collision on the 3-state databus, e. g. during a power on sequence. Also, this signal is used to transfer the 'movie phase detect' data to a register that can be read by the microprocessor.

µPCL
Microprocessor interface clock signal
This signal is transferred (asynchronous with CLK) by a microprocessor (8051, UART mode 0) as communication clock signal at 1 MHz.

µPDA
Microprocessor interface data signal
This signal is transferred or received (asynchronous with CLK) by a microprocessor (8051, UART mode 0) as communication data signal at 1 MBaud, related to µPCL. Data is valid at the rising edge of µPCL.

The external control

The µP interface has the following functions:
– Receive settings from the µP
– Transmit movie phase detect data to the µP
The interface is based on a two wire interface, one for clock, the other for bidirectional data form. It is compatible with the 8051 family UART mode 0 interface. The µP is the master of the communication, it generates the clock (nominal 12 MHz/12 = 1 MHz), only active when transfer is done.
The protocol for the communication is:
8 addressbits are sent by the µP (LSB first), if the address is a write address then 8 databits (LSB first) are sent by the µP, else (if the address is a read address) 8 databits are sent by BENDIC.
RSTR is used to reset the phase of the address/data transfer. The negative going edge of RSTR clears the address register. After reset the first transmitted bit is to be taken as the first (LSB) bit of an address.
For field1/field2 selection and for mix/median selection, 4 addresses are used to select each of the four combinations. A databyte is not obligatory after each of these four addresses, but a dummy databyte is needed if the transmission is to be followed by a further one.

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Table 1 Write address table.

ADDRESS (HEX)	FUNCTION	BIT
1	dataformat setting	bit2: invUV
		bit3: UV8bit
		bit4: UVbin
		bit5: Yclip
		bit6: 4:4:4
		bit7: feedback
2	grey value setting	bit4: grey(0)
		bit5: grey(1)
		bit6: grey(2)
		bit7: grey(3)
3	read enable setting	bit0: re1_d(0)
		bit1: re1_d(1)
		bit2: inv_re1
		bit3: re2_d(0)
		bit4: re2_d(1)
		bit5: inv_re2
		bit6: bln_d(0)
		bit 7: bln_d(1)
4	zoom setting	bit0: lps
		bit1: pixrep
		bit2: black16
		bit3: zoom(0)
		bit4: zoom(1)
		bit5: zoom(2)
		bit6: zoom(3)
		bit7: zoom(4)
5	CTI setting	bit4: range(0)
		bit5: range(1)
		bit6: gain(0)
		bit7: gain(1)
6	peaking setting, average UV select	bit0: av_w_med
		bit1: WG(0)
		bit2: WG(1)
		bit3: BFB
		bit4: BP(0)
		bit5: BP(1)
		bit6: coring(0)
		bit7: coring(1)
7C	multiplexer setting	SET select field1 OFF; select median OFF (all databits are dummy)
7D	multiplexer setting	SET select field1 ON; select median OFF (all databits are dummy)
7E	multiplexer setting	SET select field1 OFF; select median ON (all databits are dummy)
7F	multiplexer setting	SET select field1 ON; select median ON (all databits are dummy)

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The function of the bits in the control datawords are explained below:

feedback	HI: feedback output is 3-state enabled = outputs active
4:4:4	HI: YUV-4:4:4 mode selected instead of 4:1:1 mode
Yclip	HI: Y signal after peaking is clipped and converted to 9-bit range
UVbin	HI: UV signals are taken from input as binary signals instead 2's complement
UV8bit	HI: UV signals are taken from input as 8-bit values instead of 7-bit
invUV	HI: UV signals are inverted before the DACs (outputs = –U and –V)
grey(3:0)	determines highest 4 bits in shade of grey in side panels
bln_d(1:0)	shifts the internal BLN signal from 0 to 3 clock pulses with respect to input
re2_d(1:0)	shifts 5 to 8 clock pulses the RE2 output signal versus input
re1_d(1:0)	shifts 5 to 8 clock pulses the RE1 output signal versus input, additionally influenced by zoom
inv_re2	HI: RE2 output is polarity reversed in relation to RE2 input
inv_re1	HI: RE1 output is polarity reversed in relation to RE1 input
zoom(4:0)	determines vertical zoom factor, which is (32/zoom(4:0)); zoom(4:0) = 0 is equivalent to no zoom
black16	HI: the Y signal value during the blanking period is 16 instead of 0
pixrep	HI: side panels have the same Y, U and V as on the edge of the last video information
lps	HI: functional test mode for line on line median on/off
range(1:0)	determines maximum in CTI range of looking back/looking forward
gain(1:0)	determines gain of CTI function
coring(1:0)	determines coring level in Y peaking
av_w_med	enable average UV while median in Y (UV := 1/2 x direct + 1/2 x delayed)
BP(1:0)	determines frequency response in Y peaking
WG(1:0)	determines weighted addition in Y peaking with 1 or 1/2 or 1/4 or 0
BFB	HI: determines bypass for BF1 in Y peaking

The BENDIC provides the correlation of two subsequent fields with its 'Movie phase detector' via the µP interface. The MSB or LSB values of this correlation factor is read from the BENDIC by sending an addressbyte and subsequently receiving a databyte from it, according to Table 2.

Table 2 Read address table.

ADDRESS (HEX)	BIT
80	bit0: corr(0)
	bit1: corr(1)
	bit2: corr(2)
	bit3: corr(3)
	bit4: corr(4)
	bit5: corr(5)
	bit6: corr(6)
	bit7: corr(7)

ADDRESS (HEX)	BIT
81	bit0: corr(8)
	bit1: corr(9)
	bit2: corr(10)
	bit3: corr(11)
	bit4: corr(12)
	bit5: corr(13)
	bit6: corr(14)
	bit7: corr(15)

corr(15:0) is the measured Y correlation factor between two successive fields.

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CHARACTERISTICS

Specification of input/output and clock levels and timing

The following table shows the specifications of input/output/clock levels and timing for T_{amb} = 0 to +70 °C; V_{DD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD1-2}	digital supply voltages		4.5	–	5.5	V
V_{DDA1-4}	analog supply voltages		4.75	–	5.25	V
I_{DD1-2}	supply current digital		–	–	250	mA
I_{DDA1-4}	supply current analog	note 1	–	–	18	mA
Digital inputs						
V_{IL}	LOW level input voltage		–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current		–	–	10	µA
C_{IC}	input capacitance (clocks)		–	–	10	pF
C_{ID}	input capacitance (data)		–	–	10	pF
C_{IZ}	input capacitance (I/O in high Z)		–	–	10	pF
Reference and current inputs						
I_{CUR}	input current		–	–	0.4	mA
Digital outputs						
V_{OH}	HIGH level output voltage	note 2	2.4	–	V_{DD1-2}	V
V_{OL}	LOW level output voltage	note 2	0	–	0.6	V
Timing						
t_{CLK}	CLK cycle time		27	–	41	ns
k_{CLK}	CLK duty cycle $t_{CLK-HIGH}/t_{CLK}$		40	–	60	%
t_r	CLK rise time		–	–	5	ns
t_f	CLK fall time		–	–	6	ns
t_{SU}	input data setup time		–	–	5	ns
t_{HD}	input data hold time		–	–	6	ns
t_{OH}	output data hold time	note 2	6	–	–	ns
t_{OD}	output data delay time	note 2	–	–	25	ns
Data output loads (3-state outputs)						
C_{ld}	output load capacitance		10	–	35	pF
Characteristics of the DA converters						
RSL_Y	resolution of the Y DAC		–	9	–	bit
RSL_C	resolution of the U and V DAC		–	8	–	bit
B	analog signal bandwidth (–3 dB)		20	–	–	MHz
CT	crosstalk between channels		–	–	–42	dB
DNL	differential nonlinearity	referred to 8 MSB's	–	–	±0.5	LSB
INL	integral nonlinearity	referred to 8 MSB's	–	–	±1	LSB
V_{out}	output voltage (without load)		–	2 V_{p-p}	–	V

Notes to the characteristics

1. f_{CLK} = 36 MHz, f_{data} = 18 MHz (rectangular full scale); without output load.
2. Timings and levels have to be measured with load circuits 1.2 kΩ connected to 3.0 V (TTL load), and C_L = 25 pF.

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APPLICATION NOTE FOR THE ANALOG PART OF BENDIC

The digital to analog conversion is done in parallel for the three channels. The DA converters (8-bit for U and V; 9-bit for Y) are based on resistor strings with low impedance output buffers. They are designed for 2 V_{p-p} unloaded output swing. To avoid integral nonlinearity errors, the minimum output voltage is 200 mV; so the DC range for unloaded output is between 0.2 and 2.2 V.

A serial resistor of 25 Ω is integrated at the outputs of the buffers. With 50 Ω in series - close to the ouput pins - the nominal output voltage for 75 Ω line termination is 1 V_{p-p} with a DC range of 0.1 to 1.1 V. Amplitude matching to external requirements has to be done with external dividers. Capacitance load should not exceed 30 pF.

The DAC's require three separate analog supply voltages V_{DDA1-3} and analog ground lines V_{SSA1-3} for the output buffers.

The accuracy of an external voltage reference input V_{DDA4} directly influences the output amplitude of the video signals.

The current input CUR supplies the output buffers with a current of about 0.3 mA at V_{DDA} = 5 V, if a resistor of 15 kΩ is connected to this pin.

A larger current improves the output bandwidth but makes the integral nonlinearity worse.

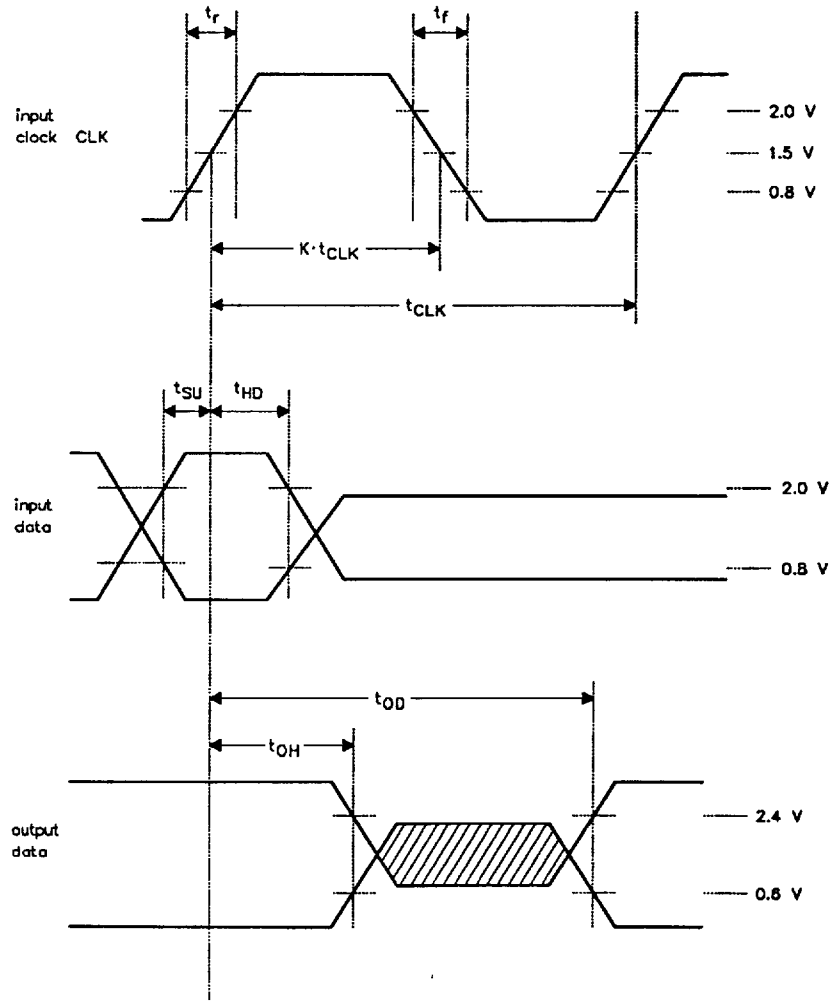

Fig.4 Timing diagram.

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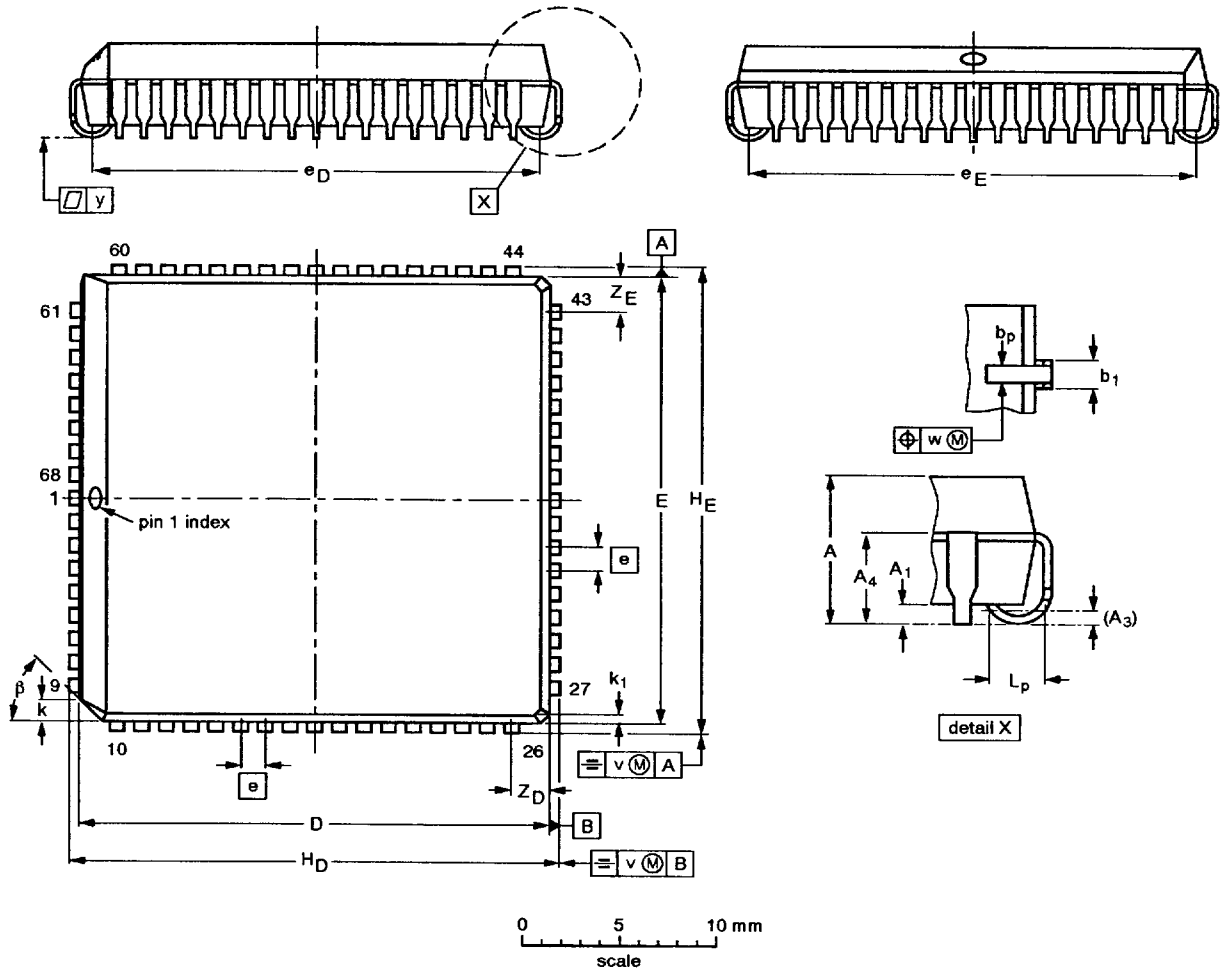
Package outlines

PLCC68: plastic leaded chip carrier; 68 leads

SOT188-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

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