VFC110

SBVS021A − OCTOBER 1988 − REVISED APRIL 2007

High-Frequency VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- **HIGH-FREQUENCY OPERATION: 4MHz FS max**
- **EXCELLENT LINEARITY: ±0.02% typ at 2MHz**
- **PRECISION 5V REFERENCE**
- **DISABLE PIN**
- **LOW JITTER**

APPLICATIONS

- **INTEGRATING A/D CONVERSION**
- **PROCESS CONTROL**
- **VOLTAGE ISOLATION**
- **VOLTAGE-CONTROLLED OSCILLATOR**
- **FM TELEMETRY**

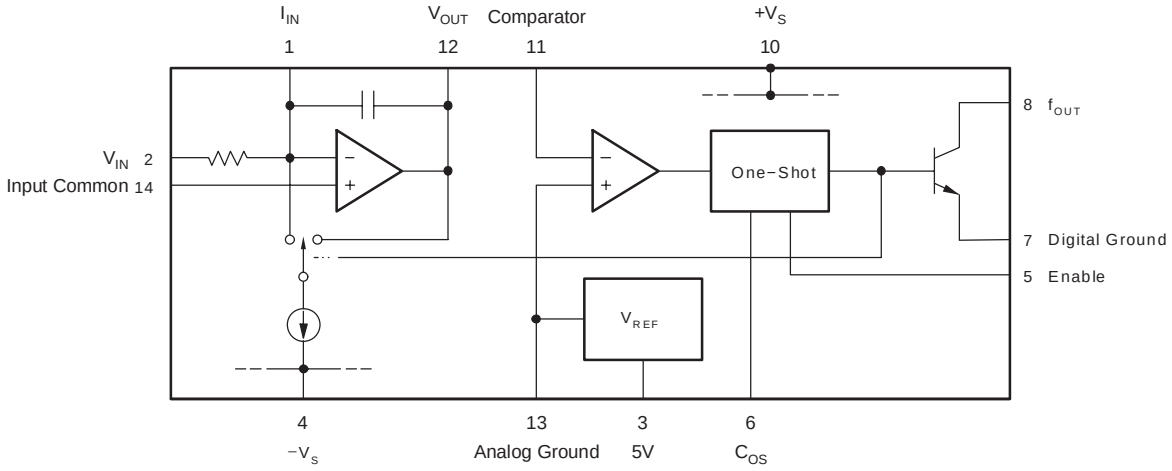
DESCRIPTION

The VFC110 voltage-to-frequency converter is a third-generation VFC offering improved features and performance. These include higher frequency operation, an onboard precision 5V reference, and a Disable function.

The precision 5V reference can be used for offsetting the VFC transfer function, as well as exciting transducers or bridges. The Enable pin allows several VFCs' outputs to be paralleled, multiplexed, or simply to shut off the VFC. The open-collector frequency output is TTL-/CMOS-compatible. The output may be isolated by using an opto-coupler or transformer.

Internal input resistor, one-shot and integrator capacitors simplify applications circuits. These components are trimmed for a full-scale output frequency of 4MHz at 10V input. No additional components are required for many applications.

The VFC110 is packaged in a plastic 14-pin DIP. Industrial and military temperature range gradeouts are available.



ABSOLUTE MAXIMUM RATINGS(1)

Power Supply Voltages ($+V_S$ to $-V_S$)	40V
f_{OUT} Sink Current	50mA
Comparator In Voltage	$-5V$ to $+V_S$
Enable Input	$+V_S$ to $-V_S$
Integrator Common-Mode Voltage	−1.5V to +1.5V
Integrator Differential Input Voltage	+0.5V to −0.5V
Integrator Out (short-circuit)	Indefinite
V_{REF} Out (short-circuit)	Indefinite
Operating Temperature Range	
P Package	−40°C to +85°C
Storage Temperature	
P Package	−40°C to +125°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

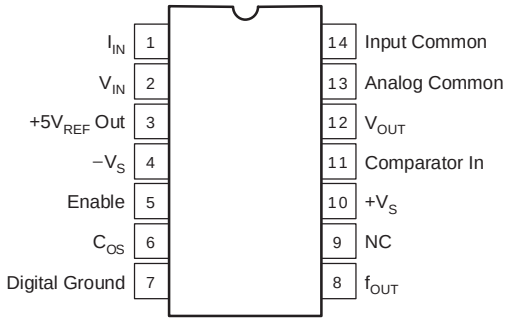
ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE
VFC110AP	14-Pin Plastic DIP	N	−25°C to +85°C

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATION

Top View P-DIP



ELECTRICAL CHARACTERISTICS

At T_A = +25°C and V_S = ±15V, unless otherwise noted.

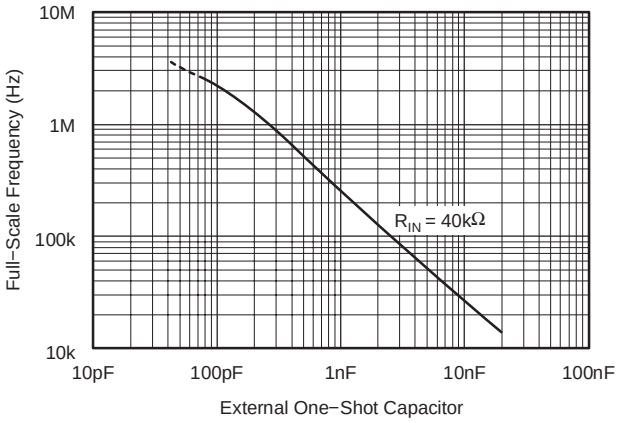
PARAMETER	CONDITIONS	VFC110AP MIN	VFC110AP TYP	VFC110AP MAX	UNITS
VOLTAGE-TO-FREQUENCY OPERATION					
Nonlinearity(1): f_{FS} = 100kHz	C_{OS} = 2.2nF, R_{IN} = 44kΩ		0.01	0.05	%FS
f_{FS} = 1MHz	C_{OS} = 150pF, R_{IN} = 40kΩ			0.1	%FS
f_{FS} = 2MHz	C_{OS} = 56pF, R_{IN} = 34kΩ		0.02		%FS
f_{FS} = 4MHz	C_{OS} = (Int), R_{IN} = (Int)		1		%FS
Gain Error, f = 1MHz	C_{OS} = 150pF, R_{IN} = 40kΩ			5	%
Gain Drift, f = 1MHz	Specified Temp Range			100	ppm/°C
Relative to V_{REF}	Specified Temp Range		100		ppm/°C
PSRR	V_S = ±8V to ±18V			0.1	%/V
INPUT					
Full-Scale Input Current			250	500	µA
I_{B-} (Inverting Input)			20	100	nA
I_{B+} (Noninverting Input)			250		nA
V_{OS}				3	mV
V_{OS} Drift	Specified Temp Range		35		µV/°C
INTEGRATOR AMPLIFIER OUTPUT					
Output Voltage Range	R_L = 2kΩ	−0.2		$+V_S$ − 4	V
Output Current Drive		5	20		mA
Capacitive Load	No Oscillations		10		nF
COMPARATOR INPUT					
I_B (Input Bias Current)			−5		µA
Trigger Voltage			±50		mV
Input Voltage Range		−5		$+V_S$	V
OPEN COLLECTOR OUTPUT					
V_O Low				0.4	V
$I_{LEAKAGE}$			0.1	1	µA
Fall Time			25		ns
Delay to Rise			25		ns
Settling Time	To Specified Linearity for a Full-Scale Input Step	One Pulse of New Frequency Plus 1µs			
REFERENCE VOLTAGE					
Voltage		4.97	5	5.03	V
Voltage Drift				50	ppm/°C
Load Regulation	I_O = 0 to 10mA		2	10	mV
PSRR	V_S = ±8V to ±18V		5		mV/V
Current Limit	Short Circuit	15	20		mA
ENABLE INPUT					
V_{HIGH} (f_{OUT} Enabled)	Specified Temp Range	2			V
V_{LOW} (f_{OUT} Disabled)	Specified Temp Range			0.4	V
I_{HIGH}			0.1		µA
I_{LOW}			1		µA
POWER SUPPLY					
Voltage, ±V_S		±8	±15	±18	V
Current			13	16	mA
TEMPERATURE RANGE					
Specified					
AP		−25		+85	°C
Storage					
AP		−40		+125	°C

(1) Nonlinearity measured from 1V to 10V input.

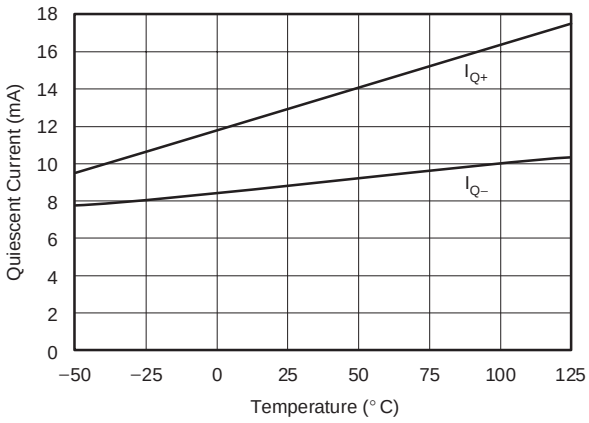
TYPICAL CHARACTERISTICS

At T_A = +25°C and V_S = ±15V, unless otherwise noted.

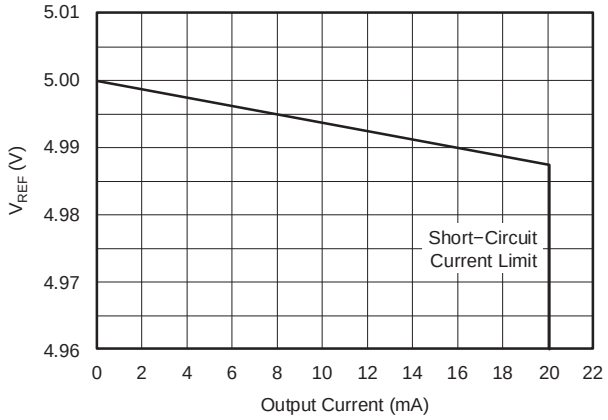
FULL−SCALE FREQUENCY
vs EXTERNAL ONE−SHOT CAPACITOR



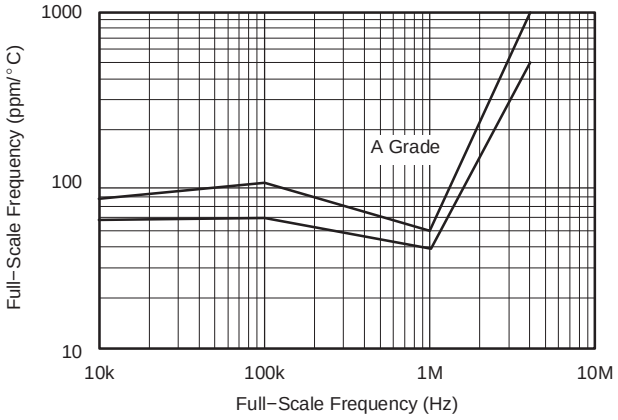
QUIESCENT CURRENT vs TEMPERATURE



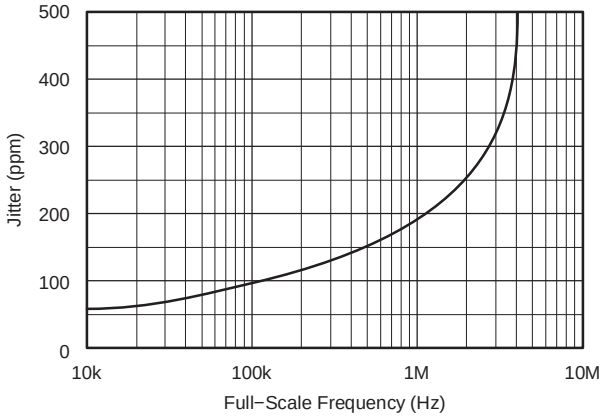
REFERENCE VOLTAGE
vs REFERENCE LOAD CURRENT



TYPICAL FULL−SCALE GAIN DRIFT
vs FULL−SCALE FREQUENCY

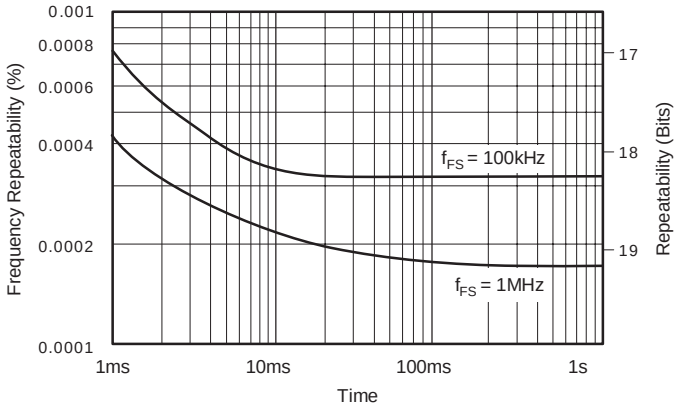


JITTER vs FULL−SCALE FREQUENCY



Jitter is the ratio of the 1σ value of the distribution of the period ($1/f_{OUT}$, max) to the mean of the period.

FREQUENCY COUNT REPEATABILITY
vs COUNTER GATE TIME

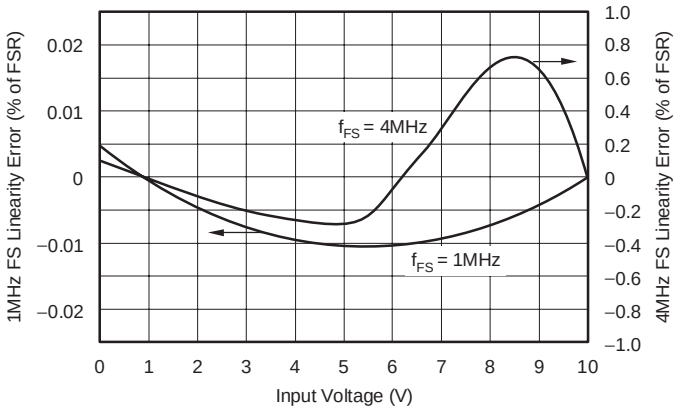


This graph describes the low frequency stability of the VFC110: the ratio of the 1σ point of the distribution of 100 runs (where each mean frequency came from 1000 readings for each gate time) to the overall mean frequency.

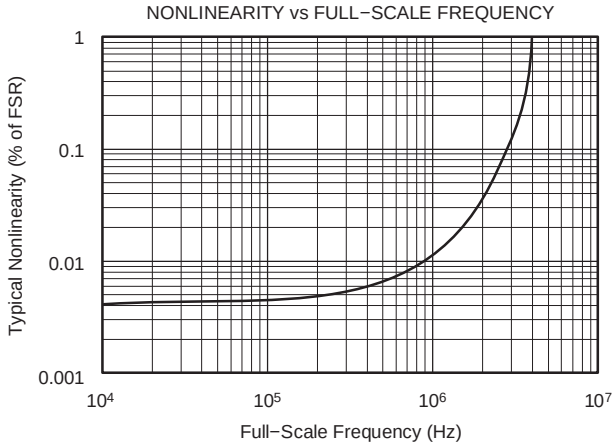
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_S = ±15V, unless otherwise noted.

NONLINEARITY vs INPUT VOLTAGE



NONLINEARITY vs FULL−SCALE FREQUENCY



OPERATION

Figure 1 shows the connections required for operation at a full-scale output frequency of 4MHz. Only power supply bypass capacitors and an output pull-up resistor, R_{PU}, are required for this mode of operation. A 0V to 10V input voltage produces a 0Hz to 4MHz output frequency. The internal input resistor, one-shot and integrator capacitors set the full-scale output frequency. The input is applied to the summing junction of the integrator amplifier through the 25kΩ internal input resistor. Pin 14 (the noninverting amplifier input) should be referred directly to the negative side of V_{IN}. The common-mode range of the integrating amplifier is limited to approximately −1V to +1V referred to analog ground. This allows the noninverting input to Kelvin-sense the common connection of V_{IN}, easily accommodating any ground-drop errors. The input impedance loading V_{IN} is equal to the input resistor—approximately 25kΩ.

OPERATION AT LOWER FREQUENCIES

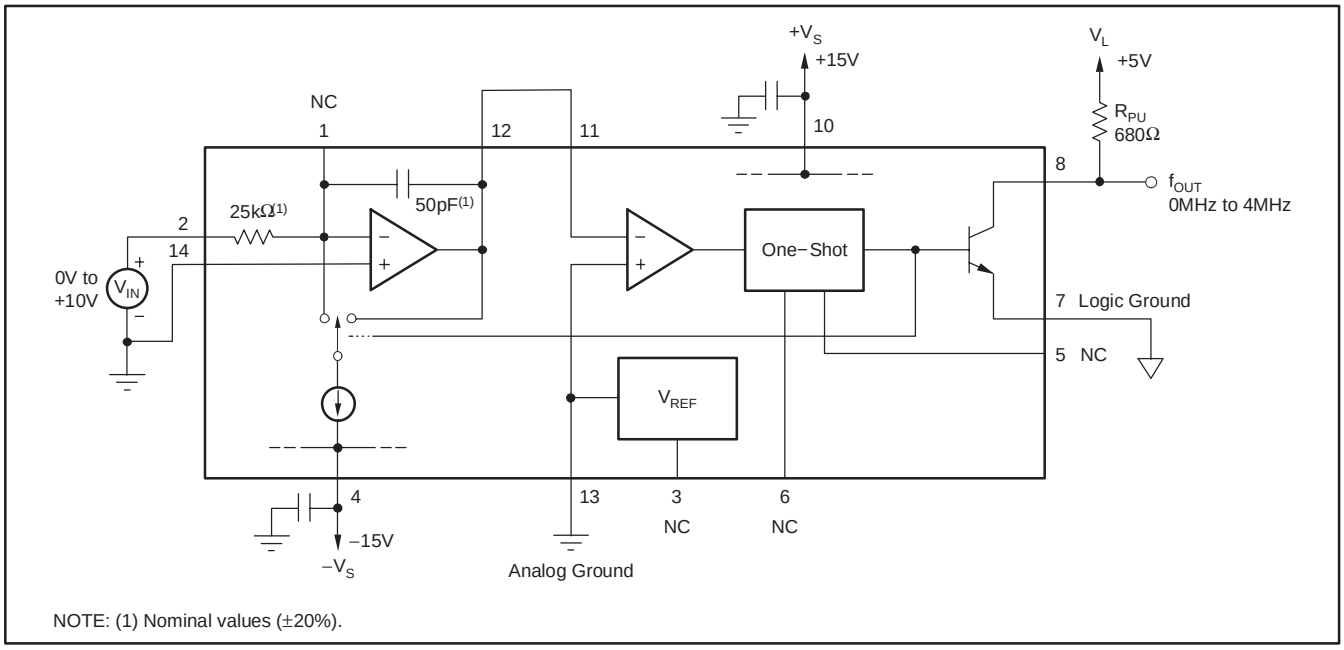
The VFC110 can be operated at lower frequencies simply by limiting the input voltage to less than the nominal 10V full-scale input. To maintain a 10V FS input and highest accuracy, however, external components are required (see Table 1). Small adjustments may be required in the nominal values indicated. Integrator and one-shot capacitors are added in parallel to internal capacitors. Figure 2 illustrates the connections required for 100kHz full-scale output. The one-shot capacitor, C_{OS}, should be connected to logic ground. The one-shot connection (pin 6) is not short-circuit protected. Short-circuits to ground may damage the device.

The integrator capacitor's value does not directly affect the output frequency, but determines the magnitude of the voltage swing on the integrator's output. Using a C_{INT} equal to C_{OS} provides an integrator output swing from 0V to approximately 1.5V.

COMPONENT SELECTION

Selection of the external resistor and capacitor type is important. Temperature drift of an external input resistor and one-shot capacitor will affect temperature stability of the output frequency. NPO ceramic capacitors will normally produce the best results. Silver-mica types will result in slightly higher drift, but may be adequate in many applications. A low temperature coefficient film resistor should be used for R_{IN}.

The integrator capacitor serves as a *charge bucket*, where charge is accumulated from the input, V_{IN}, and that charge is drained during the one-shot period. While the size of the bucket (capacitor value) is not critical, it must not leak. Capacitor leakage or dielectric absorption can affect the linearity and offset of the transfer function. High-quality ceramic capacitors can be used for values less than 0.01μF. Use caution with higher value ceramic capacitors. High-k ceramic capacitors may have voltage nonlinearities which can degrade overall linearity. Polystyrene, polycarbonate, or mylar film capacitors are superior for high values.



NOTE: (1) Nominal values (±20%).

Figure 1. 4MHz Full-Scale Operation

Table 1. Component Selection Table

FULL-SCALE FREQUENCY, f_{FS}	EXTERNAL COMPONENTS		
	R_{IN}	C_{OS}	C_{INT}
4MHz	*	*	*
2MHz	34kΩ	56pF	*
1MHz	40kΩ	150pF	*
500kHz	58kΩ	330pF	2nF
100kHz	44kΩ	2.2nF	10nF
50kHz	88kΩ	2.2nF	0.1µF
10kHz	44kΩ	22nF	0.1µF

* Use internal component only.
The values given were determined empirically to give the optimal performance, taking into consideration tradeoffs between linearity and jitter for each given full-scale frequency of operation. The capacitors listed were chosen from standard values of NPO ceramic type capacitors while the resistor values were rounded off. Larger C_{INT} values may improve linearity, but may also increase frequency noise.

PULL-UP RESISTOR

The VFC110 frequency output is an open-collector transistor. A pull-up resistor should be connected from f_{OUT} to the logic supply voltage, $+V_L$. The output transistor is On during the one-shot period, causing the output to be a logic Low. The current flowing in this resistor should be limited to 8mA to assure a 0.4V maximum logic Low. The value chosen for the pull-up resistor may depend on the full-scale frequency and capacitance on the output line. Excessive capacitance on f_{OUT} will cause a slow, rounded rising edge at the end of an output pulse. This effect can be minimized by using a pull-up resistor which sets the output current to its maximum of 8mA. The logic power supply can be any positive voltage up to $+V_S$.

ENABLE PIN

If left unconnected, the Enable input will assume a logic High level, enabling operation. Alternatively, the Enable input may be connected directly to $+V_S$. Since an internal pull-up current is included, the Enable input may be driven by an open-collector logic signal.

A logic Low at the Enable input causes output pulses to cease. This is accomplished by interrupting the signal path through the one-shot circuitry. While disabled, all circuitry remains active and quiescent current is unchanged. Since no reset current pulses can occur while disabled, any positive input voltage will cause the integrator op amp to ramp negatively and saturate at its most negative output swing of approximately −0.7V.

When the Enable input receives a logic High (greater than +2V), a reset current cycle is initiated (causing f_{OUT} to go Low). The integrator ramps positively and normal operation is established. The time required for the output frequency to stabilize is equal to approximately one cycle of the final output frequency plus 1µs.

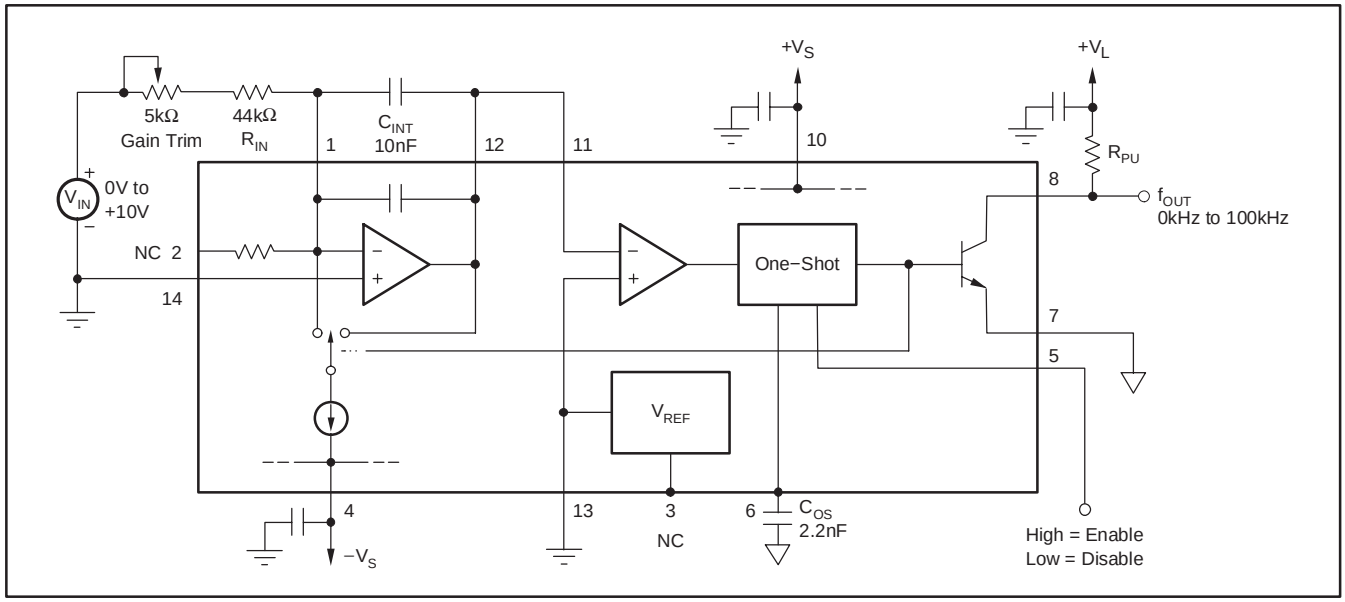


Figure 2. 100kHz Full-Scale Operation

PRINCIPLE OF OPERATION

The VFC110 uses a charge-balance technique to achieve high accuracy. The heart of this technique is an analog integrator formed by the integrator op amp, feedback capacitor C_{INT}, and input resistor R_{IN}. The integrator's output voltage is proportional to the charge stored in C_{INT}. An input voltage develops an input current of V_{IN}/R_{IN}, which is forced to flow through C_{INT}. This current charges C_{INT}, causing the integrator output voltage to ramp negatively.

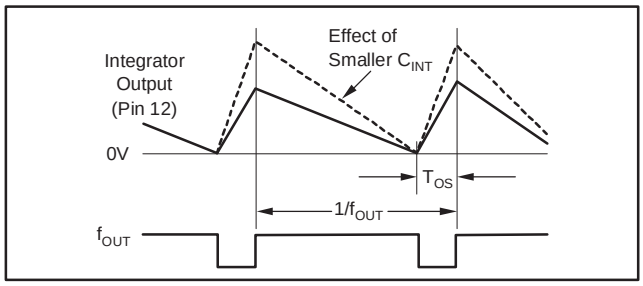
When the output of the integrator ramps to 0V, the comparator trips, triggering the one-shot. This connects the reference current, I_{REF}, (approximately 1mA) to the integrator input during the one-shot period, T_{OS}. This switched current causes the integrator output to ramp positively until the one-shot period ends. Then the cycle starts again.

The oscillation is regulated by the balance of current (or charge) between the input current and the time-averaged reset current. The equation of current balance is:

$$I_{IN} = I_{IREF} \times \text{Duty Cycle}$$

$$\frac{V_{IN}}{R_{IN}} = I_{REF} \times f_{OUT} \times T_O$$

where T_O is the one-shot period and f_{OUT} is the oscillation frequency.



Using the Enable input, several VFCs' outputs can be connected to a single output line. All disabled VFCs will have a high output impedance; one active VFC can then transmit on the output line. Since the disabled VFCs are not oscillating, they cannot interfere or *lock* with the operating VFC. Locking can occur when one VFC operates at nearly the same frequency as—or a multiple of—a nearby VFC. Coupling between the two may cause them to lock to the same or exact multiple frequency. It then takes a small incremental input voltage change to unlock them. Locking cannot occur when unneeded VFCs are disabled.

REFERENCE VOLTAGE

The V_{REF} output is useful for offsetting the transfer function and exciting sensors. Figure 3 shows V_{REF} used to offset the transfer function of the VFC110 to achieve a bipolar input voltage range. Sub-surface zener reference circuitry is used for low noise and excellent temperature drift. Output current is specified to 10mA and current-limited to approximately 20mA. Excessive or variable loads on V_{REF} can decrease frequency stability due to internal heating.

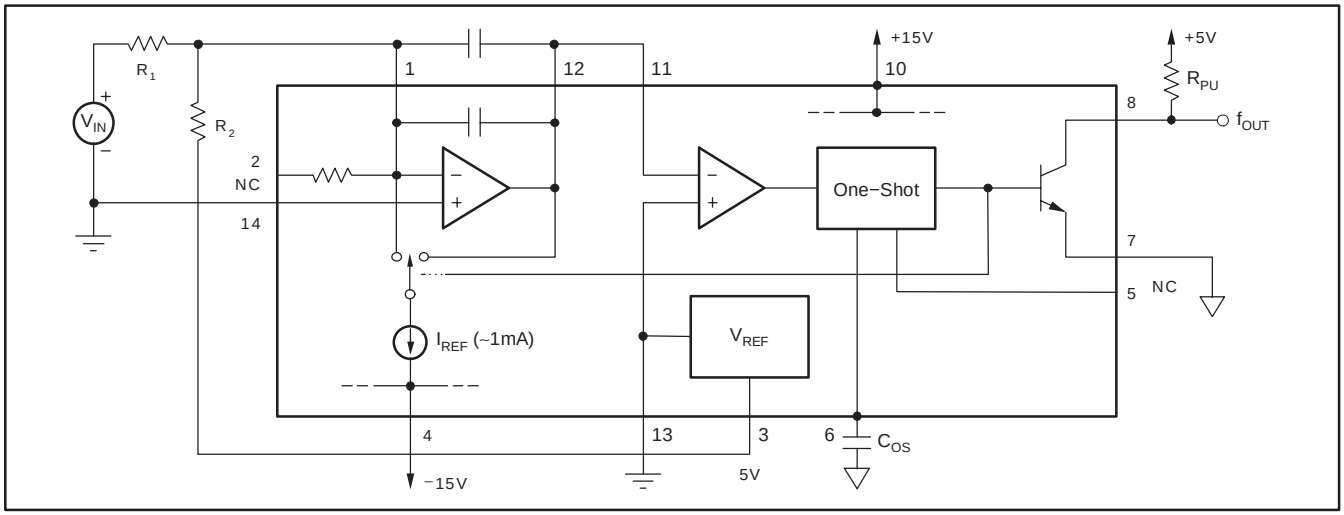


Figure 3. Offsetting the Frequency Output

MEASURING THE OUTPUT FREQUENCY

To complete an integrating A/D conversion, the output frequency of the VFC110 must be counted. Simple frequency counting is accomplished by counting output pulses for a reference time (usually derived from a crystal oscillator). This can be implemented with counter/timer peripheral chips available for many popular microprocessor families. Many microcontrollers have counter inputs that can be programmed for frequency measurement.

Since f_{OUT} is an open-collector device, the negative-going edge provides the fastest logic transition. Clocking the counter on the falling edge will provide the best results in noisy environments.

Frequency can also be measured by accurately timing the period of one or more cycles of the VFC output. Frequency must then be computed since it is inversely proportional to the measured period. This measurement technique can provide higher measurement resolution in short conversion times. It is the method used in most high-performance laboratory frequency counters. It is usually necessary to offset the transfer function so 0V input causes a finite frequency out. Otherwise the output period (and therefore the conversion time) approaches infinity.

FREQUENCY NOISE

Frequency noise (small random variation in the output frequency) limits the useful resolution of fast frequency measurement techniques. Long measurement time averages the effect of frequency noise and achieves the maximum useful resolution. The VFC110 is designed to minimize frequency noise and allows improved useful resolution with short measurement times. The typical characteristic curve *Frequency Count Repeatability vs Counter Gate Time* shows the effect of noise as the counter gate time is varied. It shows the one standard deviation (1σ) count variation (as a percentage of FS counts) versus counter gate time.

FREQUENCY-TO-VOLTAGE CONVERSION

The VFC110 can also be connected as a frequency-to-voltage converter (Figure 4). Input frequency pulses are applied to the comparator input. A negative-going pulse crossing 0V initiates a reference current pulse which is averaged by the integrator op amp. The values of the one-shot capacitor and feedback resistor (same as R_{IN}) are determined with Table 1. The input frequency pulse must not remain negative for longer than the duration of the one-shot period. Figure 4 shows the required timing to assure this. If the negative-going input frequency pulses are longer in duration, the capacitive coupling circuit shown can be used. Level shift or capacitive coupling circuitry should not provide pulses which go lower than −5V or damage to the comparator input may occur.

This frequency-to-voltage converter operates by averaging (filtering) the reference current pulses triggered on every falling edge at the frequency input. Voltage ripple with a frequency equal to the input will be present in the output voltage. The magnitude of this ripple voltage is inversely proportional to the integrator capacitor. The ripple can be made arbitrarily small with a large capacitor, but at the sacrifice of settling time. The R-C time constant of C_{INT} and R_{IN} determine the settling behavior. A better compromise between output ripple and settling time can be achieved by adding a low-pass filter following the voltage output.

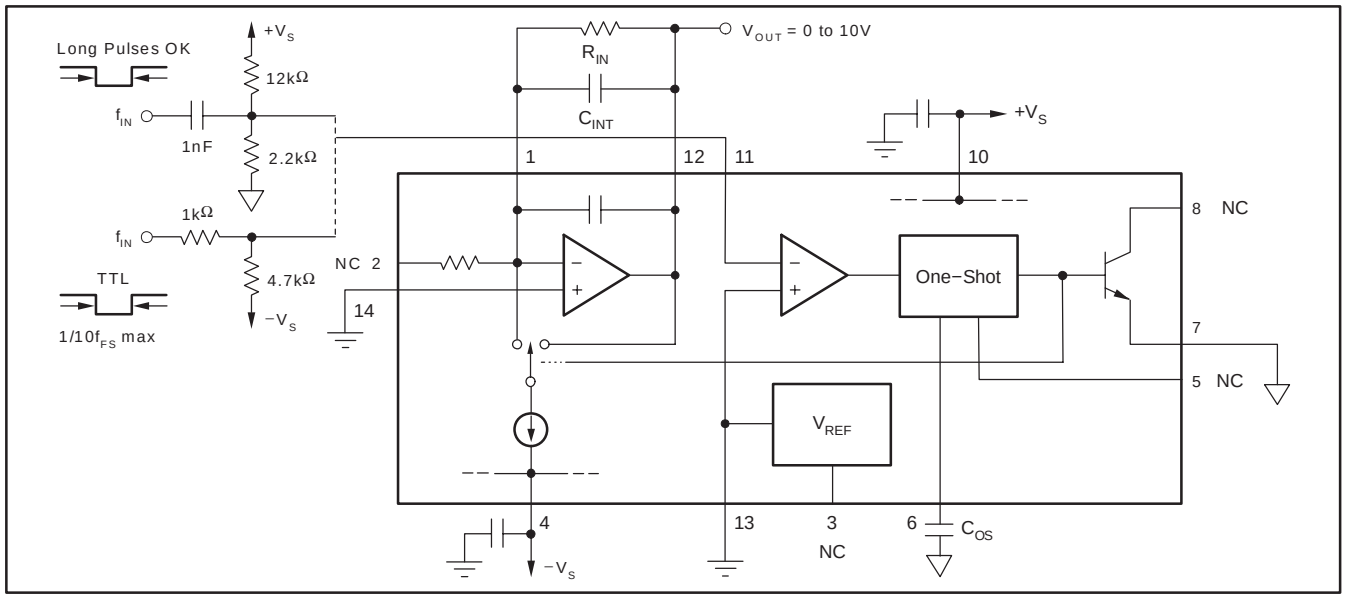


Figure 4. Frequency-to-Voltage Conversion

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
VFC110AP	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	VFC110AP
VFC110AP.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	VFC110AP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

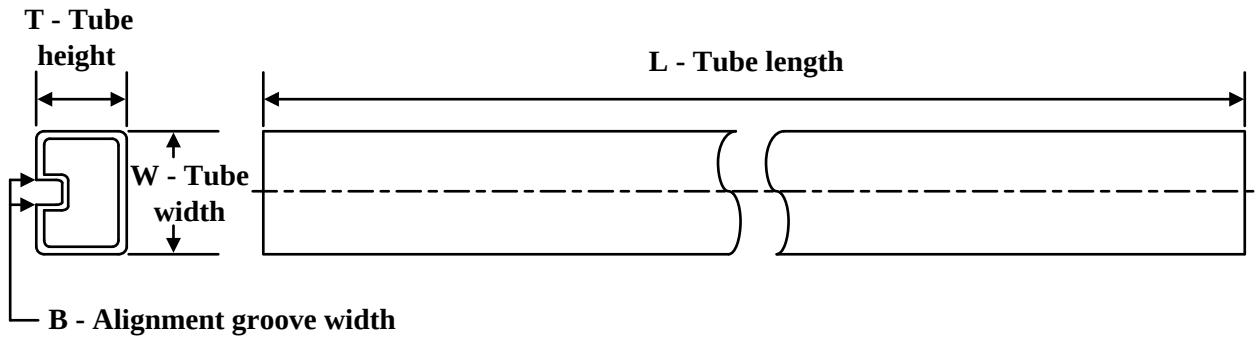
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



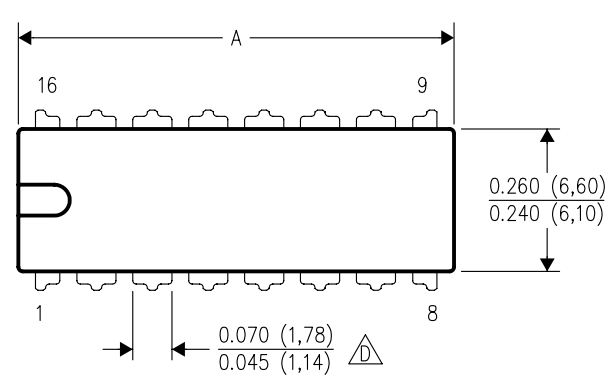
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
VFC110AP	N	PDIP	14	25	506	13.97	11230	4.32
VFC110AP.A	N	PDIP	14	25	506	13.97	11230	4.32

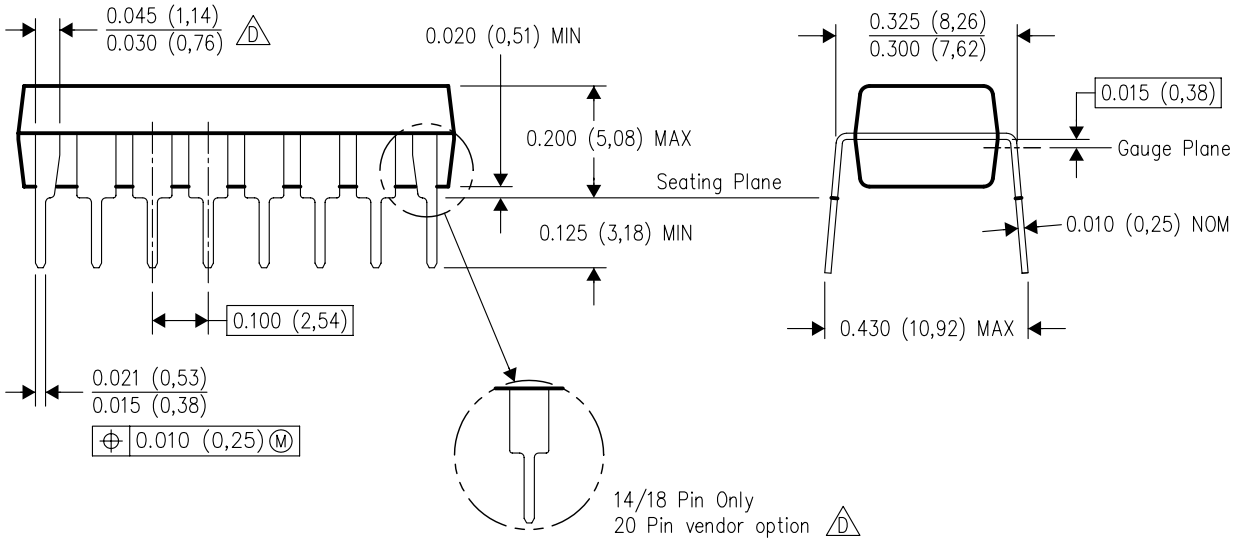
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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