

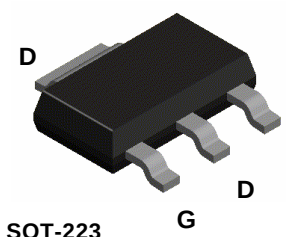
FDT457N N-Channel Enhancement Mode Field Effect Transistor

General Description

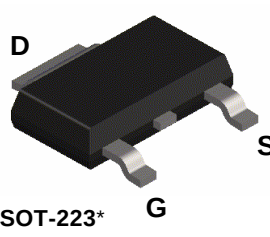
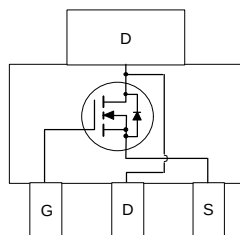
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance. These products are well suited to low voltage, low current applications such as notebook computer power management, battery powered circuits, and DC motor control.

Features

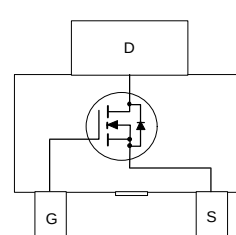
- 5 A, 30 V. $R_{DS(ON)} = 0.06 \Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 0.090 \Omega @ V_{GS} = 4.5 \text{ V}$.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



SOT-223



SOT-223*
(J23Z)



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDT457N	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage - Continuous	± 20	V
I_D	Maximum Drain Current - Continuous (Note 1a) - Pulsed	5	A
		16	
P_D	Maximum Power Dissipation (Note 1a) (Note 1b) (Note 1c)	3	W
		1.3	
		1.1	
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 150	$^\circ\text{C}$
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	12	$^\circ\text{C/W}$

* Order option J23Z for cropped center drain lead.

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
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OFF CHARACTERISTICS

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C		35		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
		T _J = 55°C			10	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	1.6	3	V
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C		-4.2		mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 5 A		0.043	0.06	Ω
		T _J = 125°C		0.065	0.1	
		V _{GS} = 4.5 V, I _D = 3.8 A		0.071	0.09	
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	5			A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 5 A		5		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz		235		pF
C _{oss}	Output Capacitance			145		pF
C _{rss}	Reverse Transfer Capacitance			50		pF

SWITCHING CHARACTERISTICS (Note 2)

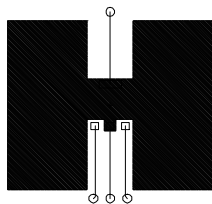
t _{D(on)}	Turn - On Delay Time	V _{DD} = 10 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		5	10	ns
t _r	Turn - On Rise Time			12	22	ns
t _{D(off)}	Turn - Off Delay Time			12	22	ns
t _f	Turn - Off Fall Time			3	8	ns
Q _g	Total Gate Charge	V _{DS} = 10 V, I _D = 5 A, V _{GS} = 5 V		4.2	5.9	nC
Q _{gs}	Gate-Source Charge			1.3		nC
Q _{gd}	Gate-Drain Charge			1.7		nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current					2.5	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.5 A (Note 2)			0.85	1.2	V

Notes:

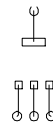
- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 42°C/W when mounted on a 1 in² pad of 2oz Cu.



b. 95°C/W when mounted on a 0.066 in² pad of 2oz Cu.



c. 110°C/W when mounted on a 0.00123 in² pad of 2oz Cu.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%

Typical Electrical Characteristics

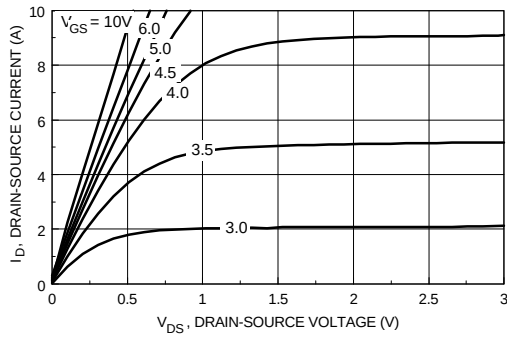


Figure 1. On-Region Characteristics.

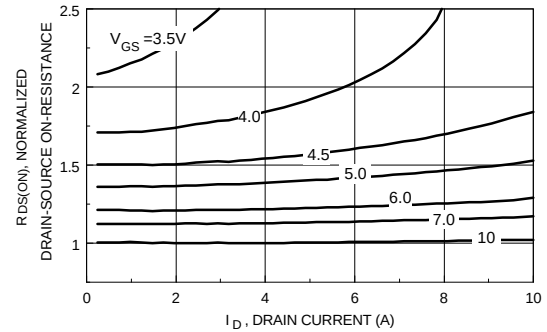


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

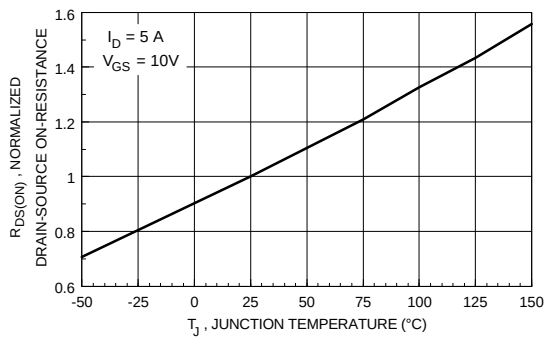


Figure 3. On-Resistance Variation with Temperature.

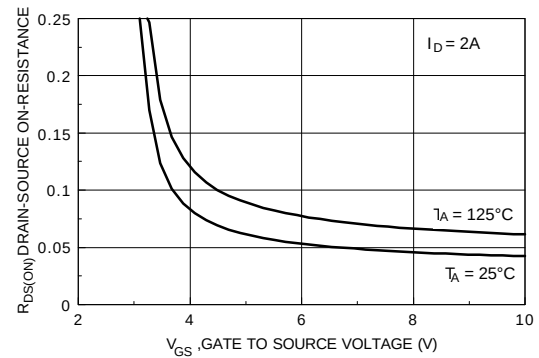


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

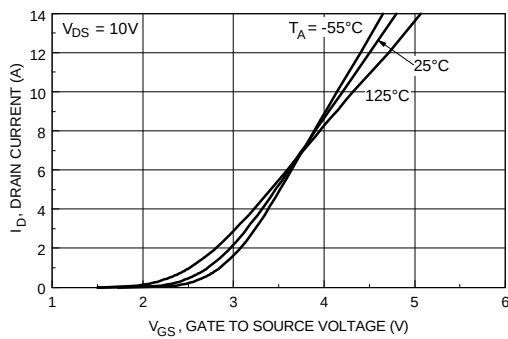


Figure 5. Transfer Characteristics.

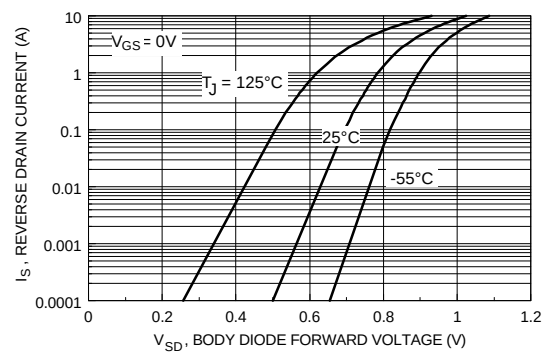


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics

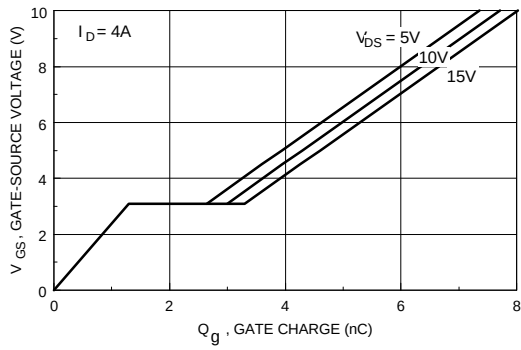


Figure 7. Gate Charge Characteristics.

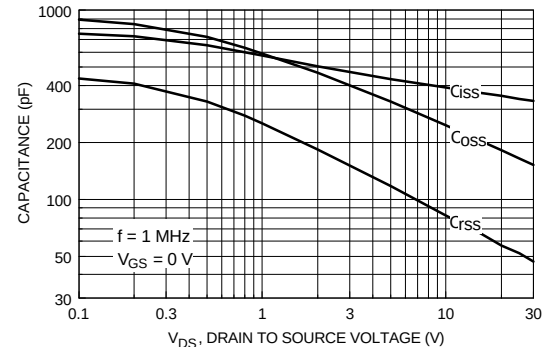


Figure 8. Capacitance Characteristics.

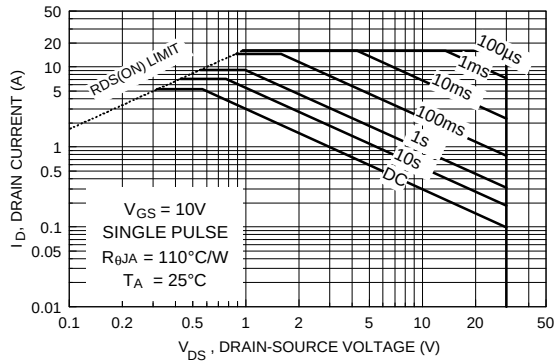


Figure 9. Maximum Safe Operating Area.

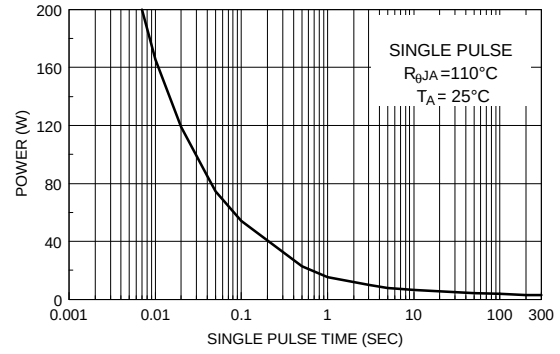


Figure 10. Single Pulse Maximum Power Dissipation.

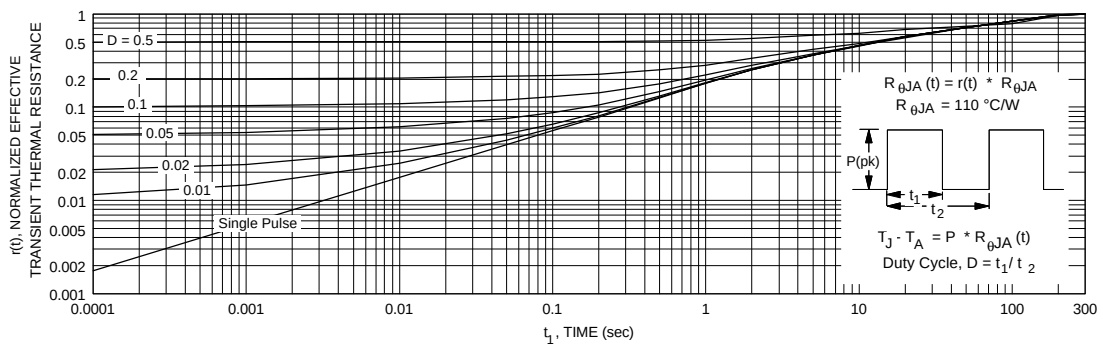


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1c.
Transient thermal response will change depending on the circuit board design.