



0.1 μ F, 5 V Powered CMOS RS-232 Drivers/Receivers

ADM205–ADM211/ADM213

FEATURES

0.1 μ F to 10 μ F Capacitors
120 kB/s Data Rate
Two Receivers Active in Shutdown (ADM213)
On-Board DC-DC Converters
 ± 9 V Output Swing with 5 V Supply
Low Power (15 mW)
Low-Power Shutdown ≤ 5 μ W
 ± 30 V Receiver Input Levels
Latch-Up FREE
Plug-In Upgrade for MAX205-211/213

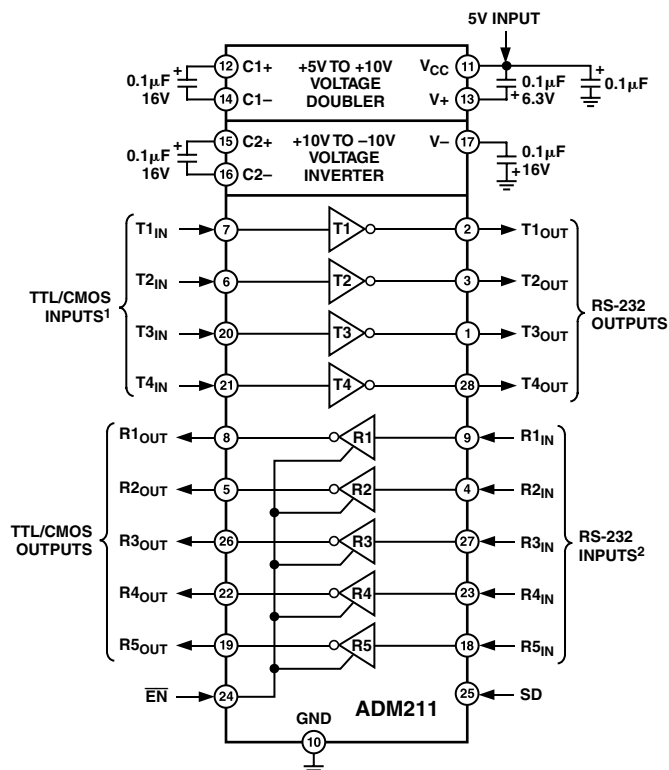
APPLICATIONS

Computers
Peripherals
Modems
Printers
Instruments

GENERAL DESCRIPTION

The ADM2xx family of line drivers/receivers is intended for all EIA-232-E and V.28 communications interfaces, especially in applications where ± 12 V is not available. The ADM205, ADM206, ADM211, and ADM213 feature a low power shutdown mode which reduces power dissipation to less than 5 μ W, making them ideally suited for battery powered equipment. The ADM205 does not require any external components and is particularly useful in applications where printed circuit board space is critical. The ADM213 has an active-low shutdown and an active-high receiver enable control. Two receivers of the ADM213 remain active during shutdown. This feature is useful for ring indicator monitoring.

TYPICAL OPERATING CIRCUIT



NOTES

¹INTERNAL 400k Ω PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
²INTERNAL 5k Ω PULL-DOWN RESISTOR ON EACH RS-232 INPUT

All members of the ADM2xx family, except the ADM209, include two internal charge pump voltage converters which allow operation from a single 5 V supply. These converters convert the 5 V input power to the ± 10 V required for RS-232 output levels. The ADM209 is designed to operate from 5 V and 12 V supplies. An internal +12 V to -12 V charge pump voltage converter generates the -12 V supply.

Table I. Selection Table

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Capacitors	Low Power Shutdown (SD)	TTL Three-State $\overline{\text{EN}}$	No. of Receivers Active in Shutdown
ADM205	5 V	5	5	None	Yes	Yes	0
ADM206	5 V	4	3	4	Yes	Yes	0
ADM207	5 V	5	3	4	No	No	0
ADM208	5 V	4	4	4	No	No	0
ADM209	5 V and 9 V to 13.2 V	3	5	2	No	Yes	0
ADM211	5 V	4	5	4	Yes	Yes	0
ADM213	5 V	4	5	4	Yes ($\overline{\text{SD}}$)	Yes (EN)	2

REV. A

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ADM205–ADM211/ADM213–SPECIFICATIONS

($V_{CC} = 5\text{ V} \pm 10\%$ (206, 207, 208, 209, 211, 213); $V_{CC} = 5\text{ V} \pm 5\%$ (ADM205); $V_+ = 9\text{ V}$ to 13.2 V (ADM209); C_1 – $C_4 = 0.1\text{ }\mu\text{F}$ Ceramic. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Swing	± 5	± 9		Volts	All Transmitter Outputs Loaded with 3 k Ω to Ground
V_{CC} Power Supply Current		5	13	mA	No Load
V_+ Power Supply Current		0.4	1	mA	No Load, ADM209
Shutdown Supply Current		3.5	5	mA	No Load, $V_+ = 12\text{ V}$ ADM209 Only
Input Logic Threshold Low, V_{INL}		1	10	μA	
Input Logic Threshold High, V_{INH}	2.4		0.8	V	$T_{IN}, \overline{EN}, SD, EN, \overline{SD}$
Logic Pull-Up Current		10	25	μA	$T_{IN}, \overline{EN}, SD, EN, \overline{SD}$
RS-232 Input Voltage Range ¹	–30		+30	V	$T_{IN} = 0\text{ V}$
RS-232 Input Threshold Low	0.8	1.2		V	
RS-232 Input Threshold High		1.7	2.4	V	
RS-232 Input Hysteresis		0.25		V	
RS-232 Input Resistance	3	5	7	k Ω	$T_A = 0^\circ\text{C}$ to 85°C
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	$I_{OUT} = 1.6\text{ mA}$
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	$I_{OUT} = -1.0\text{ mA}$
TTL/CMOS Output Leakage Current		0.05	± 10	μA	$\overline{EN} = V_{CC}, EN = 0\text{ V}, 0\text{ V} \leq R_{OUT} \leq V_{CC}$
Output Enable Time (T_{EN})		115		ns	ADM205, ADM206, ADM209, ADM211 (Figure 17. $C_L = 150\text{ pF}$)
Output Disable Time (T_{DIS})		165		ns	ADM205, ADM206, ADM209, ADM211 (Figure 17. $R_L = 1\text{ k}\Omega$)
Propagation Delay		0.5	5	μs	RS-232 to TTL
Transition Region Slew Rate		8		V/ μs	$R_L = 3\text{ k}\Omega, C_L = 2500\text{ pF}$
Output Resistance	300			Ω	Measured from +3 V to –3 V or –3 V to +3 V
RS-232 Output Short Circuit Current		± 12	± 60	mA	$V_{CC} = V_+ = V_- = 0\text{ V}, V_{OUT} = \pm 2\text{ V}$

NOTES

¹Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{CC}	–0.3 V to +6 V
V_+	($V_{CC} - 0.3\text{ V}$) to +14 V
V_-	+0.3 V to –14 V

Input Voltages

T_{IN}	–0.3 V to ($V_{CC} + 0.3\text{ V}$)
R_{IN}	$\pm 30\text{ V}$

Output Voltages

T_{OUT}	($V_+, +0.3\text{ V}$) to ($V_-, -0.3\text{ V}$)
R_{OUT}	–0.3 V to ($V_{CC} + 0.3\text{ V}$)

Short Circuit Duration

T_{OUT}	Continuous
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Power Dissipation

N-24 DIP (Derate 13.5 mW/ $^\circ\text{C}$ above 70°C)	... 1000 mW
N-24A DIP (Derate 13.5 mW/ $^\circ\text{C}$ above 70°C)	... 500 mW
R-24 SOIC (Derate 12 mW/ $^\circ\text{C}$ above 70°C)	... 850 mW
R-28 SOIC (Derate 12.5 mW/ $^\circ\text{C}$ above 70°C)	... 900 mW
RS-28 SSOP (Derate 10 mW/ $^\circ\text{C}$ above 70°C)	... 900 mW
Q-24 Cerdip (Derate 12.5 mW/ $^\circ\text{C}$ above 70°C)	... 1000 mW
D-24 Ceramic (Derate 20 mW/ $^\circ\text{C}$ above 70°C)	... 1000 mW

Thermal Impedance, θ_{JA}

N-24 DIP	120 $^\circ\text{C/W}$
N-24A DIP	110 $^\circ\text{C/W}$
R-24 SOIC	85 $^\circ\text{C/W}$
R-28 SOIC	80 $^\circ\text{C/W}$
RS-28 SSOP	100 $^\circ\text{C/W}$
Q-14 Cerdip	105 $^\circ\text{C/W}$
Q-16 Cerdip	100 $^\circ\text{C/W}$
Q-20 Cerdip	100 $^\circ\text{C/W}$
Q-24 Cerdip	55 $^\circ\text{C/W}$
D-24 Ceramic	50 $^\circ\text{C/W}$

Operating Temperature Range

Industrial (A Version)	–40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
Storage Temperature Range	–65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature, Soldering	300 $^\circ\text{C}$
Vapor Phase (60 sec)	215 $^\circ\text{C}$
Infrared (15 sec)	220 $^\circ\text{C}$

*This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM205–ADM211/ADM213 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model	Temperature Range	Package Option*	Model	Temperature Range	Package Option*	Model	Temperature Range	Package Option*
ADM205 ADM205AN	–40°C to +85°C	N-24A	ADM206 ADM206AN ADM206AR ADM206ARS	–40°C to +85°C –40°C to +85°C –40°C to +85°C	N-24 R-24 RS-24	ADM207 ADM207AN ADM207AR ADM207ARS	–40°C to +85°C –40°C to +85°C –40°C to +85°C	N-24 R-24 RS-24
ADM208 ADM208AN ADM208AR ADM208ARS	–40°C to +85°C –40°C to +85°C –40°C to +85°C	N-24 R-24 RS-24	ADM209 ADM209AN ADM209AR ADM209ARS	–40°C to +85°C –40°C to +85°C –40°C to +85°C	N-24 R-24 RS-24	ADM211 ADM211AR ADM211ARS	–40°C to +85°C –40°C to +85°C	R-28 RS-28
ADM213 ADM213AR ADM213ARS	–40°C to +85°C –40°C to +85°C	R-28 RS-28						

*N = Plastic DIP; R = Small Outline IC (SOIC); RS = Small Shrink Outline Package (SSOP).

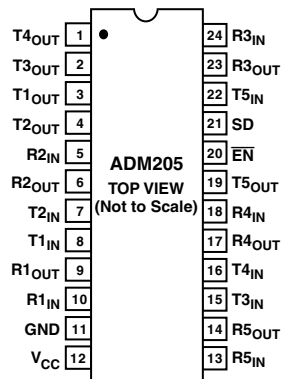
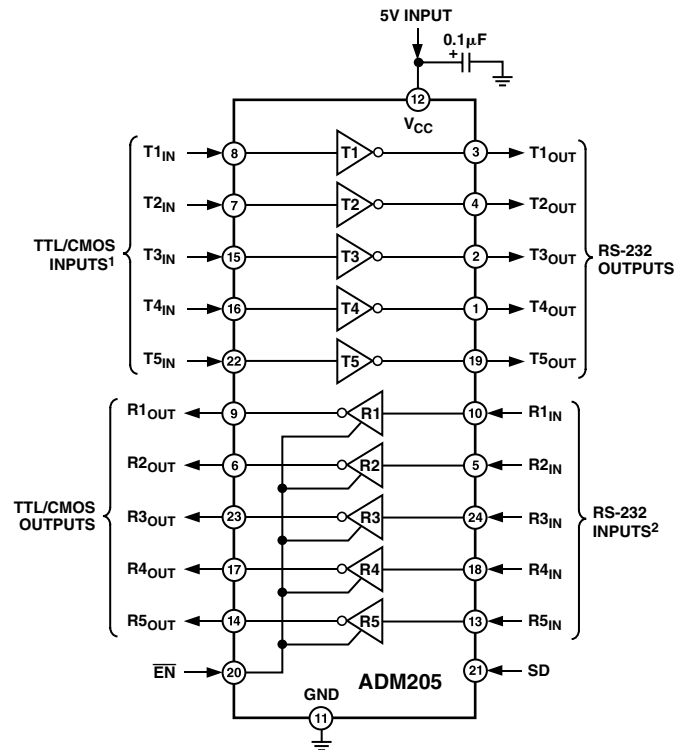


Figure 1. ADM205 DIP Pin Configuration



NOTES

- ¹INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
- ²INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 2. ADM205 Typical Operating Circuit

ADM205–ADM211/ADM213

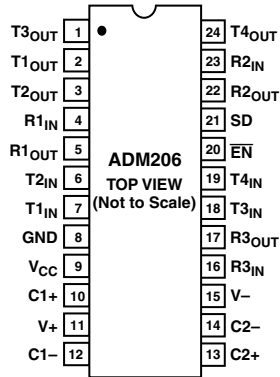


Figure 3. ADM206 DIP/SOIC/SSOP Pin Configuration

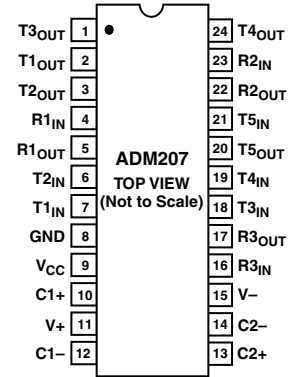
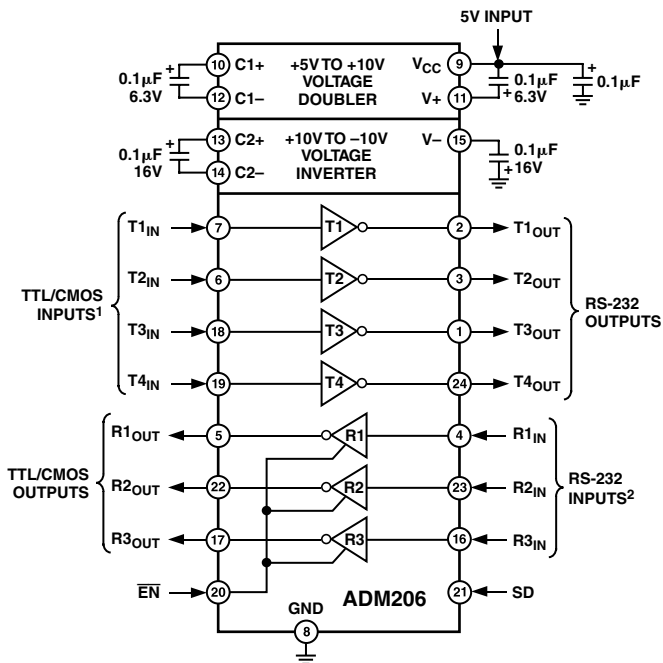


Figure 5. ADM207 DIP/SOIC/SSOP Pin Configuration

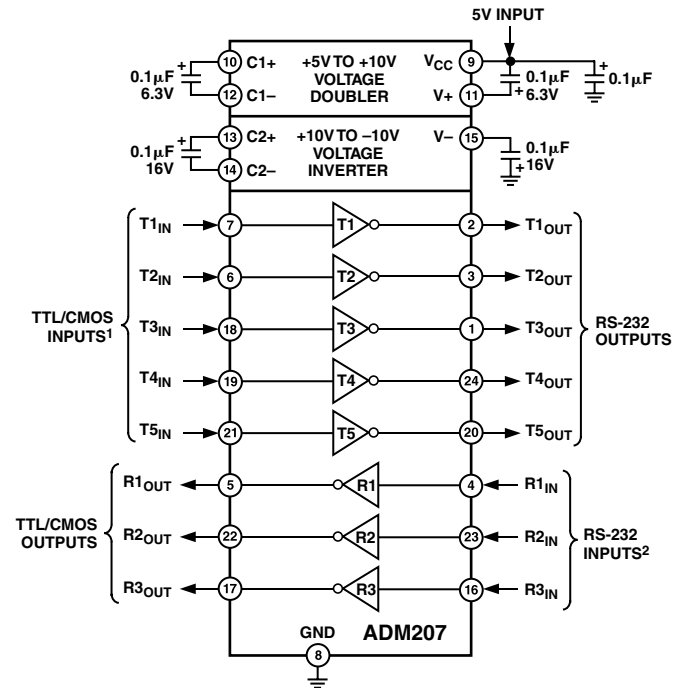


NOTES

¹INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT

²INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 4. ADM206 Typical Operating Circuit



NOTES

¹INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT

²INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 6. ADM207 Typical Operating Circuit

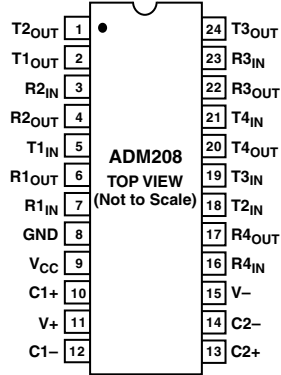


Figure 7. ADM208 DIP/SOIC/SSOP Pin Configuration

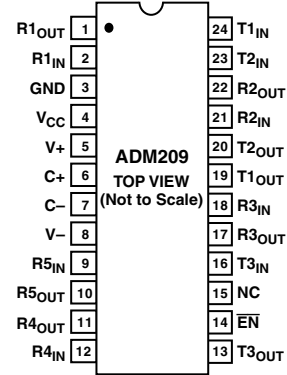
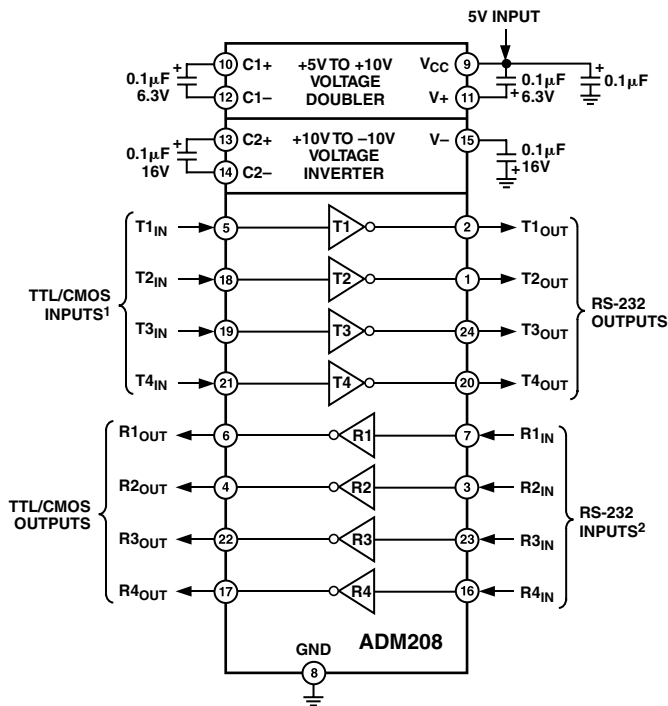


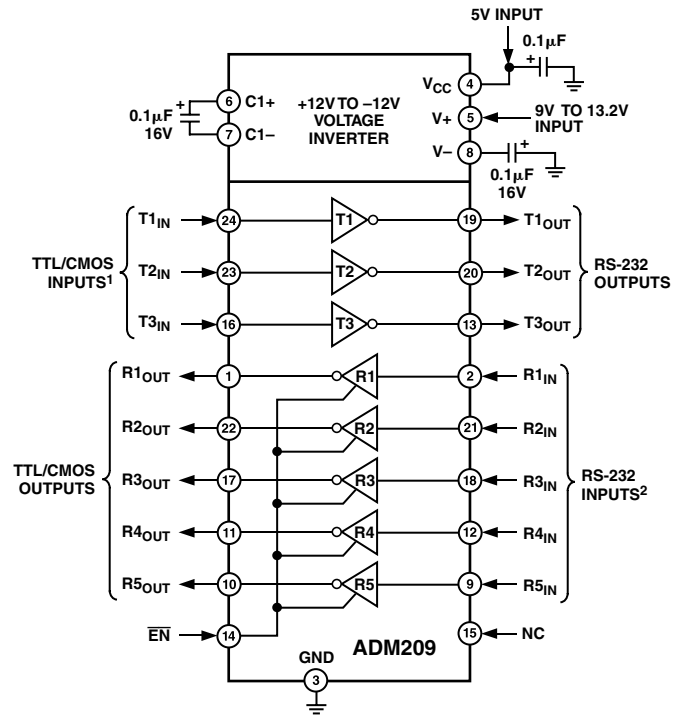
Figure 9. ADM209 DIP/SOIC/SSOP Pin Configuration



NOTES

- ¹INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
- ²INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 8. ADM208 Typical Operating Circuit



NOTES

- ¹INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
- ²INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 10. ADM209 Typical Operating Circuit

ADM205–ADM211/ADM213

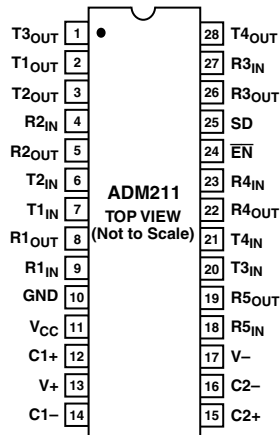
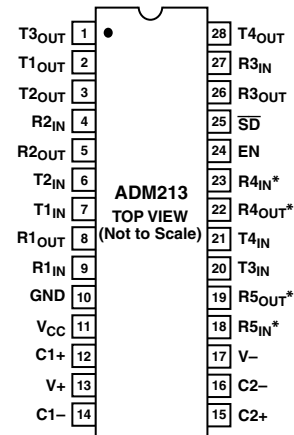
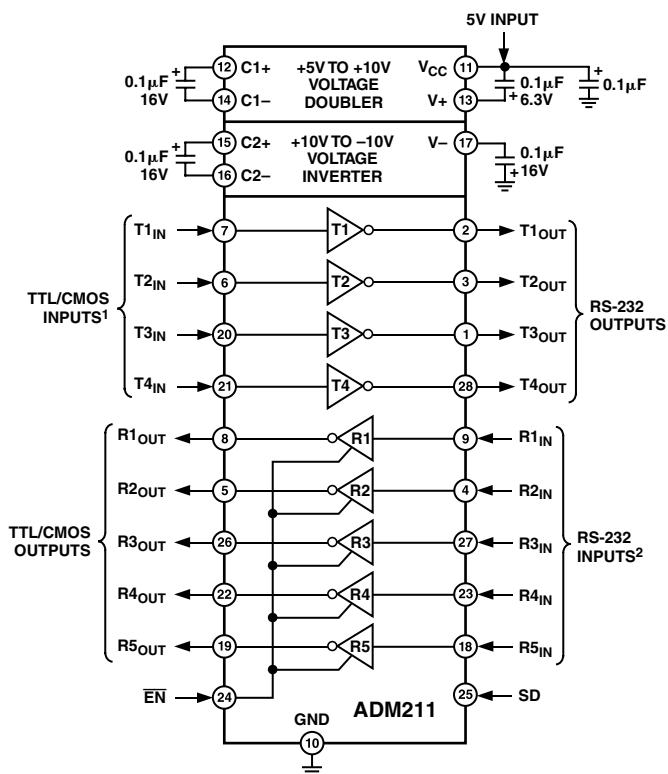


Figure 11. ADM211 SOIC/SSOP Pin Configuration



*ACTIVE IN SHUTDOWN

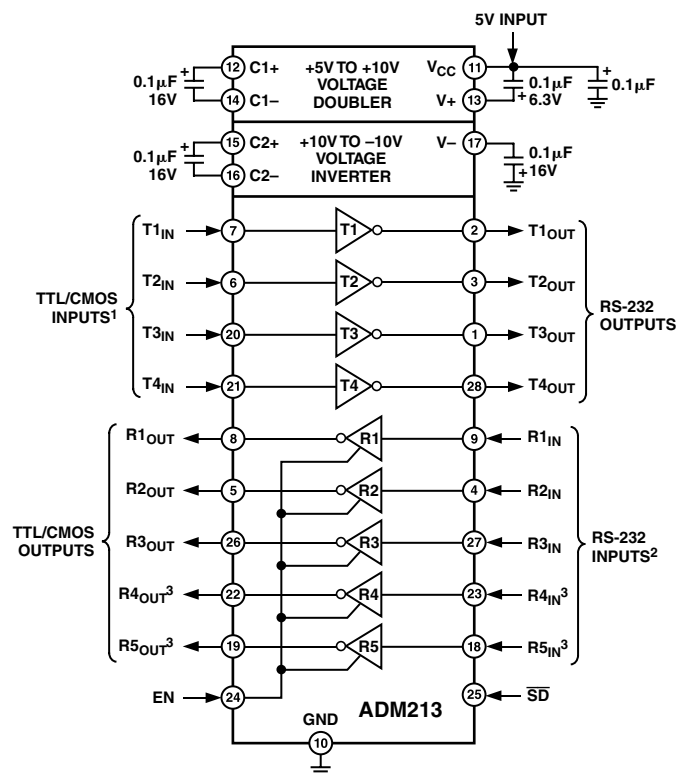
Figure 13. ADM213 SOIC/SSOP Pin Configuration



NOTES

- ¹INTERNAL 400k Ω PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
- ²INTERNAL 5k Ω PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 12. ADM211 Typical Operating Circuit



NOTES

- ¹INTERNAL 400k Ω PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
- ²INTERNAL 5k Ω PULL-DOWN RESISTOR ON EACH RS-232 INPUT
- ³ACTIVE IN SHUTDOWN

Figure 14. ADM213 Typical Operating Circuit

PIN FUNCTION DESCRIPTIONS

Mnemonic	Function
V _{CC}	Power Supply Input 5 V ± 10% (5 V ± 5% ADM205).
V+	Internally generated positive supply (10 V nominal) on all parts except ADM209. ADM209 requires external 9 V to 13.2 V supply.
V–	Internally generated negative supply (–10 V nominal).
GND	Ground Pin. Must be connected to 0 V.
C+	(ADM209 only) External capacitor (+ terminal) is connected to this pin.
C–	(ADM209 only) External capacitor (– terminal) is connected to this pin.
C1+	(ADM206, ADM207, ADM208, ADM211, ADM213) External capacitor (+ terminal) is connected to this pin.
C1–	(ADM206, ADM207, ADM208, ADM211, ADM213) External capacitor (– terminal) is connected to this pin.
C2+	(ADM206, ADM207, ADM208, ADM211, ADM213) External capacitor (+ terminal) is connected to this pin.
C2–	(ADM206, ADM207, ADM208, ADM211, ADM213) External capacitor (– terminal) is connected to this pin.
T _{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V _{CC} is connected on each input.
T _{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ±10 V).
R _{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each input.
R _{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{\text{EN}}/\text{EN}$	Enable Input. Active low on ADM205, ADM206, ADM209, ADM211. Active high on ADM213. This input is used to enable/disable the receiver outputs. With $\overline{\text{EN}}$ = Low (EN = High ADM213), the receiver outputs are enabled. With $\overline{\text{EN}}$ = High (EN = Low ADM213), the outputs are placed in a high impedance state. This facility is useful for connecting to microprocessor systems.
SD/ $\overline{\text{SD}}$	Shutdown Input. Active high on ADM205, ADM206, ADM211. Active low on ADM213. With SD = high on the ADM205, ADM206, ADM211, the charge pump is disabled, the receiver outputs are placed in a high impedance state and the driver outputs are turned off. With $\overline{\text{SD}}$ low on the ADM213, the charge pump is disabled, the driver outputs are turned off and all receivers except R4 and R5 are placed in a high impedance state. In shutdown, the power consumption reduces to 5 μW.
NC	No Connect. No connections are required to this pin.

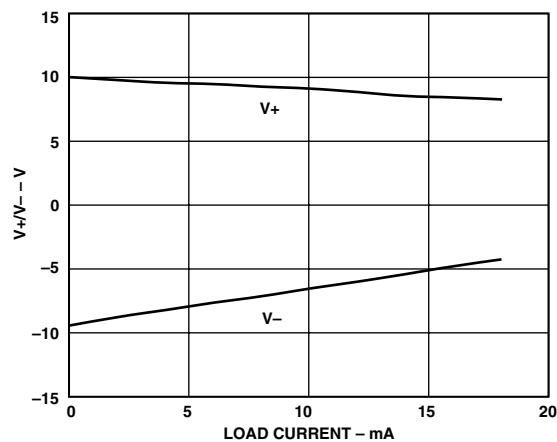
Table II. ADM205, ADM206, ADM211 Truth Table

SD	$\overline{\text{EN}}$	Status	Transmitters T1–T5	Receivers R1–R5
0	0	Normal Operation	Enabled	Enabled
0	1	Normal Operation	Enabled	Disabled
1	0	Shutdown	Disabled	Disabled

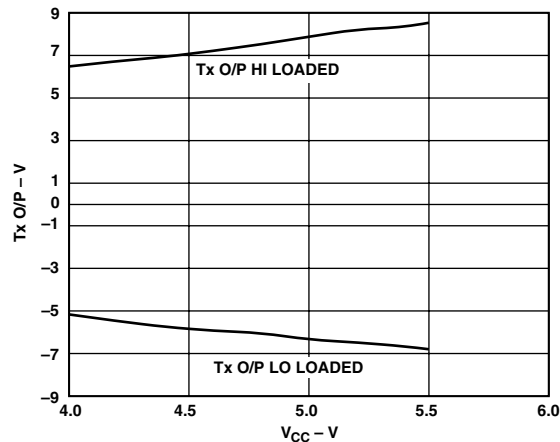
Table III. ADM213 Truth Table

$\overline{\text{SD}}$	EN	Status	Transmitters T1–T4	Receivers R1–R3	Receivers R4, R5
0	0	Shutdown	Disabled	Disabled	Disabled
0	1	Shutdown	Disabled	Disabled	Enabled
1	0	Normal Operation	Enabled	Disabled	Disabled
1	1	Normal Operation	Enabled	Enabled	Enabled

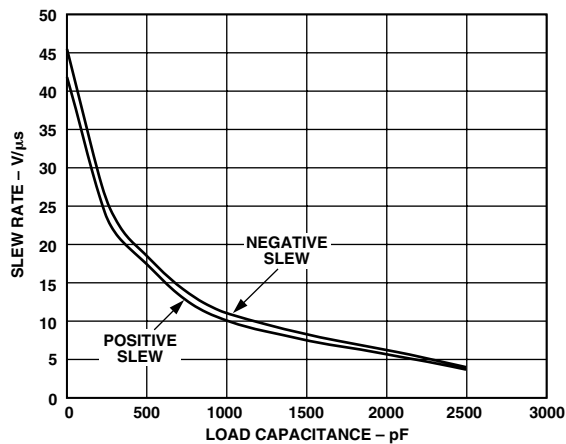
ADM205–ADM211/ADM213



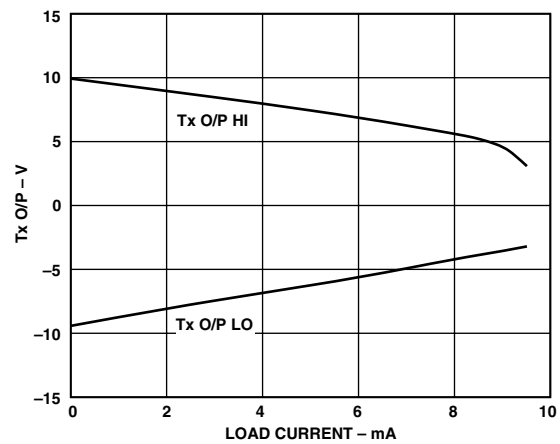
TPC 1. Charge Pump V_+ , V_- vs. Load Current



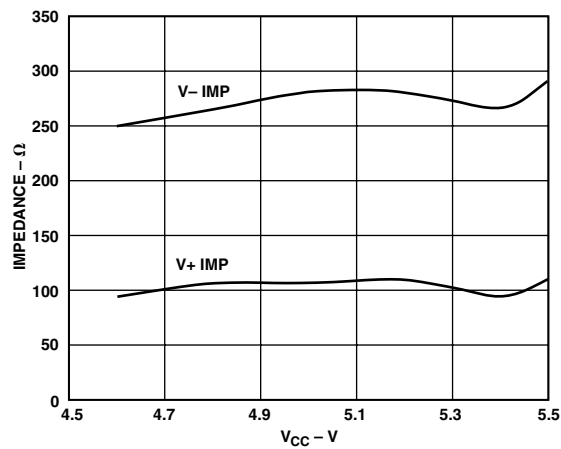
TPC 3. Transmitter Output Voltage vs. V_{CC}



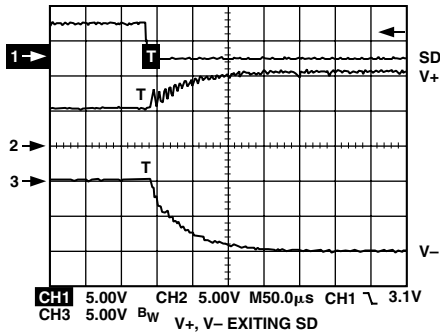
TPC 2. Transmitter Slew Rate vs. Load Capacitance



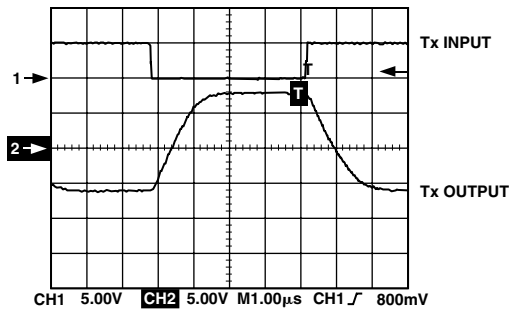
TPC 4. Transmitter Output Voltage vs. Load Current



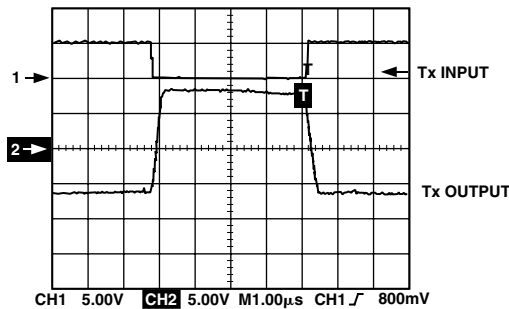
TPC 5. Charge Pump Impedance vs. V_{CC}



TPC 6. Charge Pump, V+, V- Exiting Shutdown



TPC 7. Transmitter Output Loaded Slew Rate



TPC 8. Transmitter Output Unloaded Slew Rate

GENERAL INFORMATION

The ADM205-ADM211 and ADM213 family of RS-232 drivers/receivers are designed to solve interface problems by meeting the EIA-232-E specifications while using a single digital 5 V supply. The EIA-232-E standard requires transmitters which will deliver ± 5 V minimum on the transmission channel and receivers which can accept signal levels down to ± 3 V. The ADM205-ADM211 and ADM213 meet these requirements by integrating step up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum. A comprehensive range of transmitter/receiver combinations is available to cover most communications needs. The ADM205-ADM211 and ADM213 are modifications, enhancements and improvements to the AD230-AD241 family and derivatives

thereof. They are essentially plug-in compatible and do not have materially different applications.

The ADM205, ADM206, ADM211, and ADM213 are particularly useful in battery-powered systems as they feature a low power shutdown mode which reduces power dissipation to less than 5 μ W.

The ADM205 is designed for applications where space saving is important as the charge pump capacitors are molded into the package.

The ADM209 includes only a negative charge pump converter and are intended for applications where a positive 12 V is available.

To facilitate sharing a common line or for connection to a microprocessor data bus, the ADM205, ADM206, ADM209, ADM211, and ADM213 feature an enable ($\overline{\text{EN}}$) function. When disabled, the receiver outputs are placed in a high impedance state.

CIRCUIT DESCRIPTION

The internal circuitry in the ADM205-ADM211 and ADM213 consists of three main sections. These are:

- (a) A charge pump voltage converter
- (b) RS-232 to TTL/CMOS receivers
- (c) TTL/CMOS to RS-232 transmitters

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ± 10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique as illustrated in Figures 15 and 16. First, the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate -10 V using C2 as the storage element.

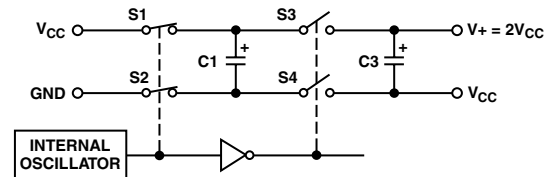


Figure 15. Charge-Pump Voltage Doubler

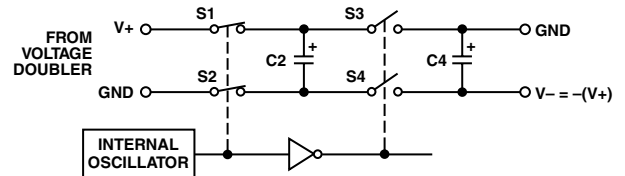


Figure 16. Charge-Pump Voltage Inverter

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V- supplies.

The V+ and V- supplies may also be used to power external circuitry if the current requirements are small.

ADM205–ADM211/ADM213

Transmitter (Driver) Section

The drivers convert TTL/CMOS input levels into EIA-232-E output levels. With $V_{CC} = 5\text{ V}$ and driving a typical EIA-232-E load, the output voltage swing is $\pm 9\text{ V}$. Even under worst-case conditions the drivers are guaranteed to meet the $\pm 5\text{ V}$ EIA-232-E minimum requirement.

The input threshold levels are both TTL- and CMOS-compatible with the switching threshold set at $V_{CC}/4$. With a nominal $V_{CC} = 5\text{ V}$ the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal $400\text{ k}\Omega$ pull-up resistor pulls them high, forcing the outputs into a low state.

As required by the EIA-232-E standard, the slew rate is limited to less than $30\text{ V}/\mu\text{s}$ without the need for an external slew limiting capacitor and the output impedance in the power-off state is greater than $300\text{ }\Omega$.

Receiver Section

The receivers are inverting level shifters which accept EIA-232-E input levels ($\pm 5\text{ V}$ to $\pm 15\text{ V}$) and translate them into 5 V TTL/CMOS levels. The inputs have internal $5\text{ k}\Omega$ pull-down resistors to ground and are also protected against overvoltages of up to $\pm 30\text{ V}$. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the $\pm 3\text{ V}$ EIA-232-E requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

The receivers have Schmitt trigger inputs with a hysteresis level of 0.5 V . This ensures error-free reception for both noisy inputs and for inputs with slow transition times.

Shutdown (SD)

The ADM205, ADM206, ADM211, and ADM213 feature a control input which may be used to disable the part and reduce the power consumption to less than $5\text{ }\mu\text{W}$. This is very useful in battery operated systems. During shutdown the charge pump is turned off, the transmitters are disabled and all receivers except R4 and R5 on the ADM213 are put into a high-impedance disabled state. Receivers R4 and R5 on the ADM213 remain enabled during shutdown. This feature allows monitoring external activity such as ring indicator monitoring while the device is in a low power shutdown mode. The shutdown control input is active high on all parts except the ADM213 where it is active low. Refer to Tables II and III.

Enable Input

The ADM205, ADM209, ADM211, and ADM213 feature an enable input used to enable or disable the receiver outputs. The enable input is active low on the ADM205, ADM209, ADM211 and active-high on the ADM213. Refer to Tables II and III. When disabled, all receiver outputs are placed in a high impedance state. This function allows the outputs to be connected directly to a microprocessor data bus. It can also be used to allow receivers from different devices to share a common data line. The timing diagram for the enable function is shown in Figure 17.

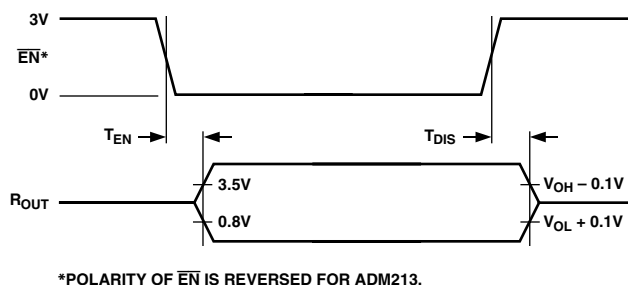


Figure 17. Enable Timing

APPLICATION HINTS

Driving Long Cables

In accordance with the EIA-232-E standard, long cables are permissible provided that the total load capacitance does not exceed 2500 pF . For longer cables which do exceed this, then it is possible to trade off baud rate vs. cable length. Large load capacitances cause a reduction in slew rate, and hence the maximum transmission baud rate is decreased. The ADM205–ADM211 and ADM213 are designed so that the slew rate reduction with increasing load capacitance is minimized.

For the receivers, it is important that a high level of noise immunity be inbuilt so that slow rise and fall times do not cause multiple output transitions as the signal passes slowly through the transition region. The ADM205–ADM211 and ADM213 have 0.5 V of hysteresis to guard against this. This ensures that, even in noisy environments, error-free reception can be achieved.

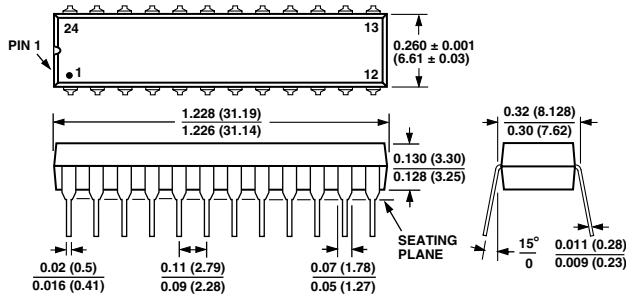
High Baud Rate Operation

The ADM205–ADM211 and ADM213 feature high slew rates permitting data transmission at rates well in excess of the EIA-232-E specification. The drivers maintain $\pm 5\text{ V}$ signal levels at data rates up to 120 kB/s under worst-case loading conditions.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

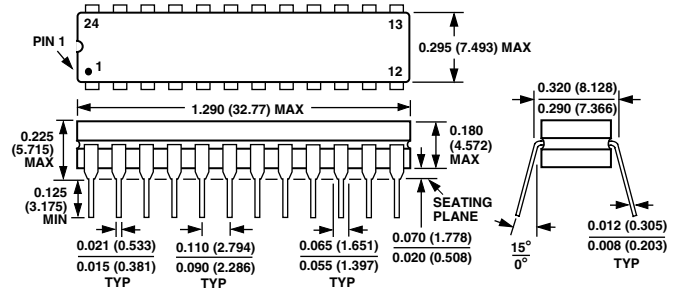
**24-Lead Plastic DIP
(N-24)**



NOTES

1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

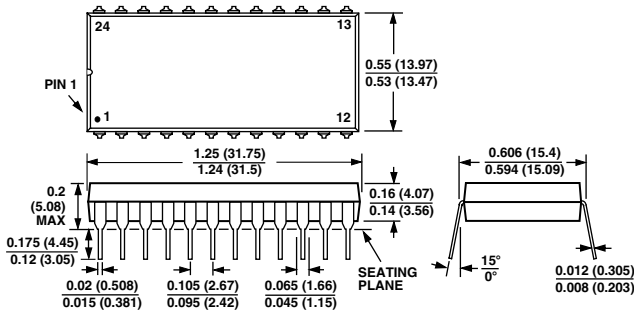
**24-Lead Cerdip
(Q-24)**



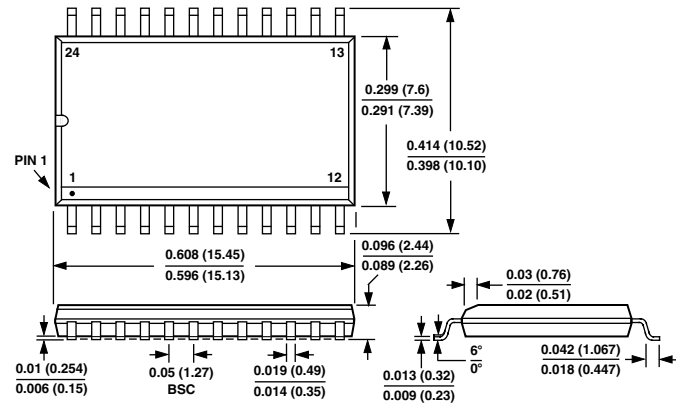
NOTES

1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

**24-Lead Plastic DIP
(N-24A)**



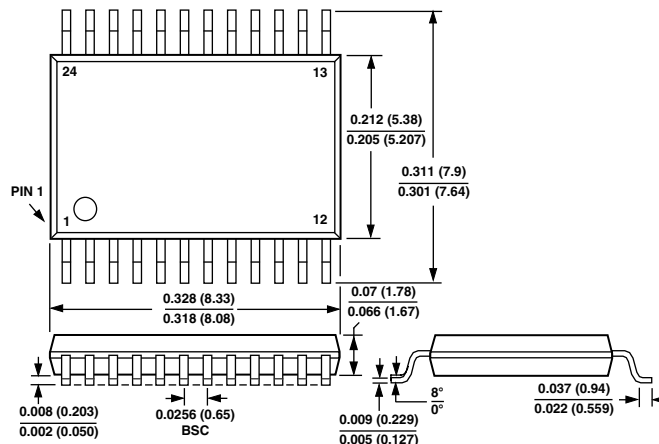
**24-Lead SOIC
(R-24)**



NOTES

1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

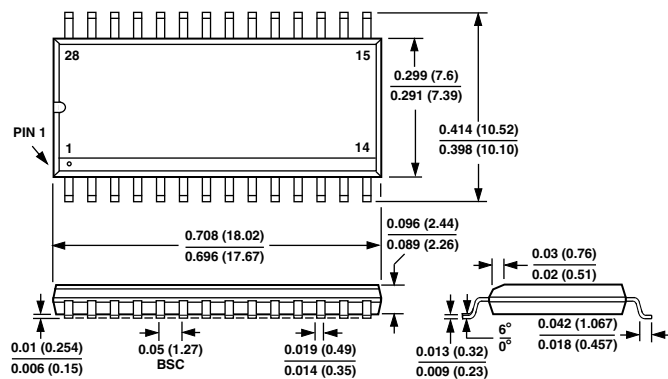
**24-Lead SSOP
(RS-24)**



NOTES

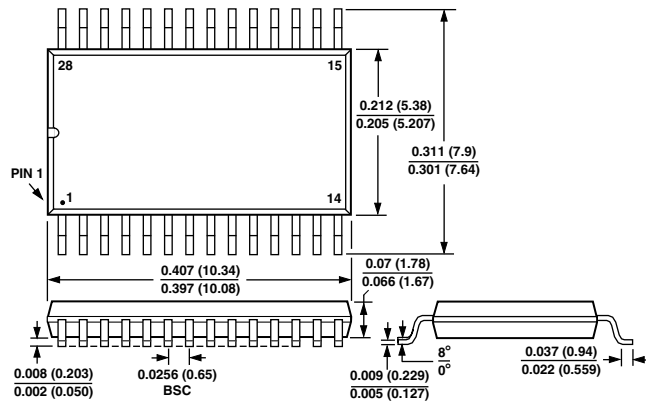
1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Lead SOIC
(R-28)



- NOTES
- 1. LEAD NO. 1 IDENTIFIED BY A DOT.
 - 2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Lead SSOP
(RS-28)



- NOTES
- 1. LEAD NO. 1 IDENTIFIED BY A DOT.
 - 2. LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

ADM205–ADM211/ADM213–Revision History

Location	Page
Data Sheet changed from REV. 0 to REV. A.	
Updated Figures.	
Changes to numbers in Min/Typ/Max column of Specification page	2