74HC251; 74HCT251

8-input multiplexer; 3-state
Rev. 7 — 14 March 2024

Product data sheet

1. General description

The 74HC251; 74HCT251 is an 8-bit multiplexer with eight binary inputs (I0 to I7), three select inputs (S0 to S2) and an output enable input (\overline{OE}). The select inputs select one of the eight binary inputs and route it to the complementary outputs (Y and \overline{Y}). A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- · Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC251: CMOS level
 - For 74HCT251: TTL level
- · Non-inverting data path
- ESD protection:
- HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

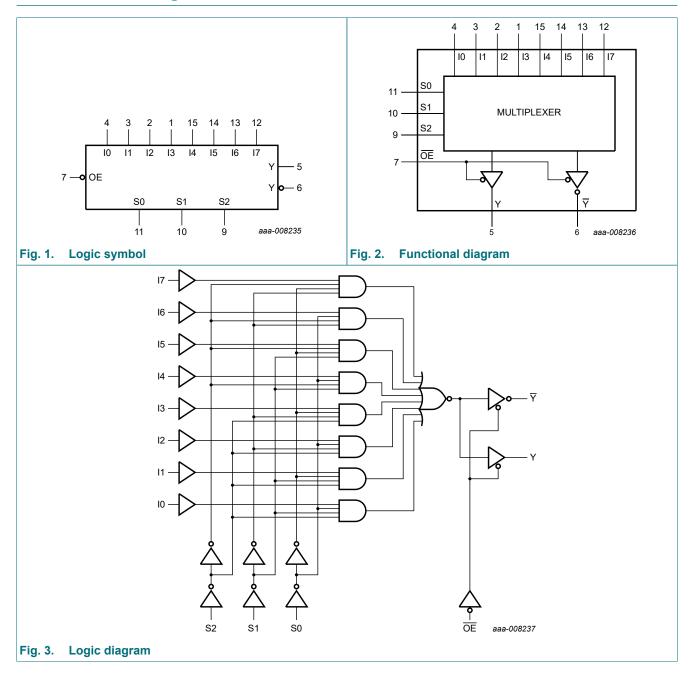
3. Ordering information

Table 1. Ordering information

Type number	Package	Package							
	Temperature range	Name	Description	Version					
74HC251D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads;	SOT109-1					
74HCT251D			body width 3.9 mm						
74HC251PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package;	SOT403-1					
74HCT251PW			16 leads; body width 4.4 mm						



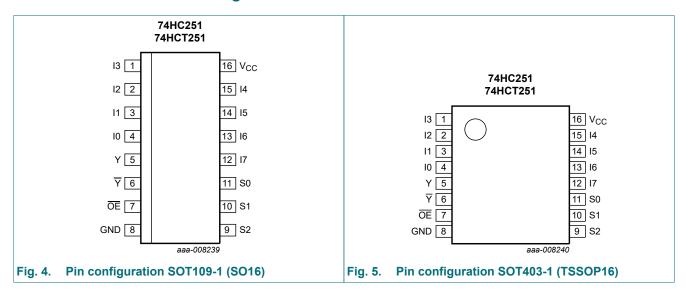
4. Functional diagram



2/16

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
10, 11, 12, 13, 14, 15, 16, 17	4, 3, 2, 1, 15, 14, 13, 12	data inputs
Υ	5	multiplexer output
₹	6	complementary multiplexer output
OE	7	output enable input (active LOW)
GND	8	ground (0 V)
S0, S1, S2	11, 10, 9	common data select inputs
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care; \ Z = high-impedance \ OFF-state.$

Input												Outp	ut
OE	S2	S1	S0	10	I1	12	13	14	15	16	17	Y	Y
Н	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Z	Z
L	L	L	L	L	Х	Х	Х	Х	Х	Х	Х	Н	L
L	L	L	L	Н	Х	Х	Х	Х	Х	Х	Х	L	Н
L	L	L	Н	Х	L	Х	Х	Х	Х	Х	Х	Н	L
L	L	L	Н	Х	Н	Х	Х	Х	Х	Х	Х	L	Н
L	L	Н	L	Х	Х	L	Х	Х	Х	Х	Х	Н	L
L	L	Н	L	Х	Х	Н	Х	Х	Х	Х	Х	L	Н
L	L	Н	Н	Х	Х	Х	L	Х	Х	Х	Х	Н	L
L	L	Н	Н	Х	X	Х	Н	Х	Х	Х	Х	L	Н
L	Н	L	L	Х	Х	Х	Х	L	Х	Х	Х	Н	L
L	Н	L	L	Х	Х	Х	Х	Н	Х	Х	Х	L	Н
L	Н	L	Н	Х	Х	Х	Х	Х	L	Х	Х	Н	L
L	Н	L	Н	Х	Х	Х	Х	Х	Н	Х	Х	L	Н
L	Н	Н	L	Х	Х	Х	Х	Х	Х	L	Х	Н	L
L	Н	Н	L	Х	Х	Х	Х	Х	Х	Н	Х	L	Н
L	Н	Н	Н	Х	Х	Х	Х	Х	Х	Х	L	Н	L
L	Н	Н	Н	Х	Х	Х	Х	Х	Х	Х	Н	L	Н

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	-	±20	mA
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$	-	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$ [1]	-	500	mW

^[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C. For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC251			74HCT251			
			Min	Тур	Max	Min	Тур	Max		
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V	
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V	
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V	
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C	
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V	
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V	
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V	

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min Typ Max		Min	Max	Min	Max		
74HC25	1									
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_{O} = -20 μ A; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_{O} = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
lı	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.5	-	±5.0	-	±10.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
Cı	input capacitance		-	3.5	-					pF
74HCT2	51								1	
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 V$								
	output voltage	Ι _Ο = 20 μΑ	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.5	-	±5.0	-	±10	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
ΔI _{CC}	additional supply current	$V_I = V_{CC} - 2.1 \text{ V};$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V; $I_O = 0 \text{ A}$								
		per input pin; In inputs	-	100	360	-	450	-	490	μΑ
		per input pin; OE input	-	150	540	-	675	-	735	μΑ
		per input pin; Sn input	-	150	540	-	675	-	735	μΑ
Cı	input capacitance		-	3.5	-					pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 9.

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC25	1			'	'	1		-		
t _{pd}	propagation	In to Y; see Fig. 6	1]							
	delay	V _{CC} = 2.0 V	-	50	170	-	215	-	255	ns
		V _{CC} = 4.5 V	-	18	34	-	43	-	51	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	29	-	37	-	43	ns
		In to \overline{Y} ; see Fig. 6	1]							
		V _{CC} = 2.0 V	-	55	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	16	30	-	37	-	45	ns
		Sn to Y; see Fig. 7	1]							
		V _{CC} = 2.0 V	-	66	205	-	255	-	310	ns
		V _{CC} = 4.5 V	-	24	41	-	51	-	62	ns
		V _{CC} = 5 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	19	35	-	43	-	53	ns
		Sn to \overline{Y} ; see Fig. 7	1]							
		V _{CC} = 2.0 V	-	69	205	-	255	-	310	ns
		V _{CC} = 4.5 V	-	25	41	-	51	-	62	ns
		V _{CC} = 5 V; C _L = 15 pF	-	21	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	20	35	-	43	-	53	ns
t _{en}	enable time	OE to Y, ∀; see Fig. 8	2]							
		V _{CC} = 2.0 V	-	36	140	-	175	-	210	ns
		V _{CC} = 4.5 V	-	13	28	-	35	-	42	ns
		V _{CC} = 6.0 V	-	10	24	-	30	-	36	ns
t _{dis}	disable time	OE to Y, Y; see Fig. 8	3]							
		V _{CC} = 2.0 V	-	39	140	-	170	-	210	ns
		V _{CC} = 4.5 V	-	14	28	-	35	-	42	ns
		V _{CC} = 6.0 V	-	11	24	-	30	-	36	ns
t _t	transition	Y, \overline{Y}; see Fig. 6	4]							
	time	V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	5] -	44	-	-	-	-	-	pF

Symbol	Parameter	Conditions			25 °C		-40 °C t	o +85 °C	-40 °C to	+125 °C	Unit
				Min	Тур	Max	Min	Max	Min	Max	
74HCT2	51										-
t _{pd}	propagation	In to Y; see Fig. 6	[1]								
	delay	V _{CC} = 4.5 V		-	22	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF		-	19	-	-	-	-	-	ns
		In to ∇; see Fig. 6	[1]								
		V _{CC} = 4.5 V		-	22	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF		-	19	-	-	-	-	-	ns
		Sn to Y; see Fig. 7	[1]								
		V _{CC} = 4.5 V		-	24	44	-	55	-	66	ns
		V _{CC} = 5 V; C _L = 15 pF		-	20	-	-	-	-	-	ns
		Sn to ₹; see Fig. 7	[1]								
		V _{CC} = 4.5 V		-	25	44	-	55	-	66	ns
		V _{CC} = 5 V; C _L = 15 pF		-	21	-	-	-	-	-	ns
t _{en}	enable time	OE to Y, Y; see Fig. 8	[2]								
		V _{CC} = 4.5 V		-	13	28	-	35	-	42	ns
		V _{CC} = 5 V; C _L = 15 pF		-	13	-	-	-	-	-	ns
t _{dis}	disable time	OE to Y, ∀; see Fig. 8	[3]								
		V _{CC} = 4.5 V		-	14	28	-	35	-	42	ns
		V _{CC} = 5 V; C _L = 15 pF		-	18	-	-	-	-	-	ns
t _t	transition	Y, ₹; see <u>Fig. 6</u>	[4]								
	time	V _{CC} = 4.5 V		-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} - 1.5 V	[5]	-	46	-	-	-	-	-	pF

- t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_{en} is the same as t_{PZH} and t_{PZL}.

- ten is the same as t_{PLZ} and t_{PLZ}.
 t_{dis} is the same as t_{PLZ} and t_{PHZ}.
 t_t is the same as t_{THL} and t_{TLH}.
 C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 P_D = C_{PD} × V_{CC}² × f_i × N + ∑(C_L × V_{CC}² × f_o) where:

 f_i = input frequency in MHz;

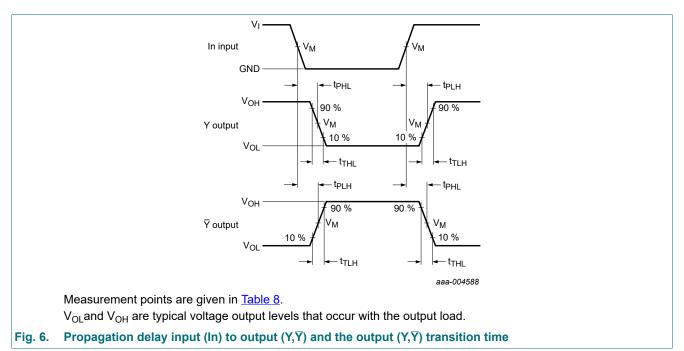
f_o = output frequency in MHz;

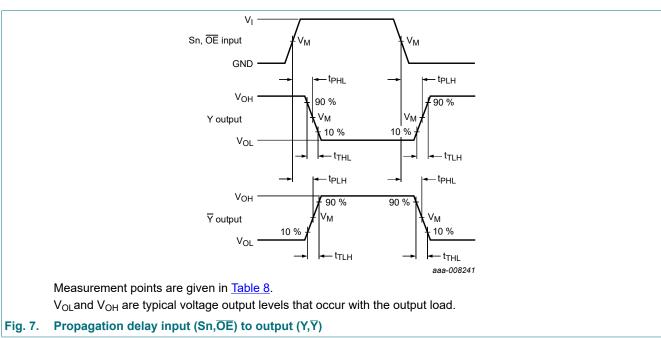
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching; $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

10.1. Waveforms and test circuit





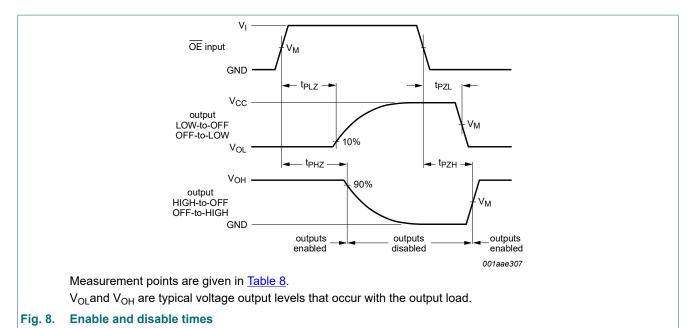
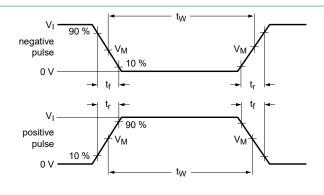
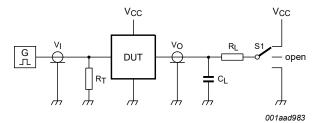


Table 8. Measurement points

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Туре	Input	Output
	V _M	V _M
74HC251	0.5V _{CC}	0.5V _{CC}
74HCT251	1.3 V	1.3 V





Test data is given in Table 9.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L= Load capacitance including jig and probe capacitance.

R_I = Load resistance.

S1 = Test selection switch.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Туре	Input		Load		S1 position		
	V _I	t _r , t _f	C _L	R_L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
74HC251	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}
74HCT251	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}

11. Package outline

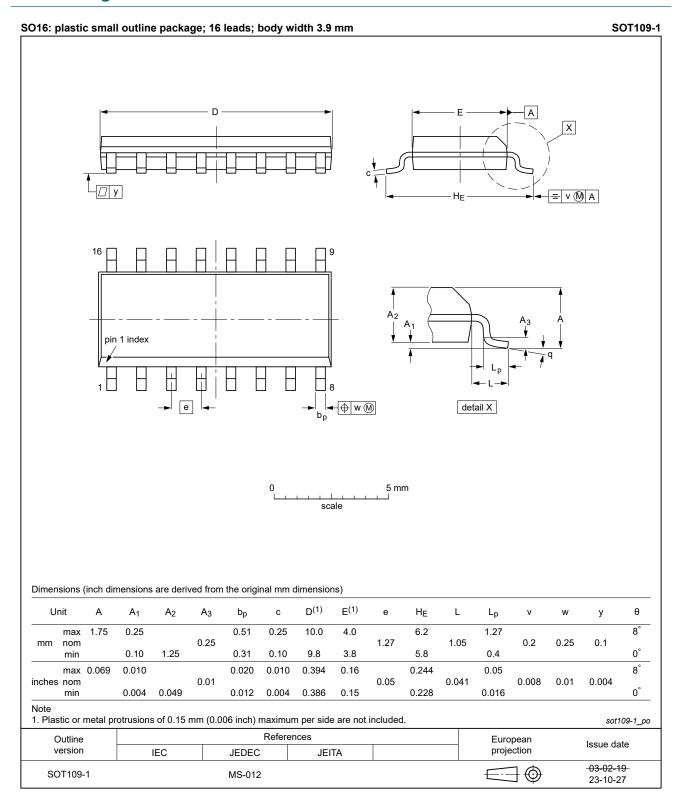


Fig. 10. Package outline SOT109-1 (SO16)

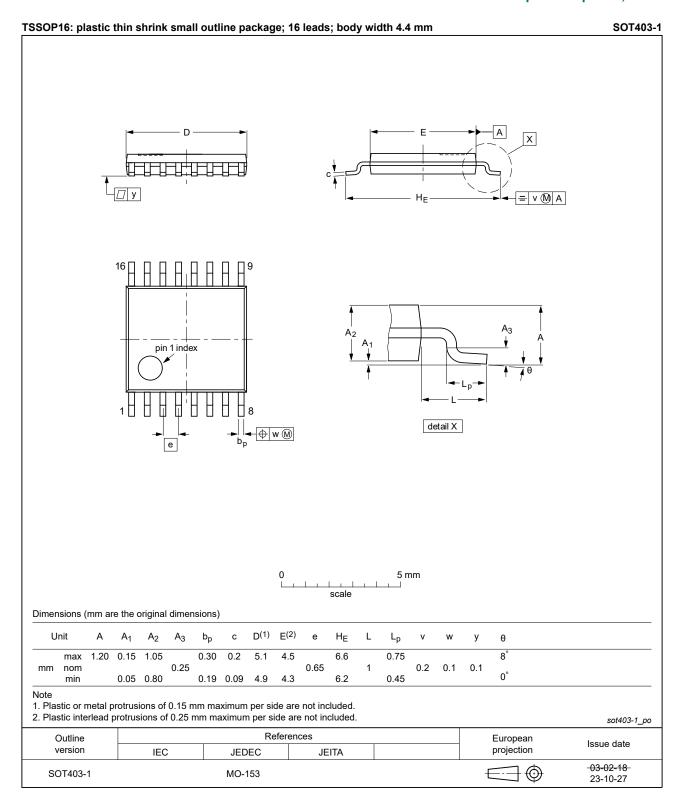


Fig. 11. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT251 v.7	20240314	Product data sheet	-	74HC_HCT251 v.6	
Modifications:	 Fig. 10, Fig. 11: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. Section 2: ESD specification updated according to the latest JEDEC standard. 				
74HC_HCT251 v.6	20210208	Product data sheet	-	74HC_HCT251 v.5	
Modifications:	 <u>Section 2</u> updated. Type numbers 74HC251DB and 74HCT251DB (SOT338-1 / SSOP16) removed. <u>Table 7</u>: Conditions for C_{PD} have changed for 74HCT251. (errata) 				
74HC_HCT251 v.5	20190715	Product data sheet	-	74HC_HCT251 v.4	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Table 4: Derating values for P_{tot} total power dissipation have changed. 				
74HC_HCT251 v.4	20160201	Product data sheet	-	74HC_HCT251 v.3	
Modifications:	Type numbers 74HC251N and 74HCT251N (SOT38-4) removed.				
74HC_HCT251 v.3	20130709	Product data sheet	-	74HC_HCT251_CNV v.2	
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 				
74HC HCT251 CNV v.2	19970828	Product specification	_		

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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