NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL78206

ISL78205

2.5A Buck Controller with Integrated High-Side MOSFET

FN7926
Rev 3.00
February 19, 2014

The ISL78205 is a synchronous buck controller with a 90mΩ high side MOSFET and low side driver integrated. The ISL78205 supports a wide input voltage range from 3V to 40V. Regarding the output current capability under thermal considerations, the ISL78205 can typically support a continuous load of 2.5A under such conditions of 5V V_{OUT}, V_{IN} range of 8V to 30V, 500kHz, +85°C ambient temperature with still air. For any specific application, the actual maximum output current depends upon the die temperature not exceeding +125°C (or certain maximum temperature acceptable for the customer) with the power dissipated in the IC, which is related to input voltage, output voltage, duty cycle, switching frequency, ambient temperature and board layout, etc. Refer to “Output Current” on page 12 for more details.

The ISL78205 offers the most robust current protections. It uses peak current mode control with cycle-by-cycle current limiting. It is implemented with frequency foldback under current limit conditions. In addition, the hiccup overcurrent mode is also implemented to guarantee reliable operations under harsh short conditions.

The ISL78205 has comprehensive protections against various faults, including overvoltage and over-temperature protections, etc.

Features

- Ultra wide input voltage range 3V to 40V (refer to “Input Voltage” on page 12 for more details)
- Less than 3µA Shut down input current (IC disabled)
- Temperature range -40°C to +105°C
- Integrated 90mΩ high-side MOSFET
- Operational topologies
  - Synchronous buck
  - Non-synchronous buck
- Programmable frequency from 200kHz to 2.2MHz and frequency synchronization capability
- ±1% tight voltage regulation accuracy
- Reliable cycle-by-cycle overcurrent protection
  - Temperature compensated current sense
  - Frequency foldback
  - Programmable OC limit
  - Hiccup mode protection in worst case short condition
- 20 Ld HTSSOP package
- AEC-Q100 Qualified
- Pb-Free (RoHS Compliant)

Applications

- Automotive applications
- General purpose power regulator
- 24V bus power
- Battery power
- Embedded processor and I/O supplies

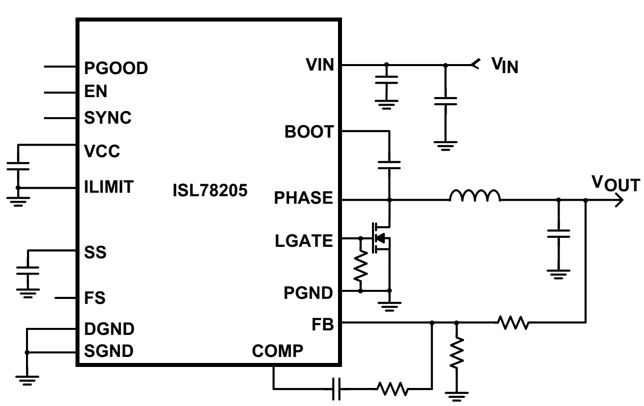


FIGURE 1. TYPICAL APPLICATION SCHEMATIC I - SYNCHRONOUS BUCK

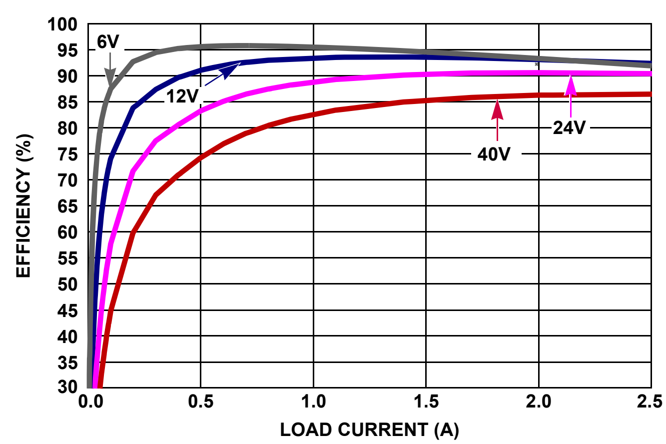
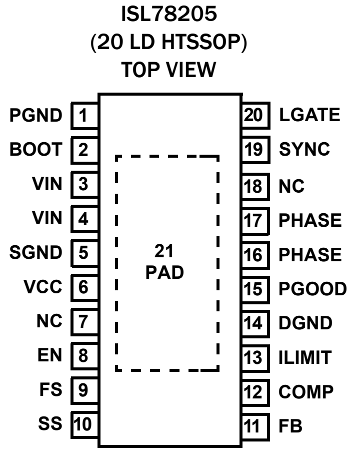


FIGURE 2. EFFICIENCY, SYNCHRONOUS BUCK, 500kHz, V_{OUT} 5V, T_A = +25°C

Pin Configuration



Functional Pin Description

PIN NAME	PIN #	DESCRIPTION
PGND	1	This pin is used as the ground connection of the power flow, including the driver.
BOOT	2	This pin provides bias voltage to the high-side MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive the internal N-channel MOSFET. The boot charge circuitries are integrated inside of the IC. No external boot diode is needed. A 1µF ceramic capacitor is recommended to be used between the BOOT and PHASE pin.
VIN	3, 4	Connect the input rail to these pins that are connected to the drain of the integrated high-side MOSFET, as well as the source for the internal linear regulator that provides the bias of the IC. With the part switching, the operating input voltage applied to the VIN pins must be under 40V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to switching while not exceeding Absolute Maximum Ratings.
SGND	5	This pin provides the return path for the control and monitor portions of the IC.
VCC	6	This pin is the output of the internal linear regulator that supplies the bias for the IC, including the driver. A minimum 4.7µF decoupling ceramic capacitor is recommended between VCC to ground.
EN	8	The controller is enabled when this pin is pulled HIGH or left floating. The IC is disabled when this pin is pulled LOW. Range: 0V to 5.5V.
FS	9	Tying this pin to VCC, or GND, or leaving it open will force the IC to have 500kHz switching frequency. The oscillator switching frequency can also be programmed by adjusting the resistor from this pin to GND.
SS	10	Connect a capacitor from this pin to ground. This capacitor, along with an internal 5µA current source, sets the soft-start interval of the converter. Also, this pin can be used to track a ramp on this pin.
FB	11	This pin is the inverting input of the voltage feedback error amplifier. With a properly selected resistor divider connected from V_{OUT} to FB, the output voltage can be set to any voltage between the input rail (reduced by maximum duty cycle and voltage drop) and the 0.8V reference. Loop compensation is achieved by connecting an RC network across COMP and FB. The FB pin is also monitored for overvoltage events.
COMP	12	Output of the voltage feedback error amplifier.
ILIMIT	13	Programmable current limit pin. With this pin connected to VCC pin, or to GND, or left open, the current limit threshold is set to a default of 3.6A; the current limit threshold can be programmed with a resistor from this pin to GND.
DGND	14	Digital ground pin. Connect to SGND at quiet ground copper plane.
PGOOD	15	PGOOD is an open drain output. Pull up this pin with a resistor to VCC. PGOOD pin will be pulled low immediately in the event that the output is out of regulation (OV or UV) or the EN pin is pulled low. PGOOD is equipped with a fixed delay of 1000 cycles upon output power-up (V_O > 90%).
PHASE	16, 17	These pins are the PHASE nodes that should be connected to the output inductor. These pins are connected to the source of the high side N-channel MOSFET.
SYNC	19	This pin can be used to synchronize two or more ISL78205 controllers. Multiple ISL78205s can be synchronized with their SYNC pins connected together. 180 degree phase shift is automatically generated between the master and slave ICs. The internal oscillator can also lock to an external frequency source applied to this pin with square pulse waveform (with frequency 10% higher than the IC's local frequency, and pulse width higher than 150ns). This pin should be left floating if not used.

Functional Pin Description (Continued)

PIN NAME	PIN #	DESCRIPTION
LGATE	20	In synchronous buck mode, this pin is used to drive the lower side MOSFET to improve efficiency. A 5.1k or smaller value resistor has to be added to connect LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise. In non-synchronous buck when a diode is used as the bottom side power device, this pin should be connected to VCC through a resistor (less than 5k) before VCC start-up to disable the low side driver (LGATE).
NC	7, 18	No connection pin. Connect these pins to SGND at quiet ground copper plane.
PAD	21	Bottom thermal pad. It is not connected to any electrical potential of the IC. In layout, it must be connected to PCB ground copper plane with area as large as possible to effectively reduce the thermal impedance.

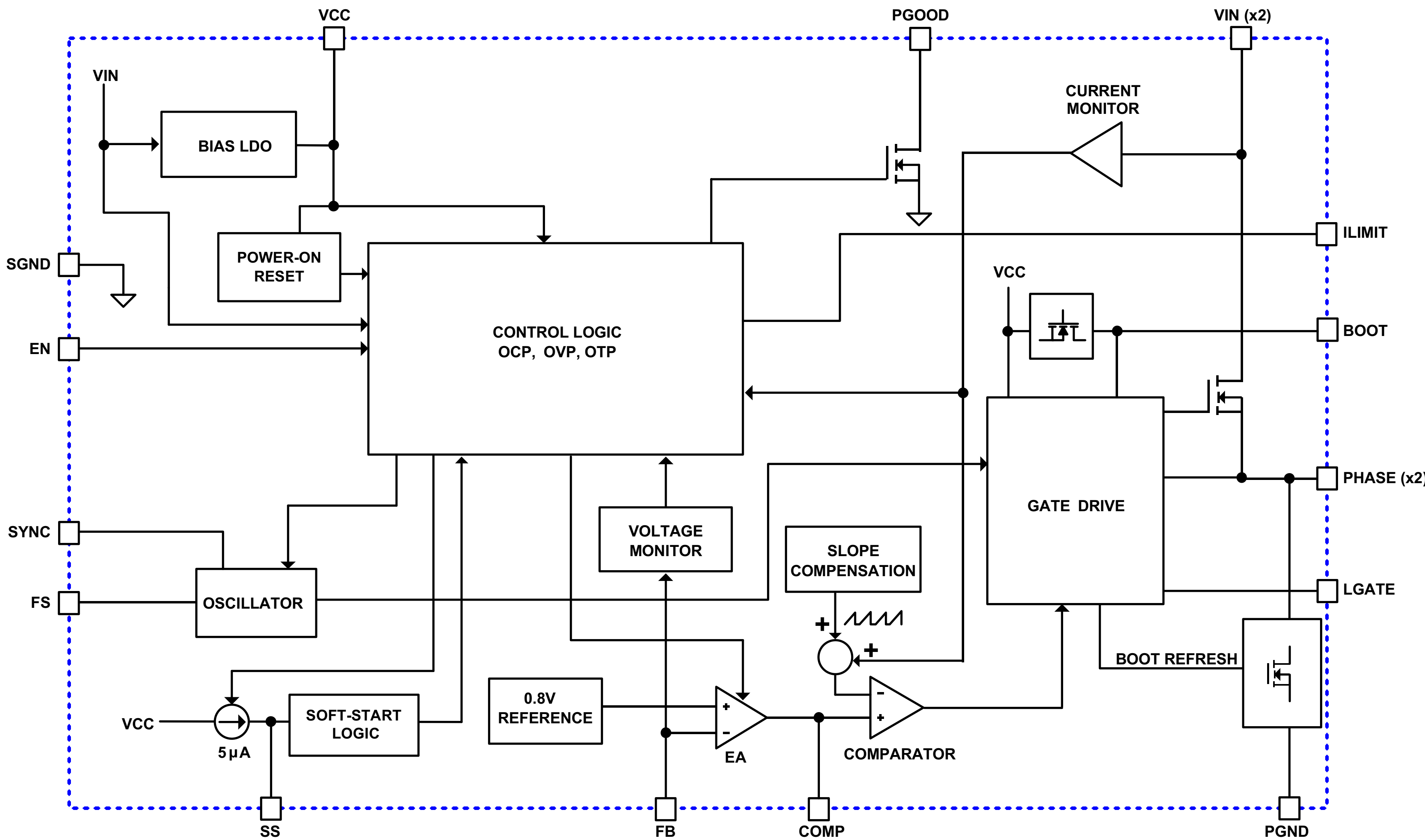
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL78205AVEZ	78205 AVEZ	-40 to +105	20 Ld HTSSOP	M20.173A
ISL78205EVAL1Z	Evaluation Board			
ISL78205EVAL2Z	Evaluation Board			

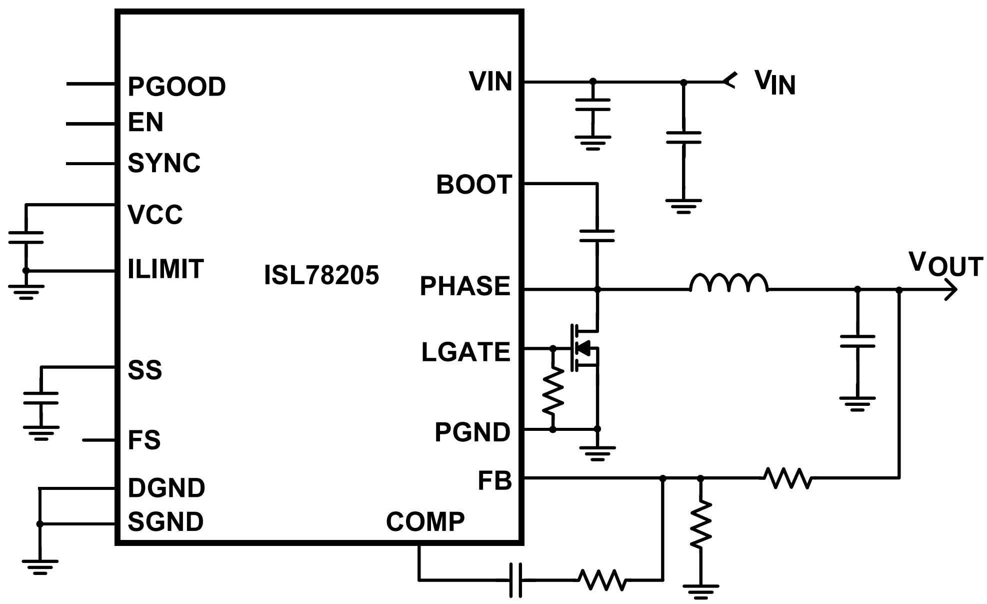
NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78205. For more information on MSL please see techbrief TB363.

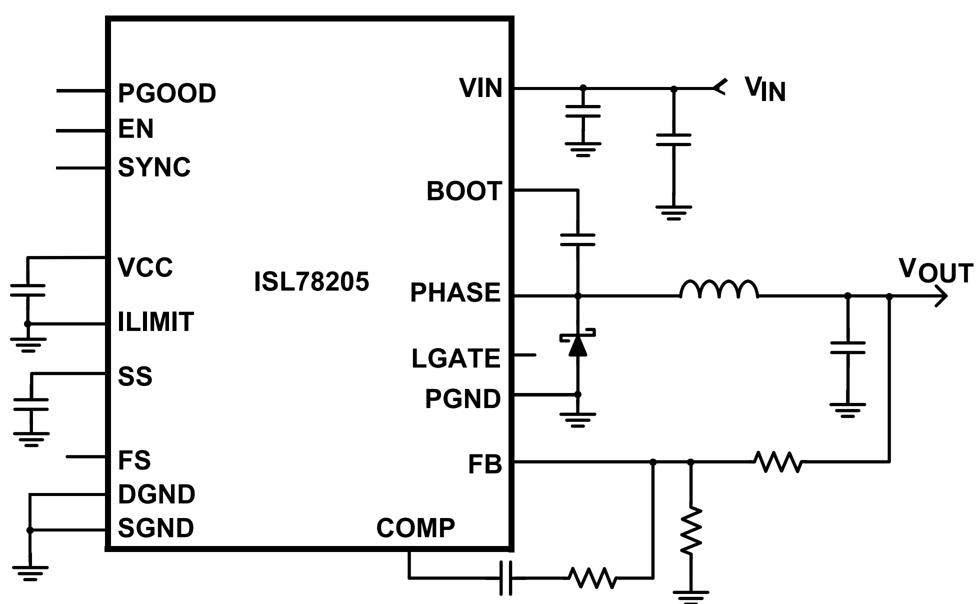
Block Diagram



Typical Application Schematic I - Synchronous Buck



Typical Application Schematic II - Non-Synchronous Buck



Absolute Maximum Ratings

VIN, PHASE .... GND - 0.3V to +44V
VCC.. GND - 0.3V to +6.0V
Absolute Boot Voltage, V_{BOOT}.............................. +50.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PHASE}.................. +6.0V
All Other Pins .... GND - 0.3V to VCC + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114F)..............2000V
Machine Model (Tested per JESD22-A115C) 250V
Charged Device Model (Tested per JESD22-C101E)............1000V
Latch Up Rating (Tested per JESD78B; Class II, Level A)......... 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld HTSSOP Package (Notes 4, 5)	32	3.5

Maximum Junction Temperature (Plastic Package) .... +150°C
Maximum Storage Temperature Range................ -65°C to +150°C
Pb-Free Reflow Profile .... see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage on VIN .... 3V to 40V
Ambient Temperature Range (Automotive).............-40°C to +105°C
Junction Temperature Range ....-40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Refer to "Block Diagram" on page 4 and Typical Application Schematics on page 5. Operating Conditions Unless Otherwise Noted: V_{IN} = 12V, or V_{CC} = 4.5V, T_A = -40°C to +105°C. Typical are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{IN} SUPPLY						
V_{IN} Voltage Range		V_{IN}	**3.05**		**40**	V
		V_{IN} connected to VCC	**3.05**		**5.5**	V
Operating Supply Current	I_Q	IC Operating, Not Including Driving Current, V_{IN} = 12V		1.2		mA
Shut Down Supply Current	I_{IN_SD}	EN connected to GND, V_{IN} = 12V		1.8	**3**	µA
INTERNAL MAIN LINEAR REGULATOR						
MAIN LDO V_{CC} Voltage	V_{CC}	V_{IN} > 5V	**4.2**	4.5	**4.8**	V
MAIN LDO Dropout Voltage	$V_{DROPOUT\_MAIN}$	V_{IN} = 4.2V, I_{VCC} = 35mA		0.3	**0.5**	V
		V_{IN} = 3V, I_{VCC} = 25mA		0.25	**0.3**	V
V_{CC} CURRENT LIMIT of MAIN LDO				60		mA
POWER-ON RESET						
Rising V_{CC} POR Threshold	V_{PORH_RISE}		**2.82**	2.9	**3.05**	V
Falling V_{CC} POR Threshold	V_{PORL_FALL}			2.6	**2.8**	V
V_{CC} POR Hysteresis	V_{PORL_HYS}			0.3		V
ENABLE						
Required Enable On Voltage	V_{ENH}		**2**			V
Required Enable Off voltage	V_{ENL}				**0.8**	V
EN Pull-Up Current	I_{EN_PULLUP}	V_{IN} = 24V		0.8		µA
		V_{IN} = 12V		0.5		µA
		V_{IN} = 5V		0.25		µA

Electrical Specifications Refer to "Block Diagram" on page 4 and Typical Application Schematics on page 5. Operating Conditions Unless Otherwise Noted: V_{IN} = 12V, or V_{CC} = 4.5V, T_A = -40°C to +105°C. Typical are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
OSCILLATOR						
PWM Frequency	f_{OSC}	R_T = 665kΩ	**160**	200	**240**	kHz
		R_T = 51.1kΩ	**1950**	2200	**2450**	kHz
		FS Pin connected to VCC or Floating or GND	**450**	500	**550**	kHz
MIN ON Time	t_{MIN_ON}			130	**225**	ns
MIN OFF Time	t_{MIN_OFF}			210	**325**	ns
SYNCHRONIZATION						
Input High Threshold	V_{IH}			2		V
Input Low Threshold	V_{IL}			0.5		V
Input Minimum Pulse Width				25		ns
Input Impedance				100		kΩ
Input Minimum Frequency Divided by Free Running Frequency				1.1		
Input Maximum Frequency Divided by Free Running Frequency				1.6		
Output Pulse Width		C_{SYNC} = 100pF		100		ns
Output Pulse High	V_{OH}	R_{LOAD} = 1kΩ		V_{CC}-0.25		V
Output Pulse Low	V_{OL}			GND		V
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}			0.8		V
System Accuracy			**-1.0**		**1.0**	%
FB Pin Source Current				5		nA
SOFT-START						
Soft-Start Current	I_{SS}		**3**	5	**7**	µA
ERROR AMPLIFIER						
Unity Gain-Bandwidth		C_{LOAD} = 50pF		10		MHz
DC Gain		C_{LOAD} = 50pF		88		dB
Maximum Output Voltage				3.6		V
Minimum Output Voltage				0.5		V
Slew Rate	SR	C_{LOAD} = 50pF		5		V/µs
INTERNAL HIGH-SIDE MOSFET						
Upper MOSFET $r_{DS(ON)}$	$r_{DS(ON)\_UP}$	Note 6		90	**150**	mΩ
LOW-SIDE MOSFET GATE DRIVER						
LGate Source Resistance		100mA Source Current		3.5		Ω
LGATE Sink Resistance		100mA Sink Current		3.3		Ω
POWER GOOD MONITOR						
Overvoltage Rising Trip Point	V_{FB}/V_{REF}	Percentage of Reference Point	**104**	110	**116**	%
Overvoltage Rising Hysteresis	V_{FB}/V_{OVTRIP}	Percentage Below OV Trip Point		3		%

Electrical Specifications Refer to "Block Diagram" on page 4 and Typical Application Schematics on page 5. Operating Conditions Unless Otherwise Noted: V_{IN} = 12V, or V_{CC} = 4.5V, T_A = -40°C to +105°C. Typical are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Undervoltage Falling Trip Point	V_{FB}/V_{REF}	Percentage of Reference Point	**84**	90	**96**	%
Undervoltage Falling Hysteresis	V_{FB}/V_{UVTRIP}	Percentage Above UV Trip Point		3		%
PGOOD Rising Delay	t_{PGOOD_DELAY}	f_{OSC} = 500kHz		2		ms
PGOOD Leakage Current		PGOOD HIGH, V_{PGOOD} = 4.5V		10		nA
PGOOD Low Voltage	V_{PGOOD}	PGOOD LOW, I_{PGOOD} = 0.2mA		0.10		V
OVERCURRENT PROTECTION						
Default Cycle by Cycle Current Limit Threshold	I_{OC_1}	ILIMIT = GND or VCC or Floating	**3**	3.6	**4.2**	A
Hiccup Current Limit Threshold	I_{OC_2}	Hiccup, I_{OC_2}/I_{OC_1}		115		%
OVERVOLTAGE PROTECTION						
OV Latching-off Trip Point		Percentage of Reference Point LG = UG = LATCH LOW		120		%
OV Non-Latching-off Trip Point		Percentage of Reference Point LG = UG = LOW		110		%
OV Non-Latching-off Release Point		Percentage of Reference Point		102.5		%
OVER TEMPERATURE PROTECTION						
Over-Temperature Trip Point				155		°C
Over-Temperature Recovery Threshold				140		°C

NOTES:

6. Wire bonds not included. The wire bond resistance between VIN and PHASE pin is 32mΩ typical.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

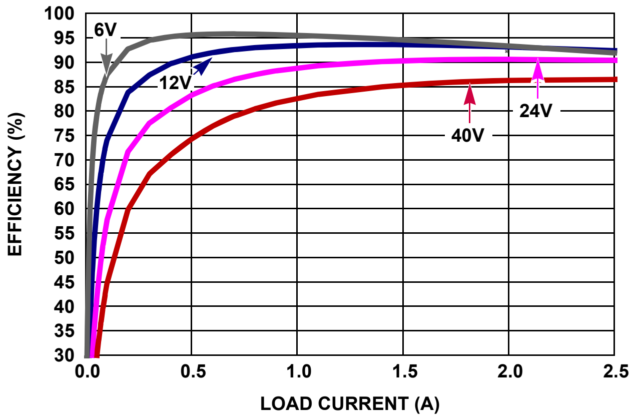


FIGURE 3. EFFICIENCY, SYNCHRONOUS BUCK, 500kHz, V_{OUT} 5V, T_A = +25°C

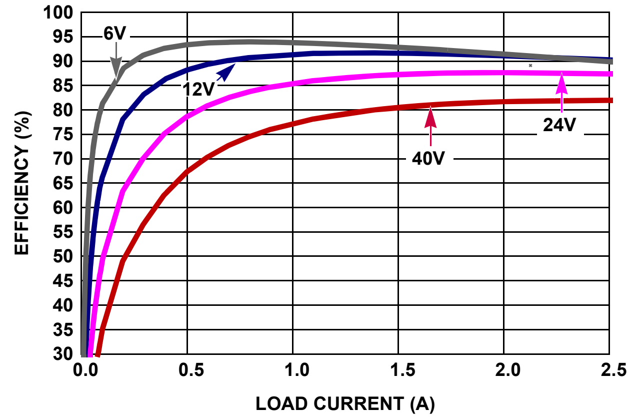


FIGURE 4. EFFICIENCY, SYNCHRONOUS BUCK, 500kHz, V_{OUT} 3.3V, T_A = +25°C

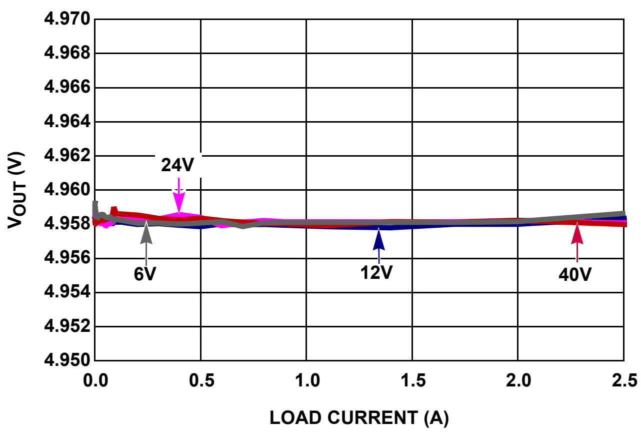


FIGURE 5. LOAD REGULATION, V_{OUT} 5V, T_A = +25°C

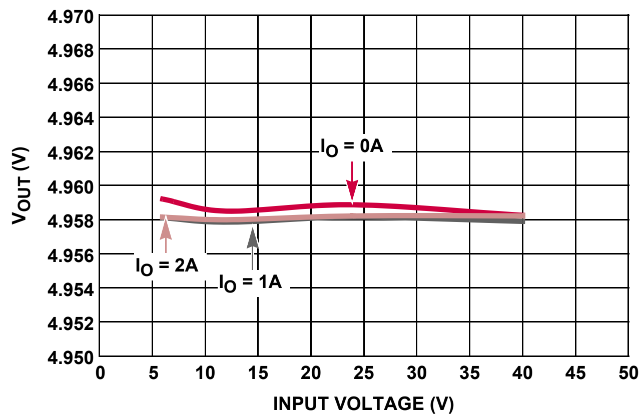


FIGURE 6. LINE REGULATION, V_{OUT} 5V, T_A = +25°C

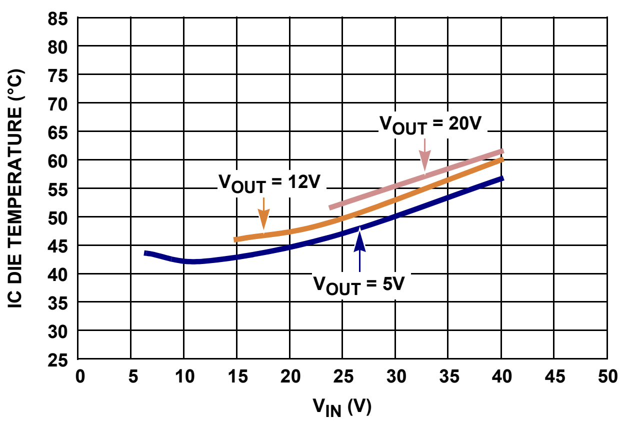


FIGURE 7. IC DIE TEMPERATURE UNDER +25°C AMBIENT TEMPERATURE, STILL AIR, 500kHz, I_O = 2A

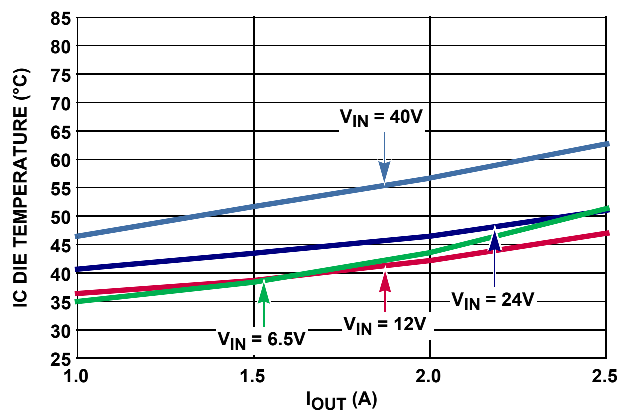


FIGURE 8. IC DIE TEMPERATURE UNDER +25°C AMBIENT TEMPERATURE, STILL AIR, 500kHz, V_{OUT} = 5V

Typical Performance Curves (Continued)

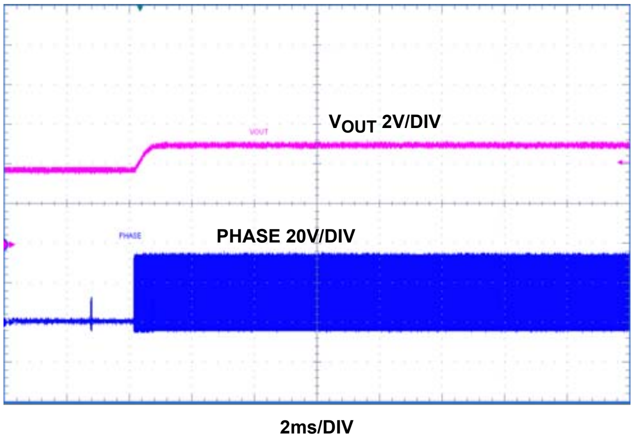


FIGURE 9. V_{IN} 36V, PRE-BIASED START-UP

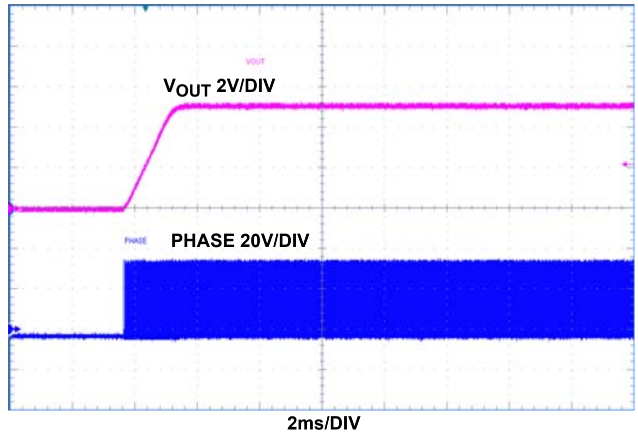


FIGURE 10. SYNCHRONOUS BUCK MODE, V_{IN} 36V, I_O 2A, ENABLE ON

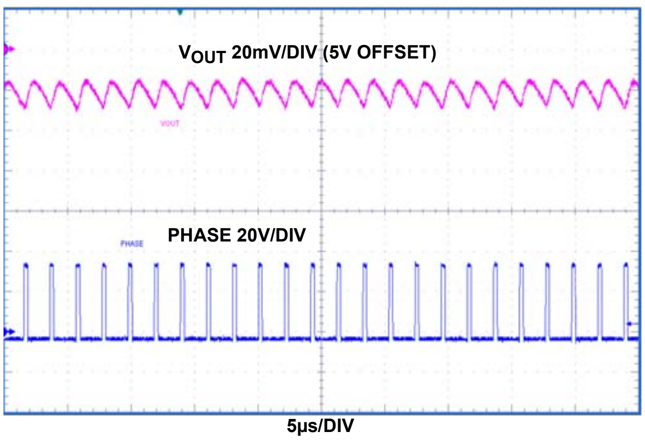


FIGURE 11. SYNCHRONOUS BUCK, V_{IN} 36V, I_O 2A

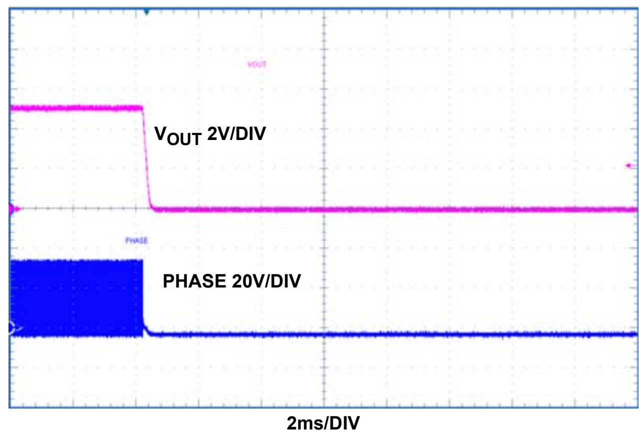


FIGURE 12. SYNCHRONOUS BUCK MODE, V_{IN} 36V, I_O 2A, ENABLE OFF

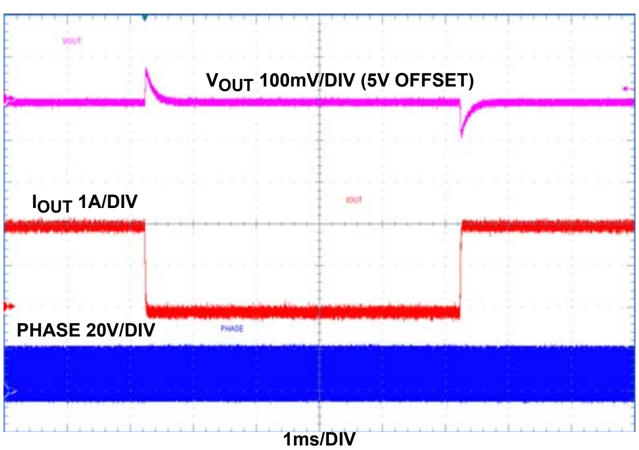


FIGURE 13. V_{IN} 24V, 0A TO 2A STEP LOAD

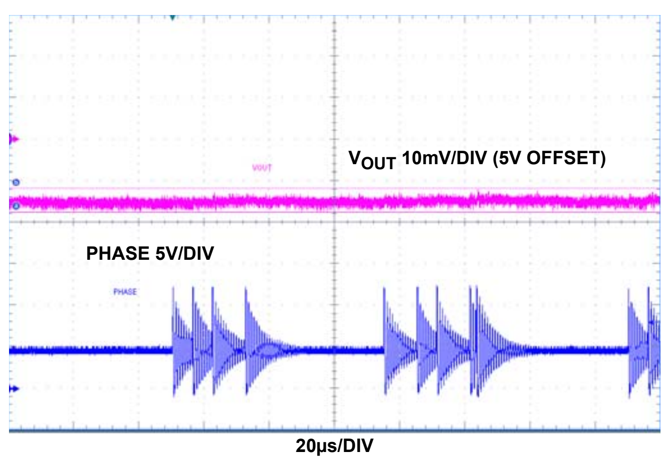


FIGURE 14. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, V_{IN} 12V, NO LOAD

Typical Performance Curves (Continued)

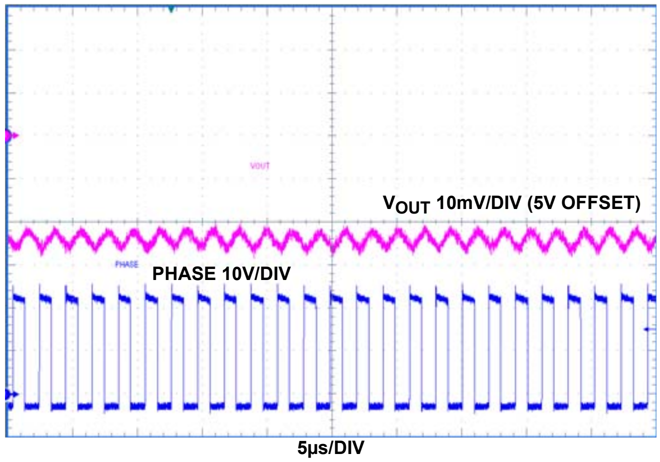


FIGURE 15. NON-SYNCHRONOUS BUCK, FORCE PWM MODE, V_{IN} 12V, 2A

Functional Description

Initialization

Initially, the ISL78205 continually monitors the voltage at the EN pin. When the voltage on the EN pin exceeds its rising threshold, the internal LDO will start-up to build up VCC. After Power-On Reset (POR) circuits detect that the VCC voltage has exceeded the POR threshold, the soft-start will be initiated.

Soft-Start

The soft-start (SS) ramp is built up in the external capacitor on the SS pin that is charged by an internal 5µA current source.

$$C_{SS}[\mu F] = 6.5 \cdot t_{SS}[S] \tag{EQ. 1}$$

The SS ramp starts from 0 to voltage above 0.8V. Once SS reaches 0.8V, the bandgap reference takes over and IC gets into steady state operation. The soft-start time is referring to the duration for SS pin ramps from 0 to 0.8V while output voltage ramps up with the same rate from 0 to target regulated voltage. The required capacitance at SS pin can be calculated from Equation 1.

The SS plays a vital role in the hiccup mode of operation. The IC works as cycle-by-cycle peak current limiting at over load condition. When a harsh condition occurs and the current in the upper side MOSFET reaches the second overcurrent threshold, the SS pin is pulled to ground and a dummy soft-start cycle is initiated. At dummy SS cycle, the current to charge the soft-start cap is cut down to 1/5 of its normal value. Therefore, a dummy SS cycle takes 5 times that of the regular SS cycle. During the dummy SS period, the control loop is disabled and there is no PWM output. At the end of this cycle, it will start the normal SS. The hiccup mode persists until the second overcurrent threshold is no longer reached.

The ISL78205 is capable of starting up with pre-biased output.

PWM Control

The ISL78205 employs the peak current mode PWM control for fast transient response and cycle-by-cycle current limiting. See the "Block Diagram" on page 4.

The PWM operation is initialized by the clock from the oscillator. The upper MOSFET is turned on by the clock at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current sense signal and the slope compensation signal reaches the error amplifier output voltage level, the PWM comparator is triggered to shut down the PWM logic to turn off the high side MOSFET. The high side MOSFET stays off until the next clock signal starts.

The output voltage is sensed by a resistor divider from V_{OUT} to FB pin. The difference between the FB voltage and 0.8V reference is amplified and compensated to generate the error voltage signal at the COMP pin. Then the COMP pin signal is compared with the current ramp signal to shut down the PWM.

Synchronous and Non-Synchronous Buck

The ISL78205 supports both synchronous and non-synchronous buck operations. For a non-synchronous buck operation when a power diode is used as the low side power device, the LGATE driver can be disabled with LGATE connected to VCC (before IC start-up). In non-synchronous buck application, the phase node will show oscillations after high-side turns off (as shown in Figure 14 blue curve). This is normal due to the oscillations among the parasitic capacitors at phase node and output inductor. A RC snubber (suggesting 200ohm and 2.2nF as typical) at phase node can reduce this ringing. The PGOOD signal could falsely dip due to this ringing. In application when PGOOD function is used, this snubber is highly recommended.

Input Voltage

With the part switching, the operating input voltage applied to the VIN pins must be under 40V. This recommendation allows for short voltage ringing spikes (within a couple of ns time range) due to switching while not exceeding Absolute Maximum Ratings.

The lowest IC operating input voltage (VIN pin) depends on VCC voltage and the Rising and Falling V_{CC} POR Threshold in the Electrical Specifications table on page 6. At IC startup, when VCC is just over the rising POR threshold, there is no switching yet before the soft-start starts. Therefore, the IC minimum start-up voltage on VIN pin is 3.05V (MAX of Rising V_{CC} POR). When the soft-start is initiated, the regulator is switching and the dropout voltage across the internal LDO increases due to driving current. Thus the IC VIN pin shutdown voltage is related to driving current and VCC POR falling threshold. The internal upper side MOSFET has typical 10nC gate drive. For a typical example of synchronous buck with 4nC lower MOSFET gate drive and 500kHz switching frequency, the driving current is 7mA total causing 70mV drop across internal LDO under 3V V_{IN}. Then the IC shutdown voltage on the VIN pin is 2.87V (2.8V + 0.07V). In practical design, extra room should be taken into account with concerns of voltage spikes at V_{IN}.

Output Voltage

The ISL78205 output voltage can be programmed down to 0.8V by a resistor divider from V_{OUT} to FB. The maximum achievable voltage is (V_{IN}*D_{MAX} - V_{DROP}), where V_{DROP} is the voltage drop in the power path, including mainly the MOSFET $r_{DS(ON)}$ and inductor DCR. The maximum duty cycle D_{MAX} is decided by (1 - Fs * $t_{MIN(OFF)}$).

Output Current

With the high side MOSFET integrated, the maximum current that the ISL78205 can support is decided by the package and many operating conditions, including input voltage, output voltage, duty cycle, switching frequency and temperature, etc.

First, The maximum output current is limited by the maximum OC threshold that is 4.18A (TYP).

Second, from the thermal perspective, the die temperature shouldn't be above +125°C with the power loss dissipated inside of the IC. Figures 7 and 8 show the thermal performance of this part operating at different conditions. Figure 7 shows 2A applications under +25°C still air conditions. Different V_{OUT} (5V, 12V, 20V) applications thermal data are shown over V_{IN} range at +25°C and still air. The temperature rise data in Figure 7 can be used to estimate the die temperature at different ambient temperatures under various operating conditions. Note that more temperature rise is expected at higher ambient temperature due to more conduction loss caused by $r_{DS(ON)}$ increase.

Figure 8 shows 5V output applications' thermal performance under various output current and input voltage. It shows the temperature rise trend with load and V_{IN} changes. The part can output 2.5A under typical application conditions (V_{IN} 8~30V, V_{OUT} 5V, 500kHz, still air and +85°C ambient conditions). The output current should be derated under any conditions, causing the die temperature to exceed +125°C.

Basically, the die temperature is equal to the sum of the ambient temperature and the temperature rise resulting from the power dissipated from the IC package with a certain junction to ambient thermal impedance θ_{JA}. The power dissipated in the IC is related to the MOSFET switching loss, conduction loss and the internal LDO loss. Besides the load, these losses are also related to input voltage, output voltage, duty cycle, switching frequency and temperature. With the exposed pad at the bottom, the heat of the IC mainly goes through the bottom pad and θ_{JA} is greatly reduced. The θ_{JA} is highly related to layout and air flow conditions. In layout, multiple vias (20 recommended) are strongly recommended in the IC bottom pad. In addition, the bottom pad with its vias should be placed in the ground copper plane with an area as large as possible connected through multiple layers. The θ_{JA} can be reduced further with air flow. For applications with high output current and bad operating conditions (compact board size, high ambient temperature, etc.), synchronous buck is highly recommended since the external low-side MOSFET generates smaller heat than external low-side power diode. This helps to reduce PCB temperature rise around the ISL78205 and accordingly less junction temperature of ISL78205.

Oscillator and Synchronization

The oscillator has a default frequency of 500kHz with the FS pin connected to VCC, or ground, or floating. The frequency can be programmed to any frequency between 200kHz and 2.2MHz with a resistor from the FS pin to GND.

$$R_{FS}[k\Omega] = \frac{145000 - 16 \cdot FS[kHz]}{FS[kHz]} \quad \text{(EQ. 2)}$$

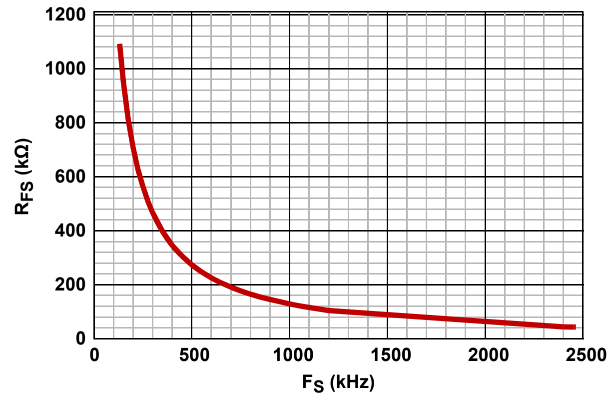


FIGURE 16. R_{FS} vs FREQUENCY

The SYNC pin is bi-directional and it outputs the IC's default or programmed local clock signal when it's free running. The IC locks to an external clock injected to SYNC pin (external clock frequency recommended to be 10% higher than the free running frequency). The delay from the rising edge of the external clock signal to the PHASE rising edge is half of the free running switching period pulse 220ns, (0.5Tsw +220ns). The maximum external clock frequency is recommended to be 1.6 of the free running frequency.

With the SYNC pins simply connected together, multiple ISL78205s can be synchronized. The slave ICs automatically have a 180 degree phase shift with respect to the master IC.

Fault Protection

Overcurrent Protection

The overcurrent function protects against any overload conditions and output shorts at worst case, by monitoring the current flowing through the upper MOSFET.

There are 2 current limiting thresholds. The first one, I_{OC1}, is to limit the high-side MOSFET peak current cycle-by-cycle. The current limit threshold is set to a default of 3.6A with the ILIMIT pin connected to GND or VCC, or left open. The current limit threshold can also be programmed by a resistor R_{LIM} at ILIMIT pin to ground. Use Equation 3 to calculate the resistor.

$$R_{LIM} = \frac{300000}{I_{OC}[A] + 0.018} \quad \text{(EQ. 3)}$$

Note that with the lower R_{LIM}, IOC1 is higher. Considering the OC programming circuit tolerances over temperature range -40°C to +105°C, 71.5k is the lowest resistor value recommended to be used for R_{LIM} to achieve highest OC threshold. With 71.5k R_{LIM}, the OC limit is 4.18A (TYP). A resistor lower than 71.5k would result in default 3.6A OC1 threshold.

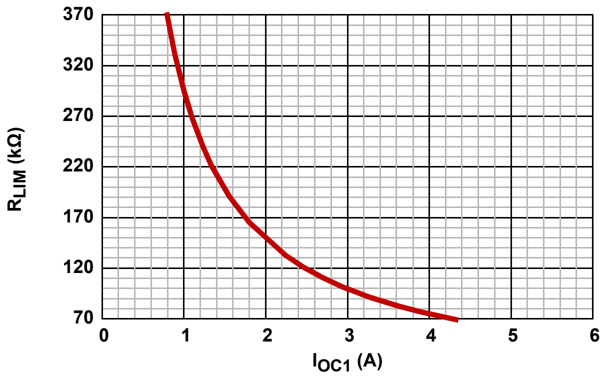


FIGURE 17. R_{LIM} vs IOC1

The second current protection threshold, I_{OC2}, is 15% higher than I_{OC1} mentioned above. Upon the instant that the high-side MOSFET current reaches I_{OC2}, the PWM shuts off after 2 cycle delay and the IC enters hiccup mode. In hiccup mode, the PWM is disabled for dummy soft-start duration equaling 5 regular soft-start periods. After this dummy soft-start cycle, the true soft-start cycle is attempted again. The I_{OC2} offers a robust and reliable protection against worst case conditions.

The frequency foldback is implemented for the ISL78205. When overcurrent limiting, the switching frequency is reduced to be proportional to the output voltage in order to keep the inductor current under limit threshold during overload conditions. The low limit of frequency under frequency foldback is 40kHz.

Overvoltage Protection

If the voltage detected on the FB pin is over 110% of reference, the high-side and low-side driver shuts down immediately and will not be allowed to turn on until the FB voltage falls down to 0.8V. When the FB voltage drops to 0.8V, the drivers are released on. If the 120% overvoltage threshold is reached, the high-side and low-side driver shut down immediately and the IC is latched off. The IC has to be reset for restart.

Thermal Protection

The ISL78205 PWM will be disabled if the junction temperature reaches +155°C. A +15°C hysteresis insures that the device will not restart until the junction temperature drops below +140°C.

Component Selection

The ISL78200 iSim model (buck mode), available on the internet (ISL78200 iSim), and can be used to simulate the ISL78205 behaviors to assist in design.

Output Capacitors

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are 2 critical factors when considering output capacitance choice. The current mode control loop allows the usage of low ESR ceramic capacitors and thus smaller board layout. Electrolytic and polymer capacitors may also be used.

Additional consideration applies to ceramic capacitors. While they offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturers data sheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations can easily result in an effective capacitance 50% lower than the rated value. Nonetheless, they are a very good choice in many applications due to their reliability and extremely low ESR.

The following equations allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR):

$$V_{OUTripple} = \frac{\Delta I}{8 * F_{SW} * C_{OUT}} \quad \text{(EQ. 4)}$$

where ΔI is the inductor's peak-to-peak ripple current, F_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 5)}$$

Regarding transient response needs, a good starting point is to determine the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor will be transferred to C_{OUT} causing its voltage to rise. After calculating capacitance required for both ripple and transient needs, choose the larger of the calculated values. The following equation determines the required output capacitor value in order to achieve a desired overshoot relative to the regulated voltage.

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * \left((V_{OUTMAX} / V_{OUT})^2 - 1 \right)} \quad \text{(EQ. 6)}$$

where V_{OUTMAX}/V_{OUT} is the relative maximum overshoot allowed during the removal of the load.

Input Capacitors

Depending upon the system input power rail conditions, the aluminum electrolytic type capacitor is normally needed to provide the stable input voltage and restrict the switching frequency pulse current in small areas over the input traces for better EMC performance. The input capacitor should be able to handle the RMS current from the switching power devices.

Ceramic capacitors must be used at the VIN pin of the IC and multiple capacitors, including 1µF and 0.1µF, are recommended. Place these capacitors as closely as possible to the IC.

Output Inductor

The inductor value determines the converter's ripple current. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is 30% to 40% of total load current. The inductor value can then be calculated using Equation 7:

$$L = \frac{V_{IN} - V_{OUT}}{Fs \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \qquad \text{(EQ. 7)}$$

Increasing the value of inductance reduces the ripple current and thus ripple voltage. However, the larger inductance value may reduce the converter's response time to a load transient. The inductor current rating should be such that it will not saturate in overcurrent conditions.

Low Side Power MOSFET

In synchronous buck application, a power N MOSFET is needed as the synchronous low side MOSFET and a good one should have low Qgd, low $r_{DS(ON)}$ and small Rg (Rg_typ < 1.5Ω recommended). Vgth_min is recommended to be higher than 1.2V. A good example is SQS462EN.

A 5.1k or smaller value resistor has to be added to connect LGATE to ground to avoid falsely turn-on of LGATE caused by coupling noise.

Output Voltage Feedback Resistor Divider

The output voltage can be programmed down to 0.8V by a resistor divider from V_{OUT} to FB, according to Equation 8.

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R_{UP}}{R_{LOW}}\right) \qquad \text{(EQ. 8)}$$

In applications requiring the least input quiescent current, large resistors should be used for the divider to keep its leakage current low. 232k is a recommended for the upper resistor.

Loop Compensation Design

The ISL78205 uses constant frequency peak current mode control architecture to achieve fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes single order system. It is much easier to design the compensator to stabilize the loop compared with voltage mode control. Peak current mode control has inherent input voltage feed-forward function to achieve good line regulation. Figure 18 shows the small signal model of a buck regulator.

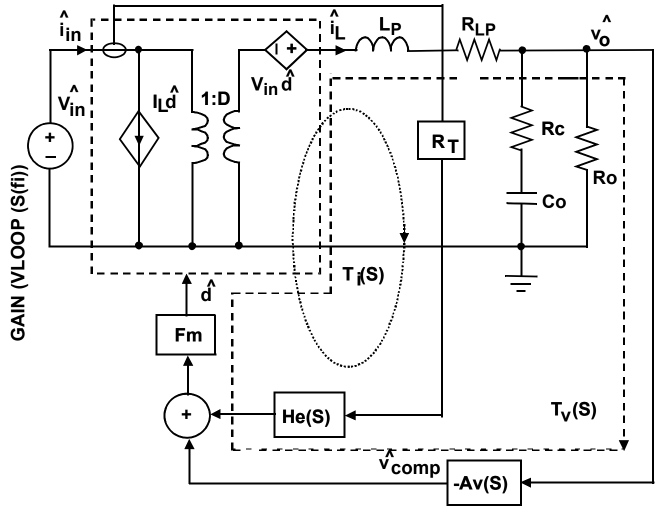


FIGURE 18. SMALL SIGNAL MODEL OF BUCK REGULATOR

PWM Comparator Gain F_m:

The PWM comparator gain F_m for peak current mode control is given by Equation 9:

$$F_m = \frac{\hat{d}}{\hat{v}_{comp}} = \frac{1}{(S_e + S_n)T_s} \qquad \text{(EQ. 9)}$$

Where S_e is the slew rate of the slope compensation and S_n is given by Equation 10.

$$S_n = R_t \frac{V_{in} - V_o}{L_P} \qquad \text{(EQ. 10)}$$

where R_t is the gain of the current amplifier.

CURRENT SAMPLING TRANSFER FUNCTION H_E(S):

In current loop, the current signal is sampled every switching cycle. It has the following transfer function in Equation 11:

$$H_e(S) = \frac{S^2}{\omega_n^2} + \frac{S}{\omega_n Q_n} + 1 \qquad \text{(EQ. 11)}$$

where Q_n and ω_n are given by $Q_n = -\frac{2}{\pi}, \omega_n = \pi f_s$

Power Stage Transfer Functions

Transfer function $F_1(S)$ from control to output voltage is:

$$F_1(S) = \frac{\hat{v}_o}{\hat{d}} = V_{in}\frac{1 + \frac{S}{\omega_{esr}}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \qquad \text{(EQ. 12)}$$

Where, $\omega_{esr} = \frac{1}{R_c C_o}, Q_p \approx R_o\sqrt{\frac{C_o}{L_P}}, \omega_o = \frac{1}{\sqrt{L_P C_o}}$

Transfer function $F_2(S)$ from control to inductor current is given by Equation 13:

$$F_2(S) = \frac{\hat{I}_o}{\hat{d}} = \frac{V_{in}}{R_o + R_{LP}} \frac{1 + \frac{S}{\omega_z}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \qquad \text{(EQ. 13)}$$

where $\omega_z = \frac{1}{R_oC_o}$.

Current loop gain $T_i(S)$ is expressed as Equation 14:

$$T_i(S) = R_tF_mF_2(S)H_e(S) \tag{EQ. 14}$$

The voltage loop gain with open current loop is Equation 15:

$$T_v(S) = KF_mF_1(S)A_v(S) \tag{EQ. 15}$$

The Voltage loop gain with current loop closed is given by Equation 16:

$$L_v(S) = \frac{T_v(S)}{1+T_i(S)} \tag{EQ. 16}$$

If $T_i(S)$>>1, then Equation 16 can be simplified as Equation 17:

$$L_v(S) = \frac{R_o+R_{LP}}{R_t}\frac{1+\frac{S}{\omega_{esr}}}{1+\frac{S}{\omega_p}}\frac{A_v(S)}{H_e(S)}, \omega_p \approx \frac{1}{R_oC_o} \tag{EQ. 17}$$

Equation 17 shows that the system is a single order system. Therefore, a simple type II compensator can be easily used to stabilize the system. While type III compensator is needed to expand the bandwidth for current mode control in some cases.

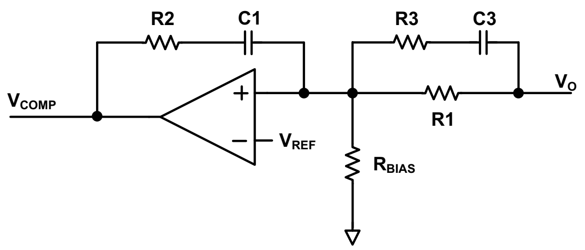


FIGURE 19. TYPE III COMPENSATOR

A compensator with 2 zeros and 1 pole is recommended for this part as shown in Figure 19. Its transfer function is expressed as Equation 18:

$$A_v(S) = \frac{\hat{v}_{comp}}{\hat{v}_O} = \frac{1}{SR_1C_1}\frac{\left(1+\frac{S}{\omega_{cz1}}\right)\left(1+\frac{S}{\omega_{cz2}}\right)}{\left(1+\frac{S}{\omega_{cp}}\right)} \tag{EQ. 18}$$

where,

$$\omega_{cz1} = \frac{1}{R_2C_1}, \quad \omega_{cz2} = \frac{1}{(R_1+R_3)C_3}, \omega_{cp} = \frac{1}{R_3C_3}$$

Compensator design goal:

Loop bandwidth f_c: $\left(\frac{1}{4} \text{to} \frac{1}{10}\right)f_s$

Gain margin: >10dB

Phase margin: 45°

The compensator design procedure is as follows:

1. **Position ω_{CZ2} and ω_{CP} to derive R3 and C3.**

Put the compensator zero ω_{CZ2} at (1 to 3)/(R_oC_o)

$$\omega_{cz2} = \frac{3}{R_oC_o} \tag{EQ. 19}$$

Put the compensator pole ω_{CP} at ESR zero or 0.35 to 0.5 times of switching frequency, whichever is lower. In all-ceramic-cap design, the ESR zero is normally higher than half of the switching frequency. R3 and C3 can be derived as following:

Case A: ESR zero $\frac{1}{2\pi R_cC_o}$ less than (0.35 to 0.5)f_s

$$C_3 = \frac{R_oC_o - 3R_cC_o}{3R_1} \tag{EQ. 20}$$

$$R_3 = \frac{3R_cR_1}{R_o - 3R_c} \tag{EQ. 21}$$

Case B: ESR zero $\frac{1}{2\pi R_cC_o}$ larger than (0.35 to 0.5)f_s

$$C_3 = \frac{0.33R_oC_of_s - 0.46}{f_sR_1} \tag{EQ. 22}$$

$$R_3 = \frac{R_1}{0.73R_oC_of_s - 1} \tag{EQ. 23}$$

2. **Derive R2 and C1.**

The loop gain $L_V(S)$ at cross over frequency of f_c has unity gain. Therefore, C1 is determined by Equation 24.

$$C_1 = \frac{(R_1+R_3)C_3}{2\pi f_cR_tR_1C_o} \tag{EQ. 24}$$

The compensator zero ω_{CZ1} can boost the phase margin and bandwidth. To put ω_{CZ1} at 2 times of cross cover frequency f_c is a good start point. It can be adjusted according to specific design. R1 can be derived from Equation 25.

$$R_2 = \frac{1}{4\pi f_cC_1} \tag{EQ. 25}$$

Example: V_{IN} = 12V, V_O = 5V, I_O = 2A, fs = 500kHz, C_o = 60µF/3mΩ, L = 10µH, R_t = 0.20V/A, f_c = 50kHz, R1 = 105k, R_{BIAS} = 20kΩ.

Select the crossover frequency to be 35kHz. Since the output capacitors are all ceramics, use Equations 22 and 23 to derive R3 to be 20k and C3 to be 470pF.

Then use Equations 24 and 25 to calculate C1 to be 180pF and R2 to be 12.7k. Select 150pF for C1 and 15k for R2.

There is approximately 30pF parasitic capacitance between the COMP to FB pins that contributes to a high frequency pole.

Figure 20 shows the simulated bode plot of the loop. It is shown that it has 26kHz loop bandwidth with 70° phase margin and H28dB gain margin.

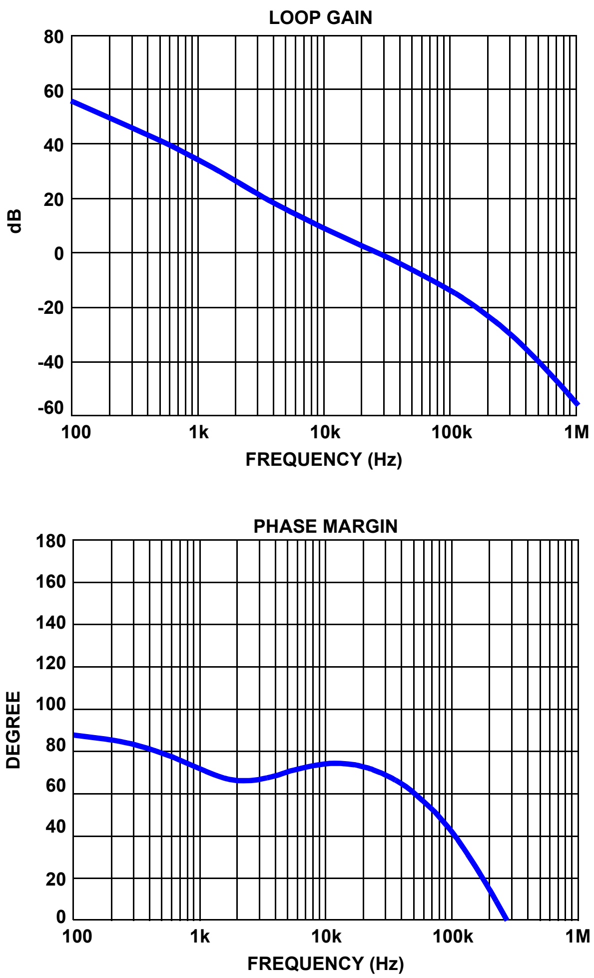


FIGURE 20. SIMULATED LOOP GAIN

PGOOD

The PGOOD pin is output of an open drain transistor (refer to at "Block Diagram" on page 4). An external resistor is required to be pulled up to VCC for proper PGOOD function. At startup, PGOOD will be turned HIGH (internal PGOOD open drain transistor is turned off) with 1000 cycles delay after soft start is finished (soft start ramp reaching 1.02V) and FB voltage is within OV/UV window(90%REF<FB<110%REF).

At normal operation, PGOOD will be pulled low with no delay if any of the OV (110%) or UV (90%) comparator is tripped. The PGOOD will be released HIGH with 1000 cycle delay after FB recovers to be within OV/UV window(90%REF<FB<110%REF). When EN is pulled low or VCC is below POR, PGOOD is pulled low with no delay.

In the case when the PGOOD pin is pulled up by external bias supply instead of VCC of itself, when the part is disabled, the internal PGOOD open drain transistor is off, the external bias supply can charge PGOOD pin HIGH. This should be known as false PGOOD reporting. At start-up when VCC rise from 0, PGOOD will be pulled low when VCC reaches 1V. After EN pulled low and VCC falling, PGOOD internal open drain transistor will open with high impedance when VCC falls below 1V. The time between EN pulled low and PGOOD OPEN depends on the VCC falling time to 1V.

In non-synchronous buck application, the phase node will show normal oscillations after high-side turns off due to oscillations among the parasitic capacitors at phase node. PGOOD signal could falsely dip due to this ringing. So in non-synchronous buck application when PGOOD function is used, an RC snubber (suggesting 200Ω and 2.2nF as typical) at phase node is highly recommended to reduce this ringing in order for correct function of PGOOD.

Layout Suggestions

1. Place the input ceramic capacitors as close as possible to the IC VIN pin and power ground connecting to the power MOSFET or diode. Keep this loop (input ceramic capacitor, IC VIN pin and MOSFET/Diode) as tiny as possible to achieve the least voltage spikes induced by the trace parasitic inductance.
2. Place the input aluminum capacitors close to the IC VIN pin.
3. Keep the phase node copper area small, but large enough to handle the load current.
4. Place the output ceramic and aluminum capacitors also close to the power stage components.
5. Put vias (20 recommended) in the bottom pad of the IC. The bottom pad should be placed in the ground copper plane with area as large as possible in multiple layers to effectively reduce the thermal impedance.
6. Place the 4.7µF ceramic decoupling capacitor at the VCC pin and as close as possible to the IC. Put multiple vias (≥3) close to the ground pad of this capacitor.
7. Keep the bootstrap capacitor close to the IC.
8. Keep the LGATE drive trace as short as possible and try to avoid using via in LGATE drive path to achieve the lowest impedance.
9. Place the positive voltage sense trace close to the load for tighter regulation.
10. Put all the peripheral control components close to the IC.

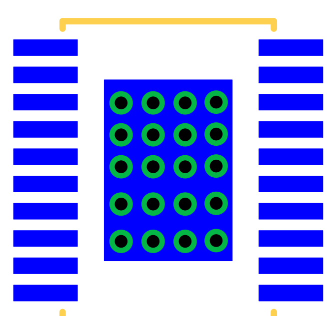


FIGURE 21. PCB VIA PATTERN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
February 19, 2014	FN7926.3	Page 1 Features bullet: Returned "Qualified for automotive applications" to original verbiage "AEC-Q100 Qualified"
October 17, 2013	FN7926.2	Added more descriptions for PGOOD function on page 17. Added ISL78205EVAL1Z and ISL78205EVAL2Z evaluation boards to Ordering information table on page 3. On page 12: "Synchronous and Non-Synchronous Buck" section, added more descriptions. Updated POD "M20.173A" to datasheet.
July 24, 2013		Added more descriptions for PGOOD function.
May 10, 2012	FN7926.1	1. Added application design guides for selection of inductor and capacitor and loop compensation. 2. Added typical electrical specification of EN pull-up current and Synchronization. 3. Under "Output Voltage" description, correct "(1/Fs t_{MINOFF})" To "(1 - Fs * $t_{MIN(OFF)}$)". 4. Add recommendation of the maximum programmable OC threshold to be 4.18A (TYP) with 71.5k R_{LIM}. 5. Added "C_3" to Equation 24 on page 16.
September 22, 2011	FN7926.0	Initial Release

About Intersil

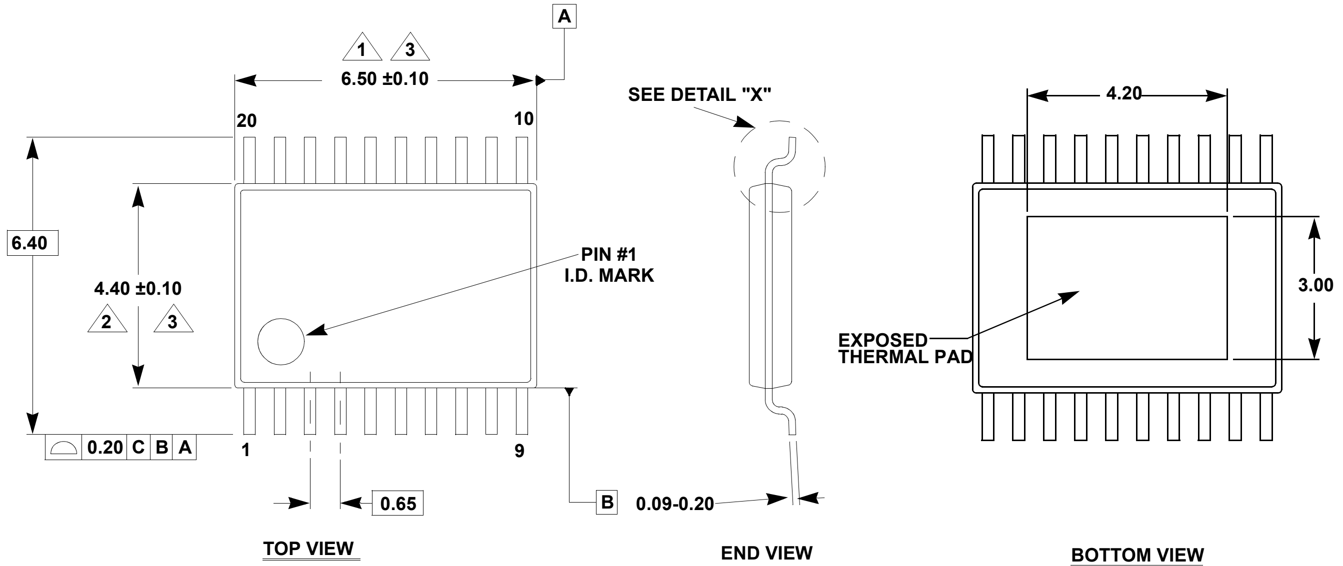
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

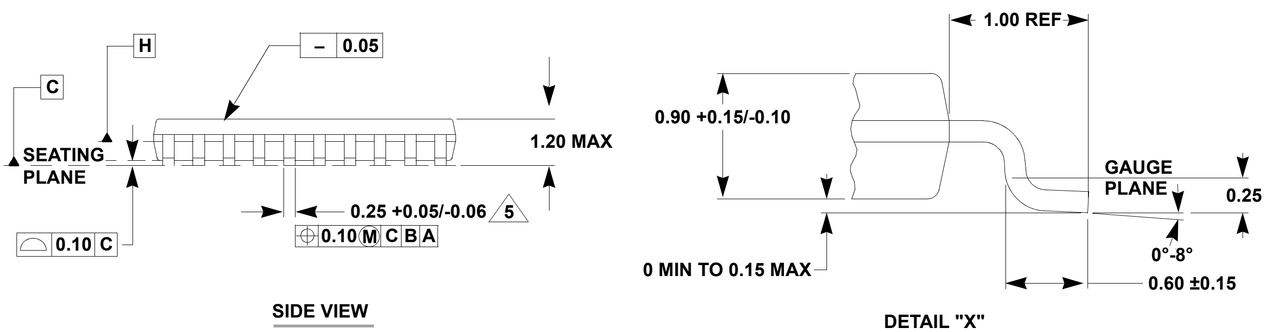
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

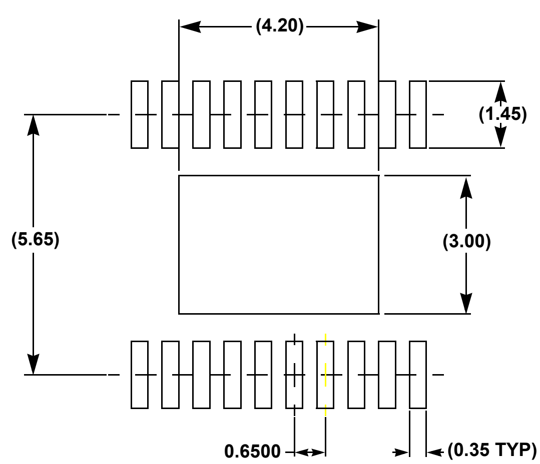
Package Outline Drawing

M20.173A

20 LEAD HEAT-SINK THIN SHRINK SMALL OUTLINE PACKAGE (HTSSOP)
Rev 0, 8/13







TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.