Dual $J\overline{K}$ flip-flop with set and reset; positive-edge trigger 74LVC109

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output capability: standard**
- **I_{CC} category: flip-flops**

DESCRIPTION

The 74LVC109 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT109.

The 74LVC109 is a dual positive-edge triggered JK-type flip-flop featuring individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table.
The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The $J\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 3.3 V	 4.0 4.5 4.5	ns
f_{max}	maximum clock frequency		250	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	27	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC109D	16	SO	plastic	SOT109-1
74LVC109DB	16	SSOP	plastic	SOT338-1
74LVC109PW	16	TSSOP	plastic	SOT403-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 15	1$\overline{R}_D$, 2$\overline{R}_D$	asynchronous reset input (active LOW)
2, 14, 3, 13	1J, 2J, 1$\overline{K}$, 2$\overline{K}$	synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
5, 11	1$\overline{S}_D$, 2$\overline{S}_D$	asynchronous set inputs (active LOW)
6, 10	1Q, 2Q	true flip-flop outputs
7, 9	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

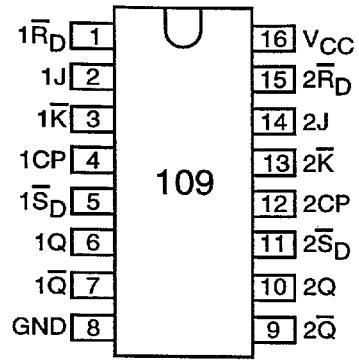


Fig.1 Pin configuration.

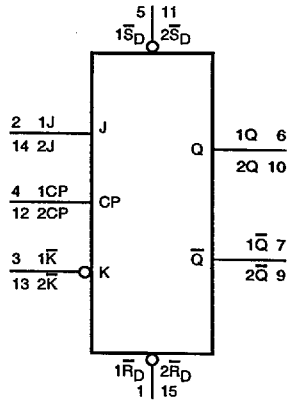


Fig.2 Logic symbol.

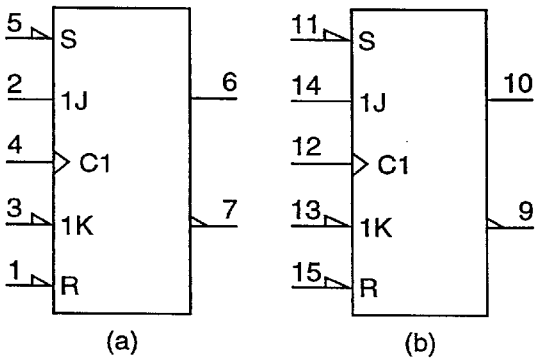


Fig3. IEC logic symbol.

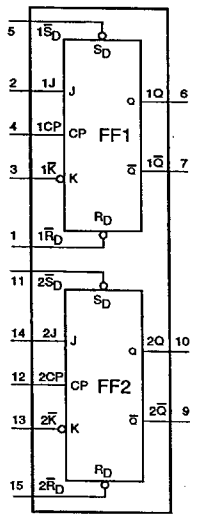


Fig.4 Functional diagram.

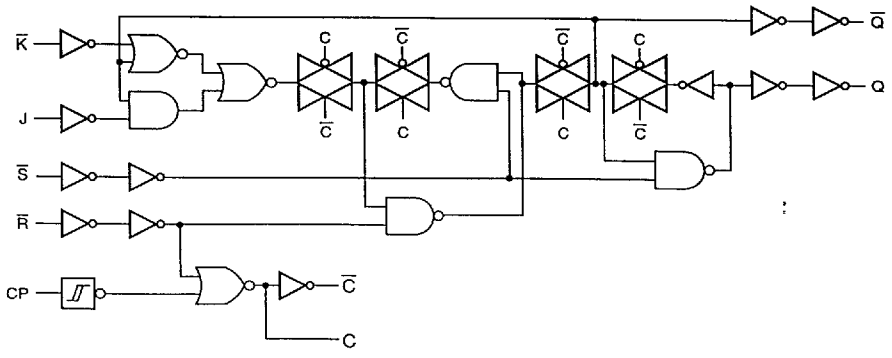


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	nCP	nJ	$n\overline{K}$	nQ	$n\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↑	h	l	$\overline{q}$	q
load "0" (reset)	H	H	↑	l	l	L	H
load "1" (set)	H	H	↑	h	h	H	L
hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.
X = don't care
↑ = LOW-to-HIGH CP transition

DC CHARACTERISTICS FOR 74LVC109

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74LVC109

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, $n\overline{Q}$	–	–	–	ns	1.2	Figs 6, 8
		–	–	8.5		2.7	
		–	4.3*	7.5		3.0 to 3.6	
t_{PLH}	propagation delay $n\overline{S}_D$ to nQ	–	–	–	ns	1.2	Figs 7, 8
		–	–	9.0		2.7	
	$n\overline{R}_D$ to $n\overline{Q}$	–	4.5*	8.0		3.0 to 3.6	
t_{PHL}	propagation delay $n\overline{S}_D$ to $n\overline{Q}$	–	–	–	ns	1.2	Figs 7, 8
		–	–	10		2.7	
	$n\overline{R}_D$ to nQ	–	5.2*	9.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LVC109 *(Continued)*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_W	clock pulse width HIGH or LOW	– 3.3	– 2.0*	– –	ns	2.7 3.0 to 3.6	Fig.6
t_W	set or reset pulse width HIGH or LOW	– 3.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.7
t_{rem}	removal time $n\overline{S}_D$, $n\overline{R}_D$ to nCP	– – 3.0	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{su}	set-up time nJ, $n\overline{K}$ to nCP	– – 2.5	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_h	hold time nJ, $n\overline{K}$ to nCP	– – 2.0	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.6
f_{max}	maximum clock pulse frequency	– 150	– 225*	– –	MHz	2.7 3.0 to 3.6	Fig.6

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

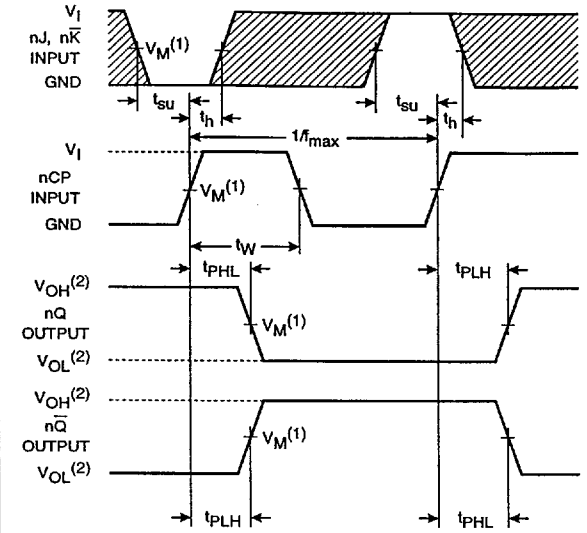


Fig.6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nJ, nK̄ to nCP set-up, the nCP to nJ, nK̄ hold times and the maximum clock pulse frequency.

Note to Fig.6: The shaded areas indicate when the input is permitted to change for predictable output performance.

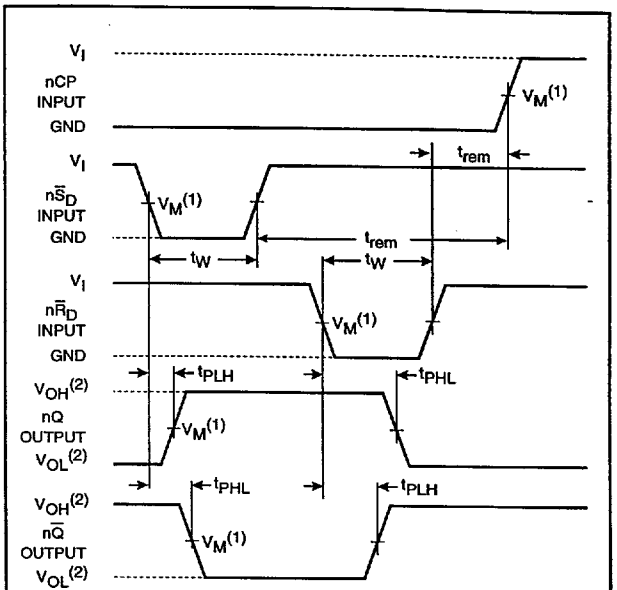
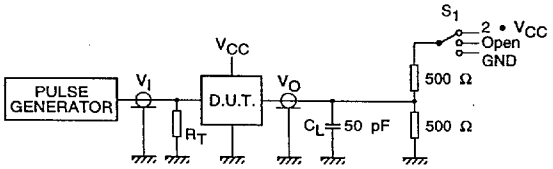


Fig.7 Waveforms showing the set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the $n\overline{R}_D$, $n\overline{S}_D$ to nCP removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.8 Load circuitry for switching times.