

Clock Generator for PowerQUICC III

MPC9865

The MPC9865 is a PLL based clock generator specifically designed for Freescale Microprocessor and Microcontroller applications including the PowerPC and PowerQUICC. This device generates a microprocessor input clock. The microprocessor clock is selectable in output frequency to any of the commonly used microprocessor input and bus frequencies. The device offers eight low skew clock outputs in two banks, each configurable to support different clock frequencies. The extended temperature range of the MPC9865 supports telecommunication and networking requirements.

Features

- 8 LVCMOS outputs for processor and other circuitry
- Crystal oscillator or external reference input
- 25 or 33 MHz Input reference frequency
- Selectable output frequencies include = 200, 166, 133, 125, 111, 100, 83, 66, 50, 33, or 16 MHz
- Buffered reference clock output (2 copies)
- Low cycle-to-cycle and period jitter
- 100-lead PBGA package
- 100-lead Pb-free package available
- 3.3 V supply with 3.3 V or 2.5 V LVCMOS output supplies
- Supports computing, networking, telecommunications applications
- Ambient temperature range -40°C to $+85^{\circ}\text{C}$

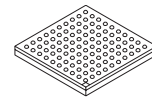
Functional Description

The MPC9865 uses either a 25 or 33 MHz reference frequency to generate 8 LVCMOS output clocks, of which, the frequency is selectable from 16 MHz to 200 MHz. The reference is applied to the input of a PLL and multiplied to 2 GHz. Output dividers, divide this frequency by 10, 12, 15, 16, 18, 20, 24, 30, 40, 60, or 120 to produce output frequencies of 200, 166, 133, 125, 111, 100, 83, 66, 50, 33, or 16 MHz. The single-ended LVCMOS outputs provide 8 low skew outputs for use in driving a microprocessor or microcontroller clock input as well as other system components. The input reference, either crystal or external input is also buffered to a separate dual outputs that may be used as the clock source for a Ethernet PHY if desired.

The reference clock may be provided by either an external clock input of 25 or 33 MHz. An internal oscillator requiring a 25 MHz crystal for frequency control may also be used. The external clock source may be applied to either of two clock inputs and selected via the CLK_SEL control input. Both single ended LVCMOS and differential LVPECL inputs are available. The crystal oscillator or external clock input is selected via the input pin of XTAL_SEL. Other than the crystal, no external components are required for crystal oscillator operation. The REF_33 MHz configuration pin is used to select between a 33 and 25 MHz input frequency.

The MPC9865 is packaged in a 100 lead MAPBGA package to optimize both performance and board density.

**MICROPROCESSOR
CLOCK GENERATOR**



**VF SUFFIX
VM SUFFIX (PB-FREE)
100 MAPBGA PACKAGE
CASE 1462-01**

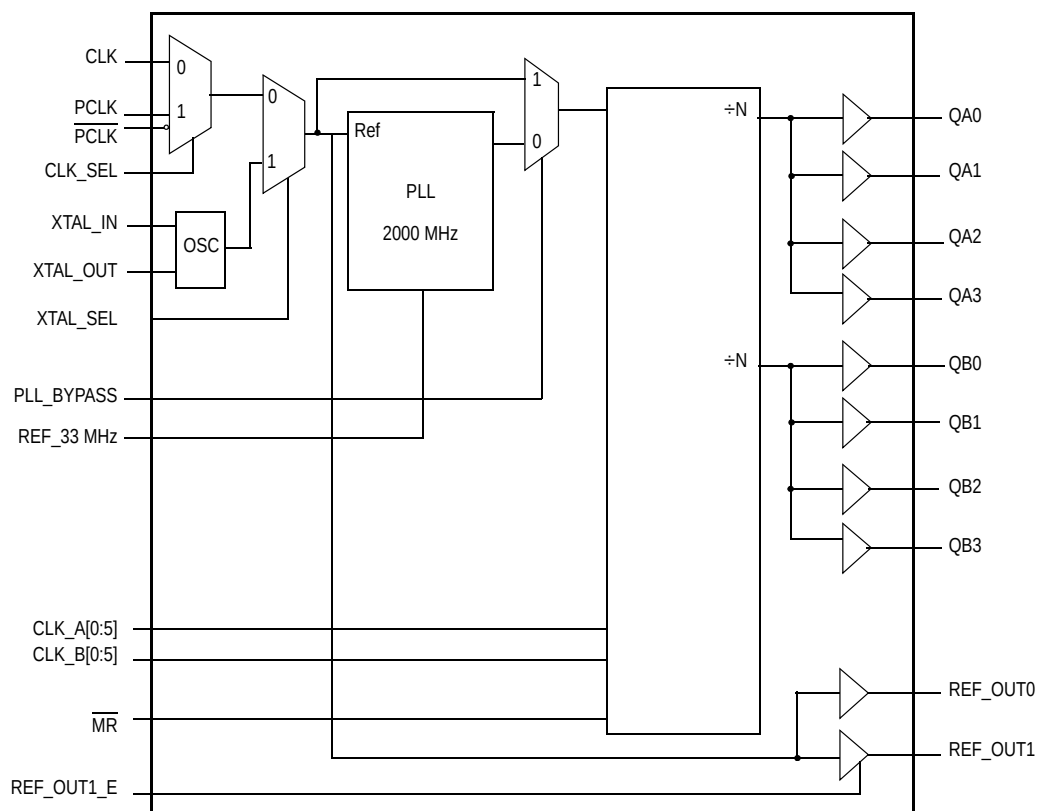


Figure 1. MPC9865 Logic Diagram

Table 1. Pin Configurations

Pin	I/O	Type	Function	Supply	Active/State
CLK	Input	LVC MOS	PLL Reference Clock Input (pull-down)	V _{DD}	
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	PLL reference clock input (PCLK — pull-down, $\overline{\text{PCLK}}$ — pull-up and pull-down)	V _{DD}	—
QA0, QA1, QA2, QA3 QB0, QB1, QB2, QB3	Output	LVC MOS	Clock Outputs	V _{DDOA}	—
REF_OUT0 REF_OUT1	Output	LVC MOS	Reference Output (25 MHz or 33 MHz)	V _{DD}	—
XTAL_IN	Input	LVC MOS	Crystal Oscillator Input Pin	V _{DD}	—
XTAL_OUT	Output	LVC MOS	Crystal Oscillator Output Pin	V _{DD}	—
CLK_SEL	Input	LVC MOS	Select between CLK and PCLK input (pull-down)	V _{DD}	High
XTAL_SEL	Input	LVC MOS	Select between External Input and Crystal Oscillator Input (pull-down)	V _{DD}	High
REF_33 MHz	Input	LVC MOS	Selects 33 MHz input (pull-down)	V _{DD}	High
REF_OUT1_E	Input	LVC MOS	Enables REF_OUT1 output (pull-down)	V _{DD}	High
$\overline{\text{MR}}$	Input	LVC MOS	Master Reset (pull-up)	V _{DD}	Low
PLL_BYPASS	Input	LVC MOS	Select PLL or static test mode (pull-down)	V _{DD}	High
CLK_A[0:5] ⁽¹⁾	Input	LVC MOS	Configures Bank A clock output frequency (pull-up)	V _{DD}	—
CLK_B[0:5] ⁽²⁾	Input	LVC MOS	Configures Bank B clock output frequency (pull-up)	V _{DD}	—
V _{DD}	—	—	3.3 V Supply	—	—
V _{DDA}	—	—	Analog Supply	—	—
V _{DDOA}	—	—	Output Supply — Bank A	—	—
V _{DDOB}	—	—	Output Supply — Bank B	—	—
GND	—	—	Ground	—	—

1. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb).
2. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb).

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLK	PCLK
XTAL_SEL	0	CLK _x	XTAL
PLL_BYPASS	0	Normal	Bypass
REF_OUT1_E	0	Disables REF_OUT1	Enables REF_OUT1
REF_33 MHz	0	Selects 25 MHz Reference	Selects 33 MHz Reference
$\overline{\text{MR}}$	1	Reset	Normal

CLK_A and CLK_B control output frequencies. See [Table 3](#) for specific device configuration.

Table 3. Output Configurations (Banks A & B)

CLK_x[0:5] ⁽¹⁾	CLK_x[0] (msb)	CLK_x[1]	CLK_x[2]	CLK_x[3]	CLK_x[4]	CLK_x[5] (lsb)	N	Frequency (MHz)
111111	1	1	1	1	1	1	126	15.87
111100	1	1	1	1	0	0	120	16.67
101000	1	0	1	0	0	0	80	25.00
011110	0	1	1	1	1	0	60	33.33
010100	0	1	0	1	0	0	40	50.00
010000	0	1	0	0	0	0	32	62.5
001111	0	0	1	1	1	1	30	66.67
001100	0	0	1	1	0	0	24	83.33
001010	0	0	1	0	1	0	20	100.00
001001	0	0	1	0	0	1	18	111.11
001000	0	0	1	0	0	0	16	125.00
000111	0	0	0	1	1	1	15	133.33
000110	0	0	0	1	1	0	12	166.67
000101	0	0	0	1	0	1	10	200.00
000100	0	0	0	1	0	0	g ⁽²⁾	250

1. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb).

2. Minimum value for N.

OPERATION INFORMATION

Output Frequency Configuration

The MPC9865 was designed to provide the commonly used frequencies in PowerQUICC, PowerPC and other microprocessor systems. Table 3 lists the configuration values that will generate those common frequencies. The MPC9865 can generate numerous other frequencies that may be useful in specific applications. The output frequency (f_{out}) of either Bank A or Bank B may be calculated by the following equation.

$$f_{out} = 2000 / N$$

where f_{out} is in MHz and $N = 2 * CLK_x[0:5]$

This calculation is valid for all values of N from 8 to 126. Note that N = 15 is a modified case of the configuration inputs

CLK_x[0:5]. To achieve N = 15 CLK_x[0:5] is configured to 00111 or 7.

Crystal Input Operation

TBD

Power-Up and $\overline{MR}$ Operation

Figure 2 defines the release time and the minimum pulse length for MR pin. The MR release time is based upon the power supply being stable and within V_{DD} specifications. See Table 9 for actual parameter values. The MPC9865 may be configured after release of reset and the outputs will be stable for use after lock indication is obtained.

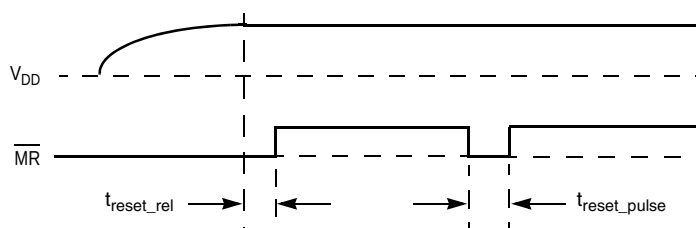


Figure 2. MR Operation

Power Supply Bypassing

The MPC9865 is a mixed analog/digital product. The architecture of the MPC9865 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{DD} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

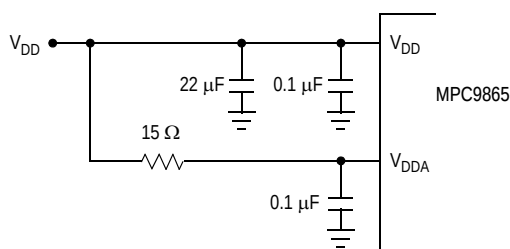


Figure 3. V_{CC} Power Supply Bypass

Power Consumption Calculation

For unloaded outputs the power consumption of the MPC9865 can be calculated as follows.

$$P = V_{DD} * I_{DDBASE} + n_A * (V_{DDOA} ** 2 * C_{PD} * f_A) + n_B * (V_{DDOB} ** 2 * C_{PD} * f_B)$$

where

V_{DD} = core supply voltage

I_{DDBASE} = base supply current

n_A = number of A bank outputs (= 4)

n_B = number of B bank outputs (= 4)

V_{DDOA} = voltage supply on bank A outputs

V_{DDOB} = voltage supply on bank B outputs

C_{PD} = power dissipation capacitance

f_A = frequency of bank A outputs

f_B = frequency of bank B outputs

Table 4. Absolute Maximum Ratings⁽¹⁾

Symbol	Characteristics	Min	Max	Unit	Condition
V _{DD}	Supply Voltage (core)	−0.3	3.8	V	
V _{DDA}	Supply Voltage (Analog Supply Voltage)	−0.3	V _{DD}	V	
V _{DDOx}	Supply Voltage (LVCMOS output for Bank A and B)	−0.3	V _{DD}	V	
V _{IN}	DC Input Voltage	−0.3	V _{DD} +0.3	V	
V _{OUT}	DC Output Voltage ⁽²⁾	−0.3	V _{DDx} +0.3	V	
I _{IN}	DC Input Current		±20	mA	
I _{OUT}	DC Output Current		±50	mA	
T _S	Storage Temperature	−65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.
2. V_{DDx} references power supply pin associated with specific output pin.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{TT}	Output Termination Voltage		V _{DD} ÷ 2		V	
C _{IN}	Input Capacitance		4		pF	Inputs
C _{PD}	Power Dissipation Capacitance		10		pF	Per Output
θ _{JA}	Thermal Resistance (Junction-to-Ambient)		54.5		°C/W	Air flow = 0
T _A	Ambient Temperature	−40		85	°C	

Table 6. DC Characteristics (T_A = −40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Supply Current for V _{DD} = 3.3 V ± 5%, V _{DDOA} = 3.3 V ± 5 and V _{DDOB} = 3.3 V ± 5%						
I _{DDBASE}	Base Supply Current (Core)		TBD	TBD	mA	V _{DD} + V _{DDA} pins
I _{DDA}	Maximum Quiescent Supply Current (Analog Supply)			TBD	mA	V _{DDIN} pins

Table 7. LVPECL DC Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C)⁽¹⁾

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential LVPECL Clock Inputs (CLK1, $\overline{\text{CLK1}}$) for $V_{DD} = 3.3\text{ V} \pm 0.5\%$						
V_{PP}	Differential Voltage ⁽²⁾ (peak-to-peak) (LVPECL)	250			mV	
V_{CMR}	Differential Input Crosspoint Voltage ⁽³⁾ (LVPECL)	1.0		$V_{DD} - 0.6$	V	

1. AC characteristics are design targets and pending characterization.
2. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

Table 8. LVCMOS I/O DC Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS for $V_{DD} = 3.3\text{ V} \pm 5\%$						
V_{IH}	Input High Voltage	2.0		$V_{DD} + 0.3$	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current ⁽¹⁾			± 200	μA	$V_{IN} = V_{DDL}$ or GND
LVCMOS for $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDOA} = 3.3\text{ V} \pm 5\%$ and $V_{DDOB} = 3.3\text{ V} \pm 5\%$						
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -24\text{ mA}$
V_{OL}	Output Low Voltage			0.5	V	$I_{OL} = 24\text{ mA}$
Z_{OUT}	Output Impedance		14 – 17		Ω	
LVCMOS for $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDOA} = 2.5\text{ V} \pm 5\%$ and $V_{DDOB} = 2.5\text{ V} \pm 5\%$						
V_{OH}	Output High Voltage	1.9			V	$I_{OH} = -15\text{ mA}$
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 15\text{ mA}$
Z_{OUT}	Output Impedance		18 – 22		Ω	

1. Inputs have pull-down resistors affecting the input current.

Table 9. AC Characteristics ($V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDOAB} = 3.3 \text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)(¹) (²)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Input and Output Timing Specification						
f_{ref}	Input Reference Frequency (25 MHz input) Input Reference Frequency (33 MHz input) XTAL Input Input Reference Frequency in PLL Bypass Mode(³)		25 33 25	250	MHz MHz MHz MHz	PLL bypass
f_{VCO}	VCO Frequency Range		2000		MHz	
f_{MCX}	Output Frequency Bank A output Bank B output	15.87 15.87		200 200	MHz MHz	PLL locked
f_{refPW}	Reference Input Pulse Width	2			ns	
f_{refCcc}	Input Frequency Accuracy			100	ppm	
t_r, t_f	Output Rise/Fall Time	150		500	ps	20% to 80%
DC	Output Duty Cycle	45	50	55	%	Bank A and B
PLL Specifications						
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_{reset_ref}	MR Hold Time on Power Up	10			ns	
t_{reset_pulse}	MR Hold Time	10			ns	
Skew and Jitter Specifications						
$t_{sk(O)}$	Output-to-Output Skew (within a bank)			50	ps	
$t_{sk(O)}$	Output-to-Output Skew (across banks A and B)			100	ps	$V_{DDOA} = 3.3 \text{ V}$ $V_{DDOB} = 3.3 \text{ V}$
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter			150	ps	Bank A and B
$t_{JIT(PER)}$	Period Jitter			150	ps	Bank A and B
t_r, t_f	Output Rise/Fall Time			TBD	ns	20% to 80%

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .
3. In bypass mode, the MPC9865 divides the input reference clock.

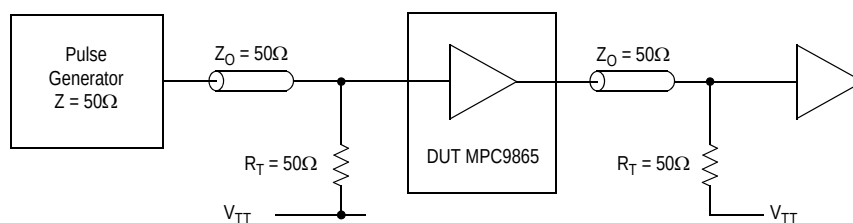


Figure 4. MPC9865 AC Test Reference (LVCMOS Outputs)

Table 10. MPC9865 Pin Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10
A	V _{DDOA}	V _{DDOA}	CLKA[1]	CLKA[3]	CLKA[5]	V _{DD}	QA1	QA2	V _{DDOA}	V _{DDOA}
B	V _{DDOA}	V _{DDOA}	CLKA[0]	CLKA[2]	CLKA[4]	QA0	V _{DDOA}	QA3	V _{DDOA}	V _{DDOA}
C	RSVD	RSVD	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	REF_OUT[0]
D	V _{DDA}	V _{DDA}	V _{DD}	GND	GND	GND	GND	V _{DD}	RSVD	REF_OUT[1]
E	XTAL_SEL	CLK	V _{DD}	GND	GND	GND	GND	V _{DD}	V _{DD}	GND
F	PCLK	PCLK	V _{DD}	GND	GND	GND	GND	V _{DD}	RSVD	RSVD
G	CLK_SEL	REF_33MHz	V _{DD}	GND	GND	GND	GND	V _{DD}	PLL_BYPASS	MR
H	XTAL_IN	XTAL_OUT	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	RSVD	REF_OUT1E
J	V _{DDOB}	V _{DDOB}	CLKB[0]	CLKB[2]	CLKB[4]	QB0	V _{DDOB}	QB3	V _{DDOB}	V _{DDOB}
K	V _{DDOB}	V _{DDOB}	CLKB[1]	CLKB[3]	CLKB[5]	V _{DD}	QB1	QB2	V _{DDOB}	V _{DDOB}

Table 11. MPC9865 Pin List

Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA
V _{DDOA}	A1	RSVD	C1	XTAL_SEL	E1	CLK_SEL	G1	V _{DDOB}	J1
V _{DDOA}	A2	RSVD	C2	CLK	E2	REF_33MHz	G2	V _{DDOB}	J2
CLKA[1]	A3	V _{DD}	C3	V _{DD}	E3	V _{DD}	G3	CLKB[0]	J3
CLKA[3]	A4	V _{DD}	C4	GND	E4	GND	G4	CLKB[2]	J4
CLKA[5]	A5	V _{DD}	C5	GND	E5	GND	G5	CLKB[4]	J5
V _{DD}	A6	V _{DD}	C6	GND	E6	GND	G6	QB0	J6
QA1	A7	V _{DD}	C7	GND	E7	GND	G7	V _{DDOB}	J7
QA2	A8	V _{DD}	C8	V _{DD}	E8	V _{DD}	G8	QB3	J8
V _{DDOA}	A9	V _{DD}	C9	V _{DD}	E9	PLL_BYPASS	G9	V _{DDOB}	J9
V _{DDOA}	A10	REF_OUT0	C10	GND	E10	MR	G10	V _{DDOB}	J10
V _{DDOA}	B1	V _{DDA}	D1	PCLK	F1	XTAL_IN	H1	V _{DDOB}	K1
V _{DDOA}	B2	V _{DDA}	D2	PCLK	F2	XTAL_OUT	H2	V _{DDOB}	K2
CLKA[0]	B3	V _{DD}	D3	V _{DD}	F3	V _{DD}	H3	CLKB[1]	K3
CLKA[2]	B4	GND	D4	GND	F4	V _{DD}	H4	CLKB[3]	K4
CLKA[4]	B5	GND	D5	GND	F5	V _{DD}	H5	CLKB[5]	K5
QA0	B6	GND	D6	GND	F6	V _{DD}	H6	V _{DD}	K6
V _{DDOA}	B7	GND	D7	GND	F7	V _{DD}	H7	QB1	K7
QA3	B8	V _{DD}	D8	V _{DD}	F8	V _{DD}	H8	QB2	K8
V _{DDOA}	B9	RSVD	D9	RSVD	F9	RSVD	H9	V _{DDOB}	K9
V _{DDOA}	B10	REF_OUT1	D10	RSVD	F10	REF_OUT1_E	H10	V _{DDOB}	K10

Figure 1 consists of three views of a test specimen: (a) Top view, (b) Bottom view, and (c) Side view.

(a) Top view: A rectangular specimen with a width of 11 units and a height of 11 units. A 4X magnification detail of the bottom right corner shows a semi-circular feature with a radius of 0.2 units. A 100X magnification detail of the top left corner shows a rectangular feature with a width of 0.12 units and a height of 0.35 units. The A1 INDEX AREA is indicated by a hatched square in the top left corner.

(b) Bottom view: A rectangular specimen with a width of 10 units and a height of 10 units. A 9X 1 magnification detail of the top left corner shows a rectangular feature with a width of 0.5 units and a height of 0.5 units. A 100X magnification detail of the bottom right corner shows a rectangular feature with a width of 0.45 units and a height of 0.55 units. The A1 INDEX AREA is indicated by a hatched square in the bottom left corner.

(c) Side view: A rectangular specimen with a width of 1.7 MAX units and a height of 1.18 units. A 100X magnification detail of the top left corner shows a rectangular feature with a width of 0.12 units and a height of 0.35 units. A 5X magnification detail of the top right corner shows a rectangular feature with a width of 0.43 units and a height of 0.29 units. A 4X magnification detail of the bottom right corner shows a rectangular feature with a width of 0.43 units and a height of 0.29 units. The SEATING PLANE is indicated by a horizontal line at the top of the specimen.

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	CASE NUMBER: 1462-01		26 MAY 2005	
	STANDARD: JEDEC MO-192 DAC-1			

VA SUFFIX
VM SUFFIX (PB-FREE)
100 MAPBGA PACKAGE
CASE 1462-01
ISSUE A

PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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	CASE NUMBER: 1462-01	26 MAY 2005
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**VA SUFFIX
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ISSUE A**

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