

PHU101NQ03LT

N-channel TrenchMOS logic level FET

Rev. 04 — 30 June 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC convertors

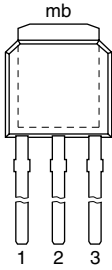
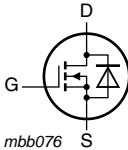
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	166	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 50\text{ A}$; $V_{DS} = 15\text{ V}$; $T_j = 25\text{ °C}$; see Figure 11	-	8	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9 ; see Figure 10	-	4.5	5.5	mΩ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT533 (IPAK)	 <i>mbb076</i>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PHU101NQ03LT	IPAK	plastic single-ended package (IPAK); 3 leads (in-line)	SOT533

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

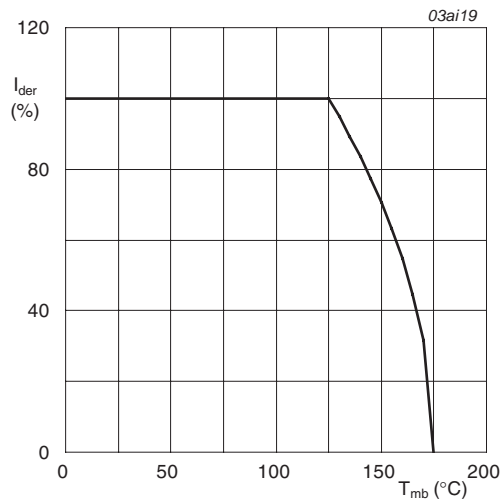
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	75	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	-	75	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 3	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	166	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
V_{GSM}	peak gate-source voltage	pulsed; $\delta = 25\%$; $T_j \leq 150\text{ °C}$; $t_p \leq 50\text{ }\mu\text{s}$	-25	25	V

Source-drain diode

I_S	source current	$T_{mb} = 25\text{ °C}$	-	75	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	240	A

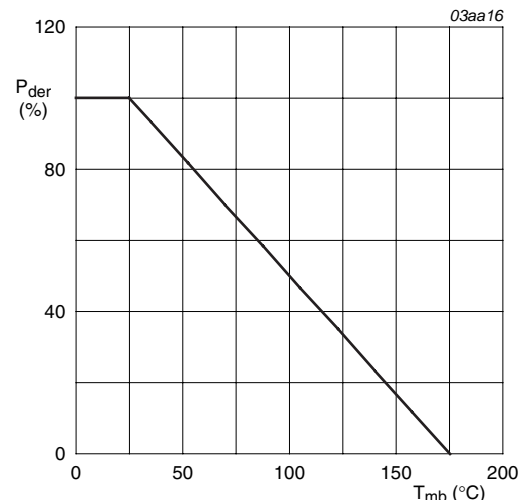
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 43\text{ A}$; $V_{sup} \leq 15\text{ V}$; unclamped; $t_p = 0.19\text{ ms}$; $R_{GS} = 50\text{ }\Omega$	-	185	mJ
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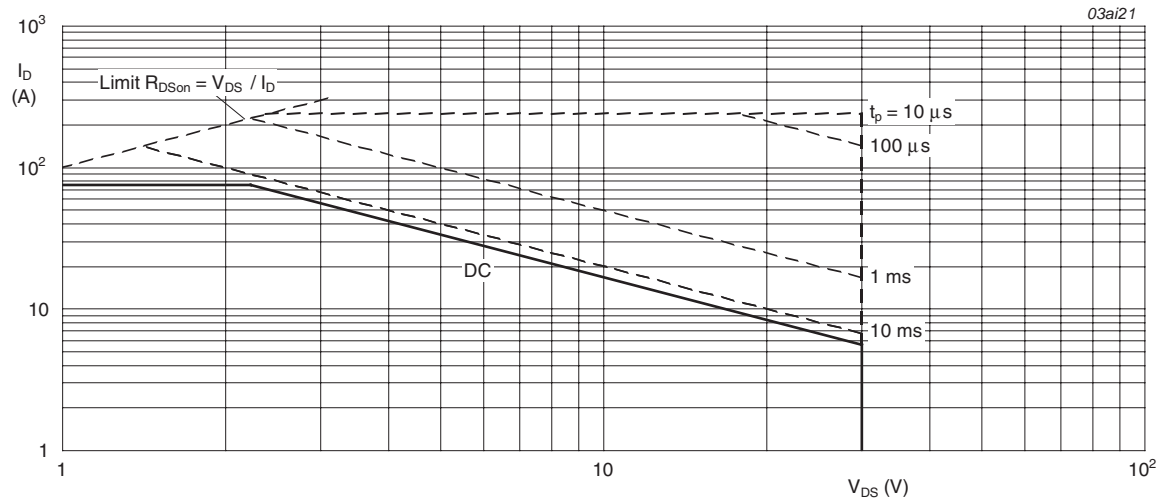
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 10V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.19	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	70	-	K/W

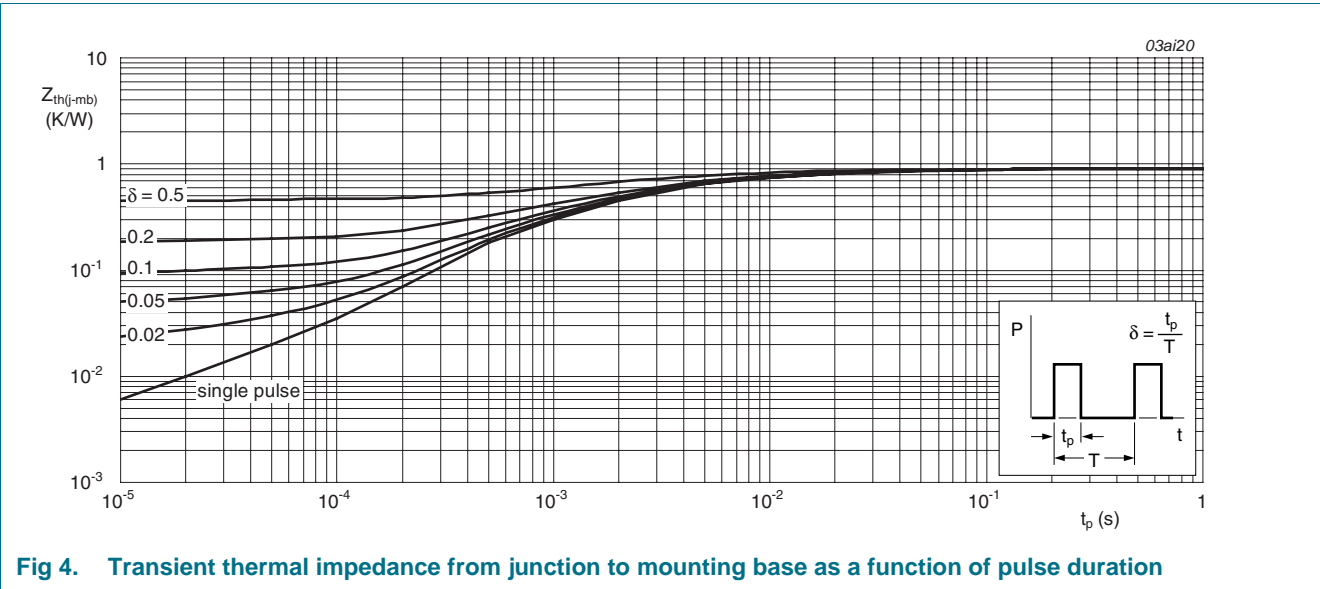
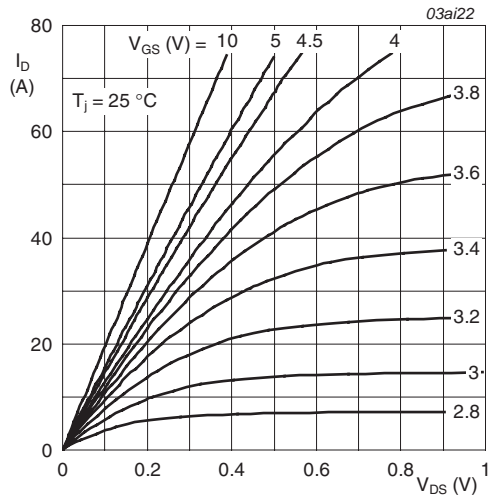


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

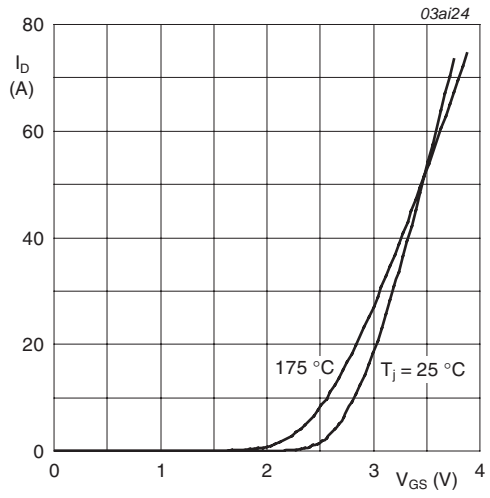
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	27	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 7 ; see Figure 8	-	-	2.9	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 7 ; see Figure 8	0.6	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 7 ; see Figure 8	1	1.9	2.5	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	1	μA
		V _{DS} = 30 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 9 ; see Figure 10	-	4.5	5.5	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; see Figure 9 ; see Figure 10	-	10.5	13.5	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; see Figure 9 ; see Figure 10	-	5.8	7.5	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 50 A; V _{DS} = 15 V; V _{GS} = 5 V; T _j = 25 °C; see Figure 11	-	23	-	nC
Q _{GS}	gate-source charge		-	10.5	-	nC
Q _{GD}	gate-drain charge		-	8	-	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 12	-	2180	-	pF
C _{oss}	output capacitance		-	600	-	pF
C _{rss}	reverse transfer capacitance		-	225	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; R _L = 0.6 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 5.6 Ω; T _j = 25 °C; I _D = 25 A	-	23	-	ns
t _r	rise time		-	90	-	ns
t _{d(off)}	turn-off delay time		-	37	-	ns
t _f	fall time		-	33	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 13	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V; T _j = 25 °C	-	37	-	ns
Q _r	recovered charge		-	33	-	nC



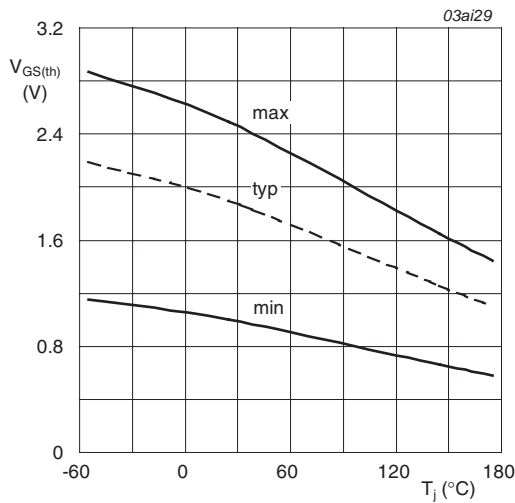
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



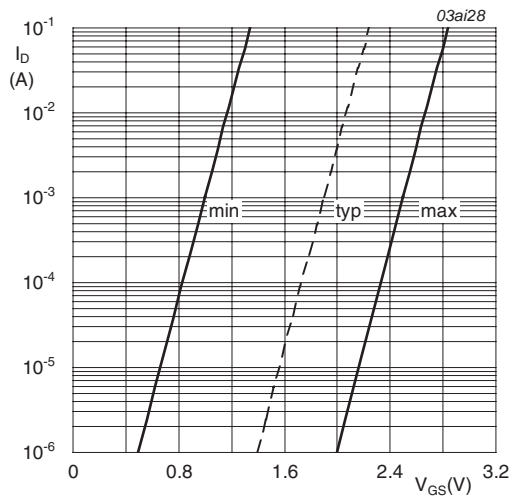
$T_j = 25\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



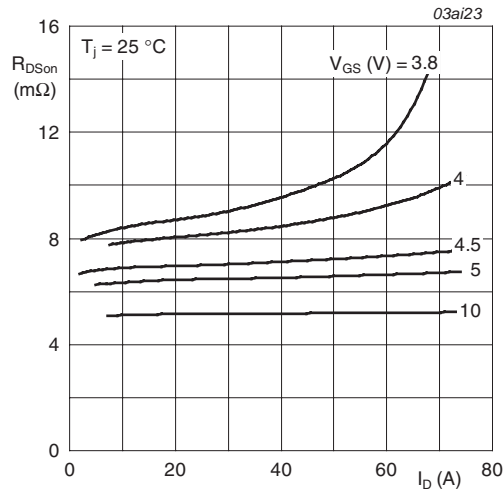
$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



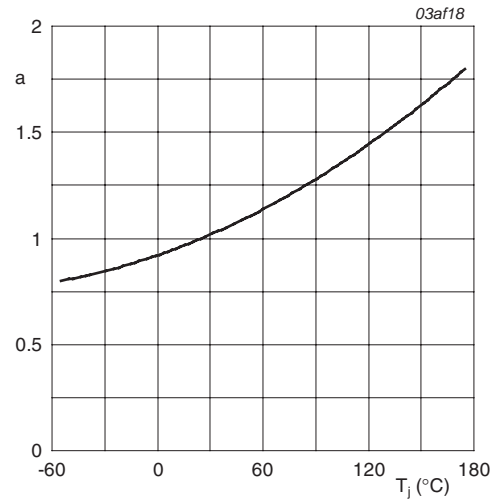
$T_j = 25\text{ }^\circ\text{C}$; $V_{DS} = 5\text{ V}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



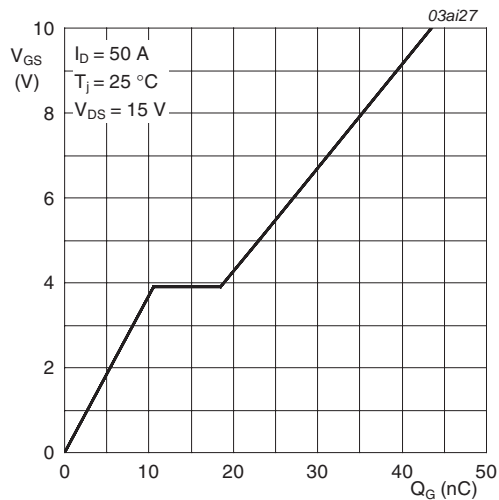
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



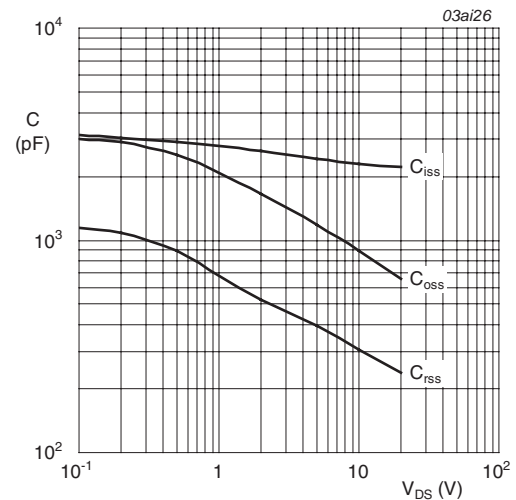
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^{\circ}\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



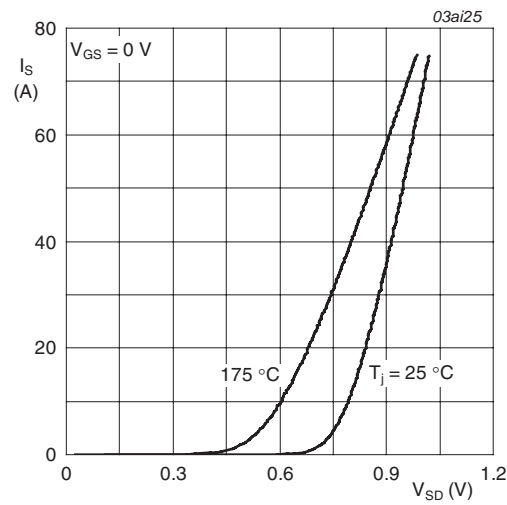
$I_D = 50\text{ A}; V_{DS} = 15\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ\text{C}$ and 175°C ; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended package (IPAK); 3 leads (in-line)

SOT533

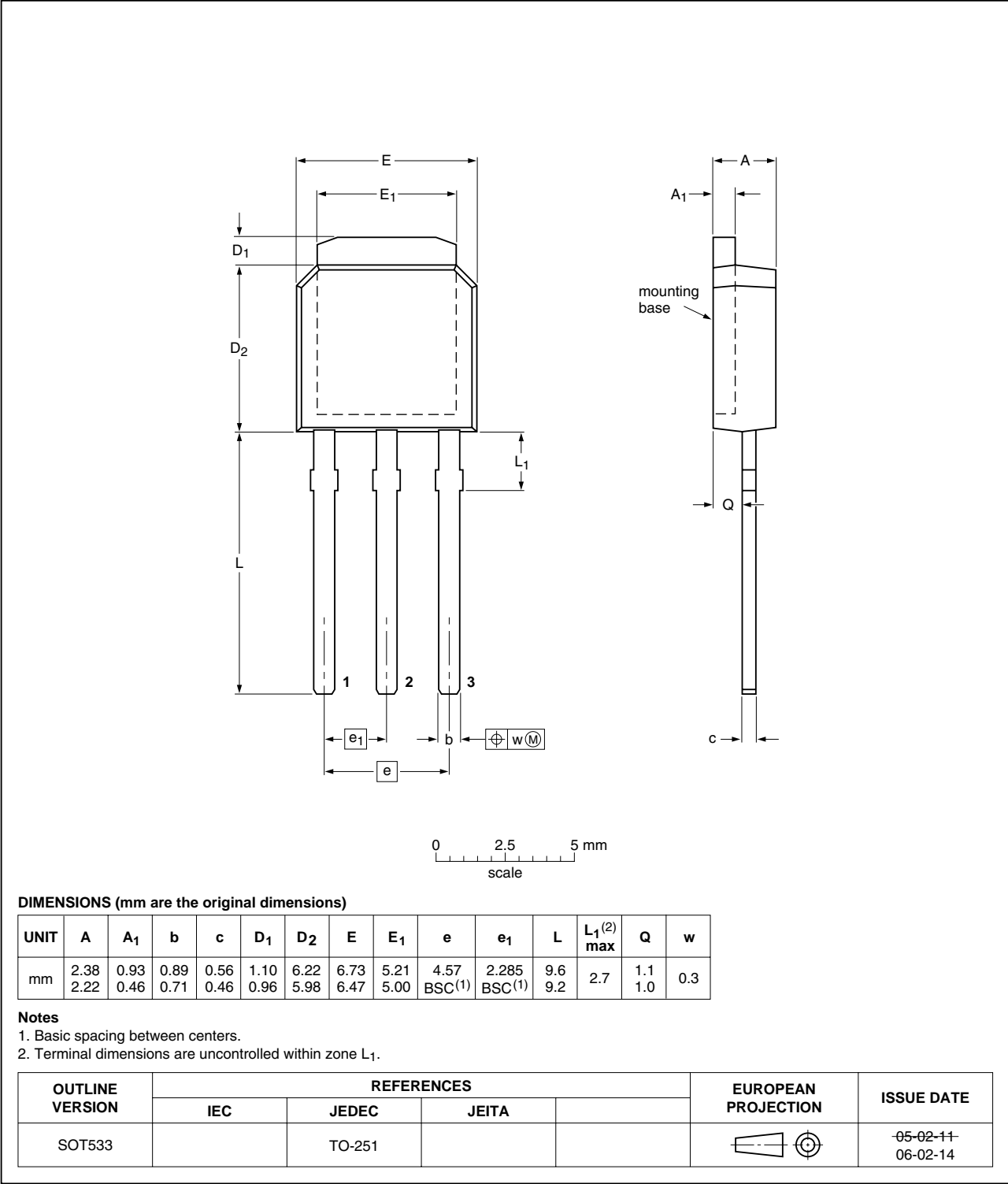


Fig 14. Package outline SOT533 (IPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHU101NQ03LT_4	20090630	Product data sheet	-	PHP_PHU101NQ03LT_3
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Type number PHU101NQ03LT separated from data sheet PHP_PHU101NQ03LT_3.			
PHP_PHU101NQ03LT_3	20051117	Product data sheet	CPC # 200309016	PHP_PHU101NQ03LT-02
PHP_PHU101NQ03LT-02 (9397 750 10927)	20030225	Product data	-	PHP_PHD_PHB_PHU101 NQ03LT-01
PHP_PHD_PHB_PHU101 NQ03LT-01 (9397 750 09307)	20020220	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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