

Octal Buffer/Line Driver with 3-STATE Outputs

74VHCT245A

General Description

The VHCT245A is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHCT245A is intended for bidirectional asynchronous communication between data busses. The direction of data transmission is determined by the level of the T/R input. The enable input can be used to disable the device so that the busses are effectively isolated.

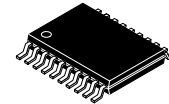
Protection circuits ensure that 0 V to 5.5 V can be applied to the input and output⁽¹⁾ pins without regard to the supply voltage. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up.

NOTE:

1. Outputs in OFF-State

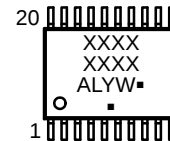
Features

- High Speed: $t_{PD} = 5.4 \text{ ns}$ (Typ) at $V_{CC} = 5 \text{ V}$
- Power Down Protection on Inputs and Outputs
- Low Power Dissipation: $I_{CC} = 4 \mu\text{A}$ (Max) @ $T_A = 25^\circ\text{C}$
- Pin and Function Compatible with 74HCT245
- This is a Pb-Free Device



TSSOP20, 4.4x6.5
CASE 948AQ

MARKING DIAGRAM



XXXXXX = Specific Device Code

A = Assembly Location

L = Wafer Lot

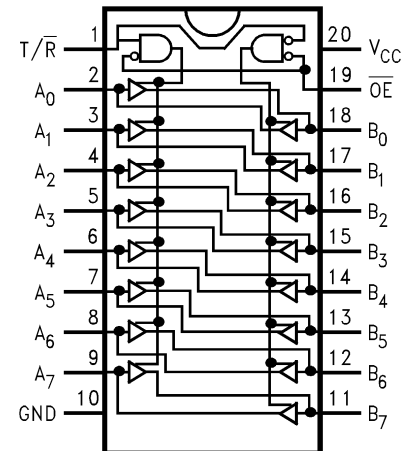
Y = Year

W = Work Week

■ = Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0 – A_7	Side A Inputs or 3-STATE Outputs
B_0 – B_7	Side B Inputs or 3-STATE Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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Logic Symbol

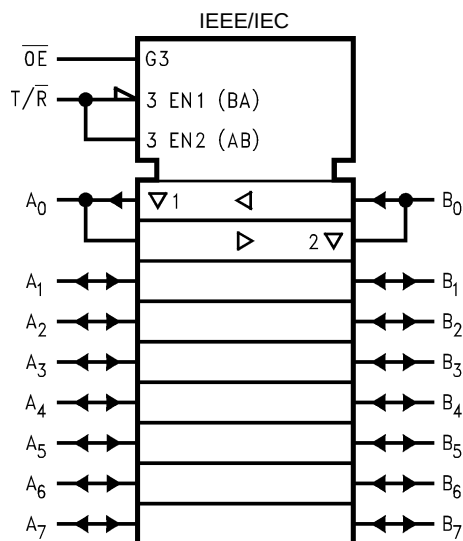


Figure 1. Logic Symbol

TRUTH TABLE

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +6.5	V
V _{IN}	DC Input Voltage		-0.5 to +6.5	V
V _{OUT}	DC Output Voltage	Active Mode (High or Low State)	-0.5 to V _{CC} + 0.5	V
		Tristate Mode (Note 2)	-0.5 to +6.5	
		Power-Off Mode (V _{CC} = 0 V)	-0.5 to +6.5	
I _{IN}	DC Input Current, per Pin		±20	mA
I _{OUT}	DC Output Current, per Pin		±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins		±75	mA
I _{IK}	Input Clamp Current		-20	mA
I _{OK}	Output Clamp Current		-20	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T _J	Junction Temperature Under Bias		+150	°C
θ _{JA}	Thermal Resistance (Note 3)		150	°C/W
P _D	Power Dissipation in Still Air at 25°C		833	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.245 in	
V _{ESD}	ESD Withstand Voltage (Note 4)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Applicable to devices with outputs that may be tri-stated.

3. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.

4. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage		4.5	5.5	V
V _{IN}	DC Input Voltage (Note 5)		0	5.5	V
V _{OUT}	DC Output Voltage (Note 5)	Active Mode (High or Low State)	0	V _{CC}	V
		Tristate Mode	0	5.5	
		Power-Off Mode (V _{CC} = 0 V)	0	5.5	
T _A	Operating Temperature		-40	+85	°C
t _r , t _f	Input Rise or Fall Rate	V _{CC} = 4.5 V to 5.5 V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C			T _A = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		4.5	2.0	–	–	2.0	–	V
			5.5	2.0	–	–	2.0	–	
V _{IL}	LOW Level Input Voltage		4.5	–	–	0.8	–	0.8	V
			5.5	–	–	0.8	–	0.8	
V _{OH}	HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = –50 µA I _{OH} = –8 mA	4.5	4.40	4.50	–	4.40	–	V
				3.94	–	–	3.80	–	
V _{OL}	LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 µA I _{OL} = 8 mA	4.5	–	0.0	0.1	–	0.1	V
				–	–	0.36	–	0.44	
I _{OZ}	3-STATE Output Off-State Current	V _{IN} = V _{IH} or V _{IL} ; V _{OUT} = V _{CC} or GND	5.5	–	–	±0.25	–	±2.5	µA
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0–5.5	–	–	±0.1	–	±1.0	µA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	–	–	4.0	–	40.0	µA
I _{CCT}	Maximum I _{CC} /Input	V _{IN} = 3.4 V, Other Input = V _{CC} or GND	5.5	–	–	1.35	–	1.50	mA
I _{OFF}	Output Leakage Current (Power Down State)	V _{OUT} = 5.5 V	0.0	–	–	0.5	–	5.0	µA

NOISE CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		Unit
				Typ	Limits	
V _{OLP} (Note 6)	Quiet Output Maximum Dynamic V _{OL}	C _L = 50 pF	5.0	1.2	1.6	V
V _{OLV} (Note 6)	Quiet Output Minimum Dynamic V _{OL}	C _L = 50 pF	5.0	–1.2	–1.6	V
V _{IHD} (Note 6)	Minimum HIGH Level Dynamic Input Voltage	C _L = 50 pF	5.0	–	2.0	V
V _{ILD} (Note 6)	Maximum LOW Level Dynamic Input Voltage	C _L = 50 pF	5.0	–	0.8	V

6. Parameter guaranteed by design.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V _{CC} (V)	T _A = 25°C			T _A = -40°C to +85°C		Unit
					Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay Time		C _L = 15 pF	5.0 ±0.5	–	4.9	7.7	1.0	8.5	ns
			C _L = 50 pF		–	5.4	8.7	1.0	9.5	
t _{PZL} , t _{PZH}	3-STATE Output Enable Time	R _L = 1 kΩ	C _L = 15 pF	5.0 ±0.5	–	9.4	13.8	1.0	15.0	ns
			C _L = 50 pF		–	9.9	14.8	1.0	16.0	
t _{PLZ} , t _{PHZ}	3-STATE Output Disable Time	R _L = 1 kΩ	C _L = 50 pF	5.0 ±0.5	–	10.1	15.4	1.0	16.5	ns
t _{OSLH} , t _{OSHL}	Output to Output Skew	(Note 7)		5.0 ±0.5	–	–	1.0	–	1.0	ns
C _{IN}	Input Capacitance	V _{CC} = Open			–	4	10	–	10	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.0 V			–	13	–	–	–	pF
C _{PD}	Power Dissipation Capacitance	(Note 8)			–	16	–	–	–	pF

7. Parameter guaranteed by design. t_{OSLH} = |t_{PLH} max – t_{PLH} min|; t_{OSHL} = |t_{PHL} max – t_{PHL} min|

8. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (Opr.) = C_{PD} · V_{CC} · f_{IN} + I_{CC} / 8 (per F/F). The total C_{PD} when n pcs. of the Octal D Flip-Flop operates can be calculated by the equation: C_{PD} (total) = 20 + 12n

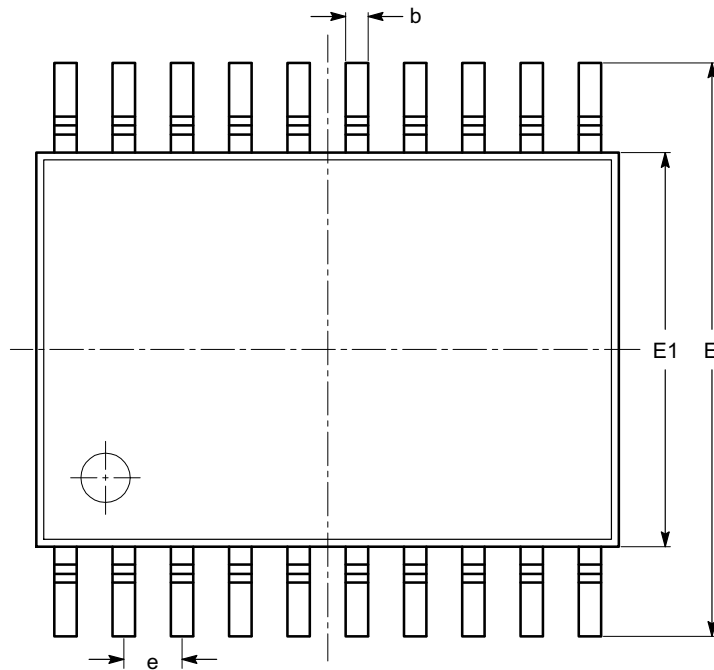
ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
74VHCT245AMTCX	VHCT 245A	TSSOP20 (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

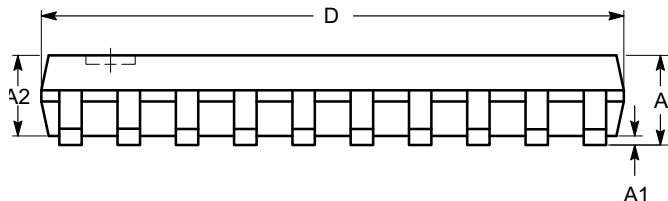
TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

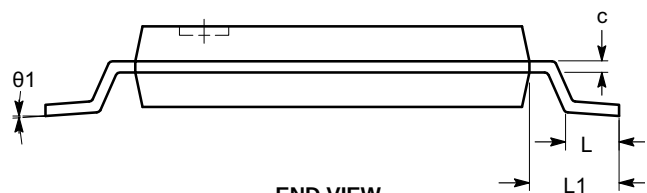


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°		8°



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

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