

74LCX374

Low Voltage Octal D-Type Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The LCX374 consists of eight D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops. The LCX374 is designed for low voltage (3.3V or 2.5V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 8.5 ns t_{PD} max ($V_{CC} = 3.3V$), 10 μA I_{CC} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human Body Model > 2000V
 - Machine Model > 200V

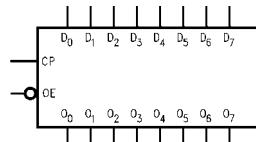
Note 1: To ensure the high-impedance state during power up or down, \overline{OE} should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

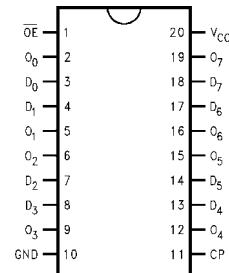
Order Number	Package Number	Package Description
74LCX374VM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX374MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
D_0 – D_7	Data Inputs
CP	Clock Pulse Input
\overline{OE}	Output Enable Input
O_0 – O_7	3-STATE Outputs

Functional Description

The LCX374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	\overline{OE}	O_n
H	✓	L	H
L	✓	L	L
X	L	L	O_0
X	X	H	Z

H = HIGH Voltage Level

L = LOW Voltage Level

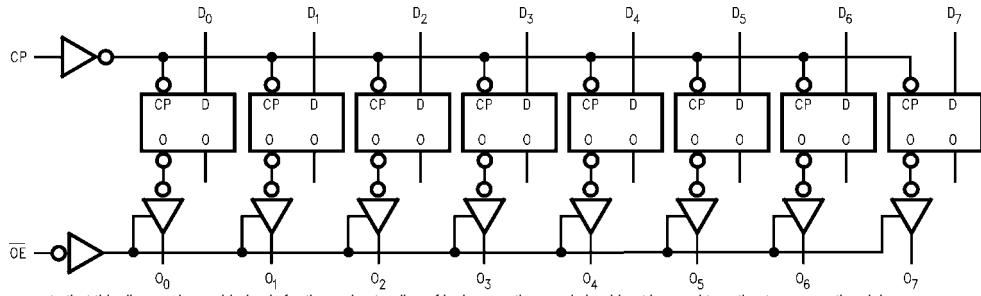
X = Immaterial

Z = High Impedance

✓ = LOW-to-HIGH Transition

O_0 = Previous O_0 before HIGH-to-LOW of CP

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0 −0.5 to V_{CC} + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 3)	V
I_{IK}	DC Input Diode Current	−50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	−50 +50	$V_O < GND$ $V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	V
		Data Retention	1.5	3.6
V_I	Input Voltage	0	5.5	V
V_O	Output Voltage	HIGH or LOW State 3-STATE	0 0	V_{CC} 5.5
I_{OH}/I_{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$ $V_{CC} = 2.7V - 3.0V$ $V_{CC} = 2.3V - 2.7V$	±24 ±12 ±8	mA
T_A	Free-Air Operating Temperature	−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$, $V_{CC} = 3.0V$	0	10	ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs or I_O s must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7 2.7 – 3.6	1.7 2.0		V
V_{IL}	LOW Level Input Voltage		2.3 – 2.7 2.7 – 3.6		0.7 0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu\text{A}$	2.3 – 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -8 \text{ mA}$	2.3	1.8		
		$I_{OH} = -12 \text{ mA}$	2.7	2.2		
		$I_{OH} = -18 \text{ mA}$	3.0	2.4		
		$I_{OH} = -24 \text{ mA}$	3.0	2.2		
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu\text{A}$	2.3 – 3.6		0.2	V
		$I_{OL} = 8 \text{ mA}$	2.3		0.6	
		$I_{OL} = 12 \text{ mA}$	2.7		0.4	
		$I_{OL} = 16 \text{ mA}$	3.0		0.4	
		$I_{OL} = 24 \text{ mA}$	3.0		0.55	
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5\text{V}$	2.3 – 3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 5.5\text{V}$ $V_I = V_{IH}$ or V_{IL}	2.3 – 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5\text{V}$	0		10	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6		10	μA
		3.6V ≤ V _I , V _O ≤ 5.5V (Note 5)	2.3 – 3.6		±10	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} – 0.6V	2.3 – 3.6		500	μA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500 Ω						Units	
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5 ± 0.2			
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF			
		Min	Max	Min	Max	Min	Max		
f _{MAX}	Maximum Clock Frequency	150		150		150		MHz	
t _{PHL}	Propagation Delay CP to O _n	1.5	8.5	1.5	9.5	1.5	10.5	ns	
t _{PLH}		1.5	8.5	1.5	9.5	1.5	10.5	ns	
t _{PZL}	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns	
t _{PZH}		1.5	8.5	1.5	9.5	1.5	10.5	ns	
t _{PLZ}	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns	
t _{PHZ}		1.5	7.5	1.5	8.5	1.5	9.0	ns	
t _S	Setup Time	2.5		2.5		4.0		ns	
t _H	Hold Time	1.5		1.5		2.0		ns	
t _W	Pulse Width	3.3		3.3		4.0		ns	
t _{OSHL}	Output to Output Skew (Note 6)			1.0				ns	
t _{OSLH}				1.0				ns	

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		Units
				Typical		
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8		V
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	0.6		
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	-0.8		V
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	-0.6		

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	25	pF

AC LOADING and WAVEFORMS Generic for LCX Family

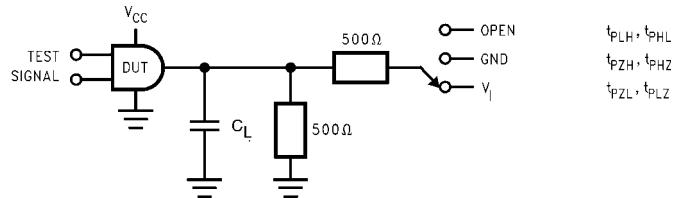
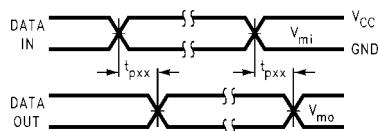
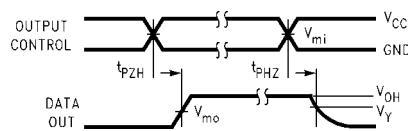


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

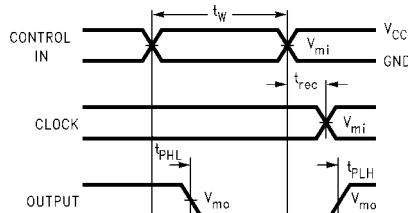
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND



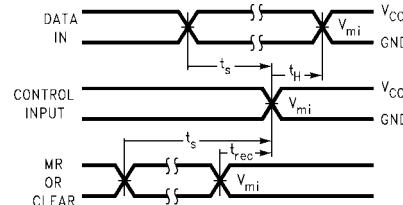
Waveform for Inverting and Non-Inverting Functions



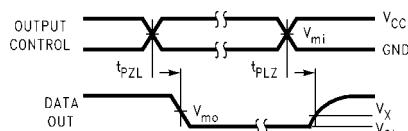
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

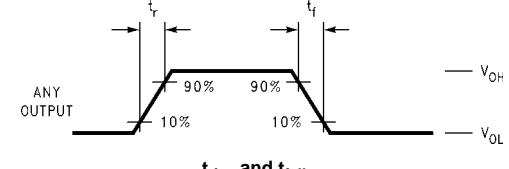
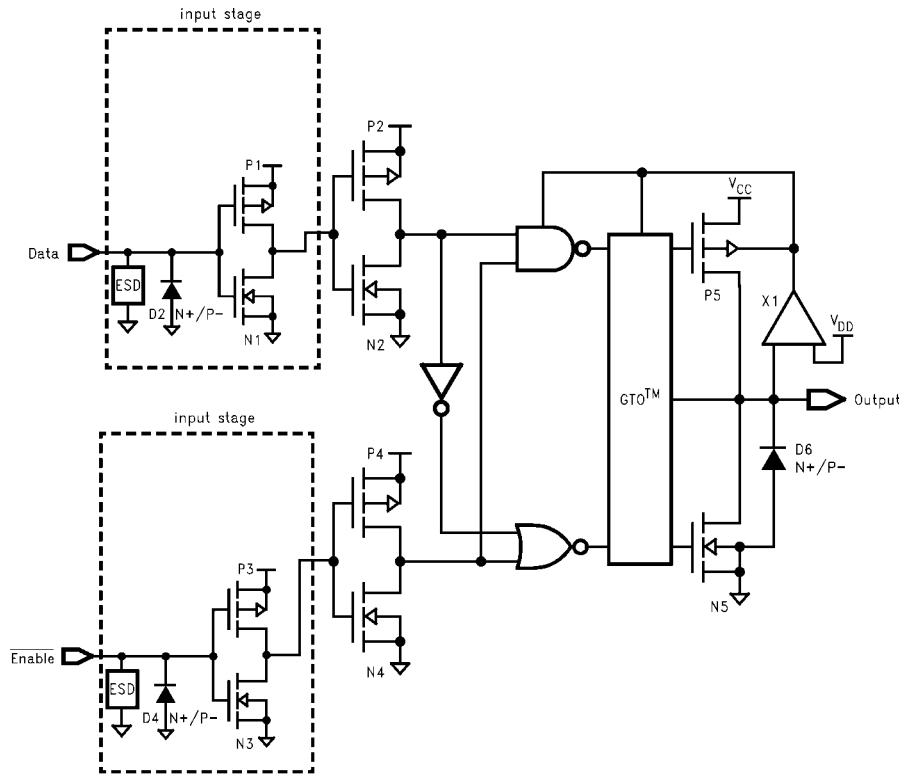
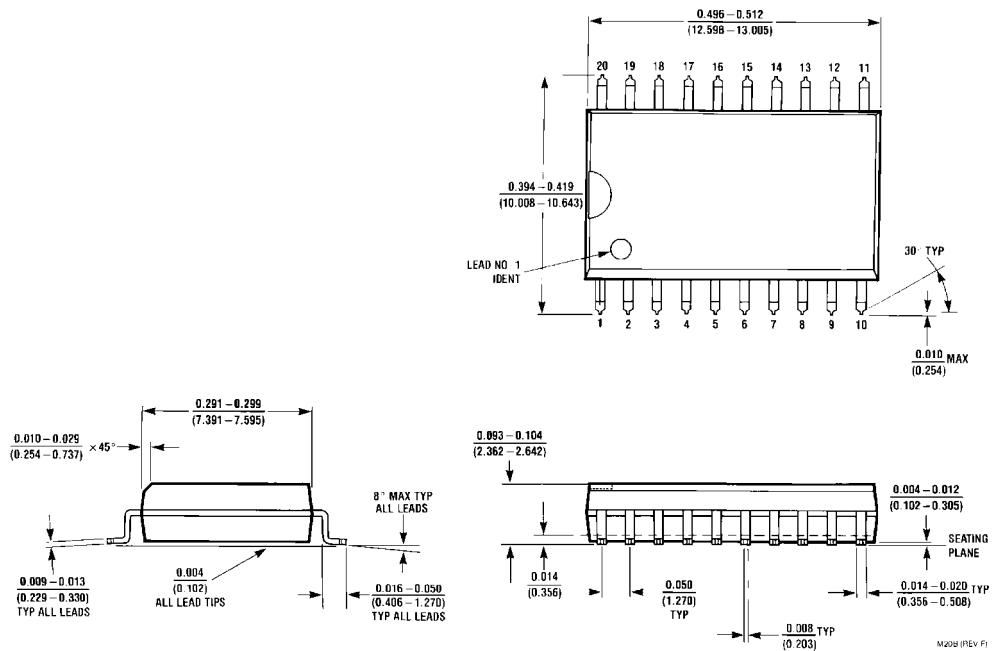


FIGURE 2. Waveforms
(Input Characteristics; $f = 1MHz$, $t_r = t_f = 3ns$)

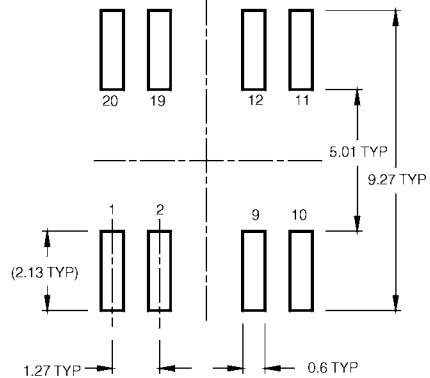
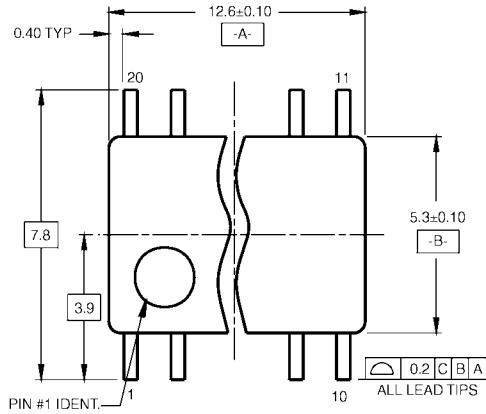
Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

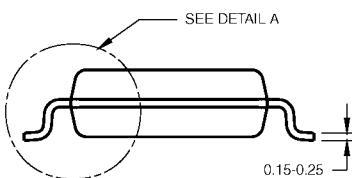
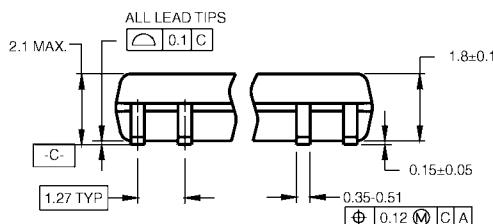
Physical Dimensions inches (millimeters) unless otherwise noted

20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

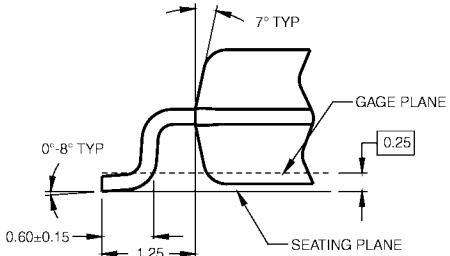


DIMENSIONS ARE IN MILLIMETERS

NOTES:

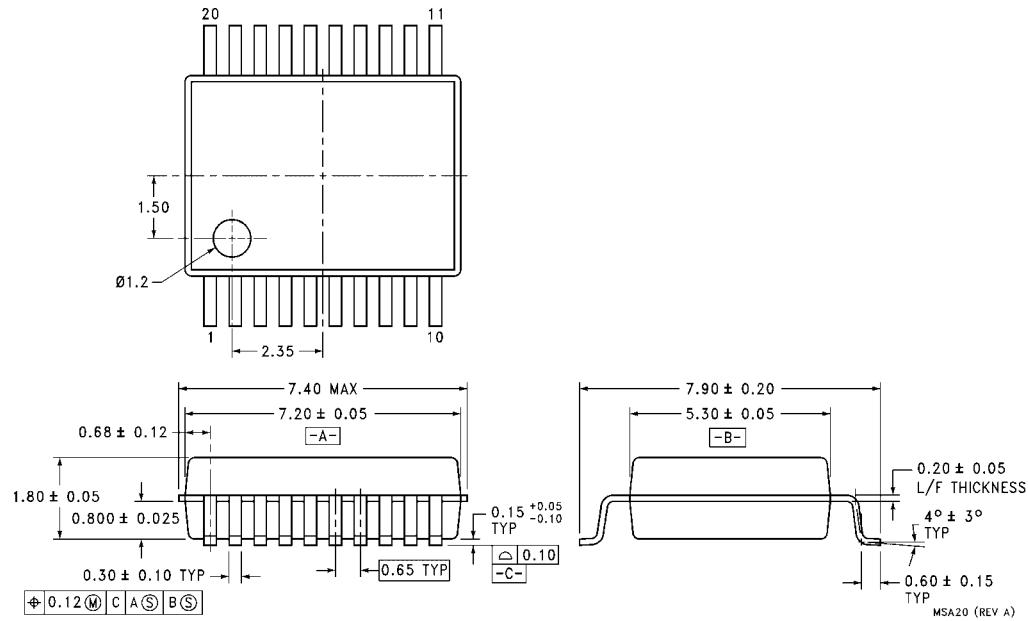
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

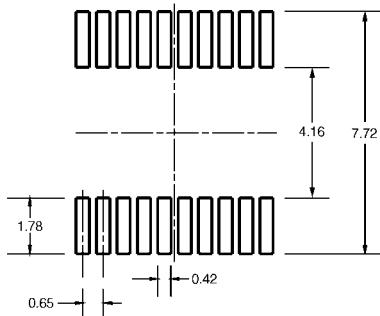
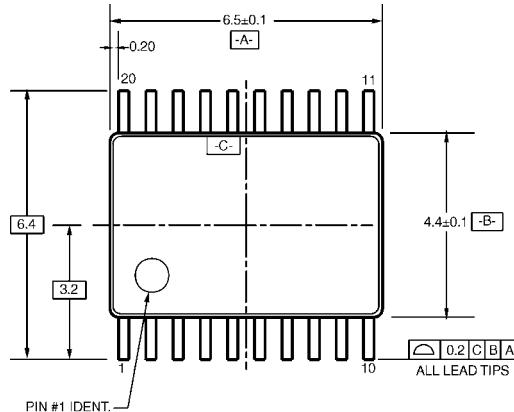


DETAIL A

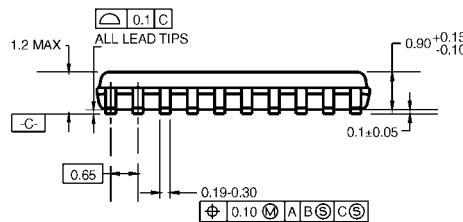
**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

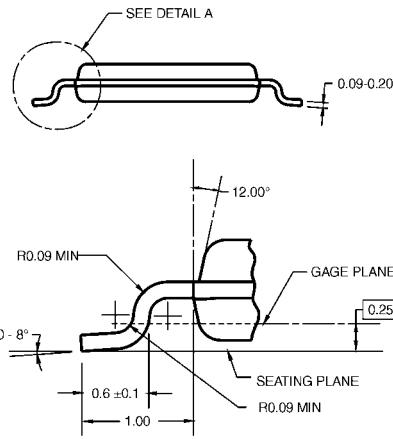


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1



DETAIL A

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com