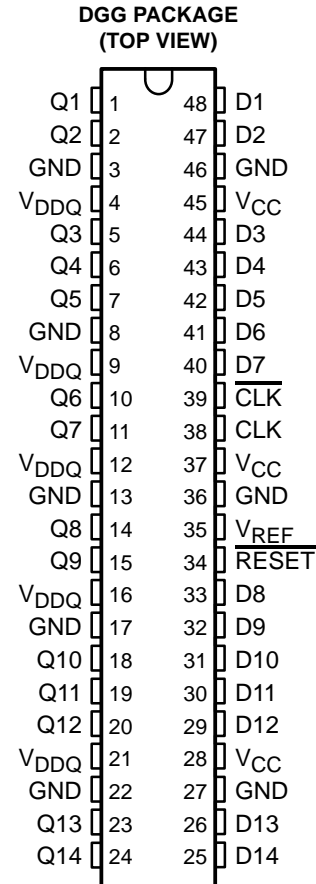# SN74SSTVF16857
14-BIT REGISTERED BUFFER
WITH SSTL_2 INPUTS AND OUTPUTS

SCES411B – AUGUST 2002 – REVISED APRIL 2003

- Member of the Texas Instruments Widebus™ Family
- Operates at 2.3 V to 2.7 V for PC1600, PC2100, and PC2700; 2.5 V to 2.7 V for PC3200
- Pinout and Functionality Compatible With JEDEC Standard SSTV16857
- 600 ps Faster (Simultaneous Switching) Than JEDEC Standard SSTV16857 in PC2700 DIMM Applications
- Output Edge-Control Circuitry Minimizes Switching Noise in Unterminated DIMM Load
- Outputs Meet SSTL_2 Class I Specifications
- Supports SSTL_2 Data Inputs
- Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs
- Supports LVCMOS Switching Levels on the $\overline{\text{RESET}}$ Input
- $\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DGG PACKAGE
(TOP VIEW)

Q1	1	48	D1
Q2	2	47	D2
GND	3	46	GND
V_{DDQ}	4	45	V_{CC}
Q3	5	44	D3
Q4	6	43	D4
Q5	7	42	D5
GND	8	41	D6
V_{DDQ}	9	40	D7
Q6	10	39	$\overline{\text{CLK}}$
Q7	11	38	CLK
V_{DDQ}	12	37	V_{CC}
GND	13	36	GND
Q8	14	35	V_{REF}
Q9	15	34	$\overline{\text{RESET}}$
V_{DDQ}	16	33	D8
GND	17	32	D9
Q10	18	31	D10
Q11	19	30	D11
Q12	20	29	D12
V_{DDQ}	21	28	V_{CC}
GND	22	27	GND
Q13	23	26	D13
Q14	24	25	D14

description/ordering information

This 14-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are edge-controlled circuits optimized for unterminated DIMM loads and meet SSTL_2 Class I specifications.

The SN74SSTVF16857 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TSSOP – DGG	Tape and reel	SN74SSTVF16857GR	SSTVF16857

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

## description/ordering information (continued)

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X, or floating	X, or floating	X, or floating	L

logic diagram (positive logic)

To 13 Other Channels
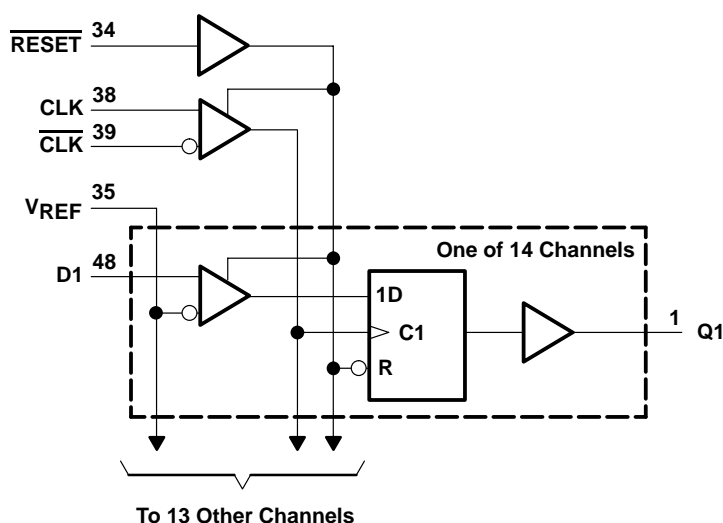
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} or V_{DDQ} . . . . –0.5 V to 3.6 V

Input voltage range, V_I (see Notes 1 and 2) . . . . –0.5 V to V_{CC} + 0.5 V

Output voltage range, V_O (see Notes 1 and 2) . . . . –0.5 V to V_{DDQ} + 0.5 V

Input clamp current, I_{IK} (V_I < 0) . . . . –50 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDQ}) . . . . ±50 mA

Continuous output current, I_O (V_O = 0 to V_{DDQ}) . . . . ±50 mA

Continuous current through each V_{CC}, V_{DDQ}, or GND . . . . ±100 mA

Package thermal impedance, θ_{JA} (see Note 3) . . . . 70°C/W

Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage	PC1600, PC2100, PC2700	2.3		2.7	V
		PC3200	2.5		2.7	
V_{REF}	Reference voltage (V_{REF} = V_{DDQ}/2)	PC1600, PC2100, PC2700	1.15	1.25	1.35	V
		PC3200	1.25	1.3	1.35	
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs	V_{REF}+310mV			V
V_{IL}	AC low-level input voltage	Data inputs			V_{REF}−310mV	V
V_{IH}	DC high-level input voltage	Data inputs	V_{REF}+150mV			V
V_{IL}	DC low-level input voltage	Data inputs			V_{REF}−150mV	V
V_{IH}	High-level input voltage	$\overline{\text{RESET}}$	1.7			V
V_{IL}	Low-level input voltage	$\overline{\text{RESET}}$			0.7	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{\text{CLK}}$	0.97		1.53	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{\text{CLK}}$	360			mV
I_{OH}	High-level output current				−16	mA
I_{OL}	Low-level output current				16	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 4: The $\overline{\text{RESET}}$ input of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{\text{RESET}}$ is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS INSTRUMENTS

electrical characteristics for PC1600, PC2100, and PC2700 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC} AND V_{DDQ}	MIN	TYP†	MAX	UNIT
V_{IK}		I_I = −18 mA		2.3 V			−1.2	V
V_{OH}		I_{OH} = −100 µA		2.3 V to 2.7 V	V_{DDQ}−0.2			V
		I_{OH} = −8 mA		2.3 V	1.95			
V_{OL}		I_{OL} = 100 µA		2.3 V to 2.7 V			0.2	V
		I_{OL} = 8 mA		2.3 V			0.35	
I_I	All inputs	V_I = V_{CC} or GND		2.7 V			±5	µA
I_{CC}	Static standby	$\overline{RESET}$ = GND	I_O = 0	2.7 V			10	µA
	Static operating	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$				8	25	mA
I_{CCD}	Dynamic operating – clock only	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	I_O = 0	2.5 V		28		µA/ MHz
	Dynamic operating – per each data input	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				7		µA/ clock MHz/ D input
C_i	Data inputs	V_I = V_{REF} ± 310 mV		2.5 V	2.5	3	3.5	pF
	CLK, $\overline{CLK}$	V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360mV			2.5	3	3.5	
	$\overline{RESET}$	V_I = V_{CC} or GND			2.3	3	3.5	

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

electrical characteristics for PC3200 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC} AND V_{DDQ}	MIN	TYP†	MAX	UNIT
V_{IK}		I_I = −18 mA		2.5 V			−1.2	V
V_{OH}		I_{OH} = −100 µA		2.5 V to 2.7 V	V_{DDQ}−0.2			V
		I_{OH} = −8 mA		2.5 V	1.95			
V_{OL}		I_{OL} = 100 µA		2.5 V to 2.7 V			0.2	V
		I_{OL} = 8 mA		2.5 V			0.35	
I_I	All inputs	V_I = V_{CC} or GND		2.7 V			±5	µA
I_{CC}	Static standby	$\overline{RESET}$ = GND	I_O = 0	2.7 V			10	µA
	Static operating	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$				8	25	mA
I_{CCD}	Dynamic operating – clock only	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	I_O = 0	2.6 V		28		µA/ MHz
	Dynamic operating – per each data input	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				7		µA/ clock MHz/ D input
C_i	Data inputs	V_I = V_{REF} ± 310 mV		2.6 V	2.5	3	3.5	pF
	CLK, $\overline{CLK}$	V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360mV			2.5	3	3.5	
	$\overline{RESET}$	V_I = V_{CC} or GND			2.3	3	3.5	

† All typical values are at V_{CC} = 2.6 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V_{CC} = 2.5 V ± 0.2 V†		V_{CC} = 2.6 V ± 0.1 V†		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				250		250	MHz
t_w	Pulse duration, CLK, $\overline{CLK}$ high or low			2		2		ns
t_{act}	Differential inputs active time (see Note 5)				22		22	ns
t_{inact}	Differential inputs inactive time (see Note 6)				22		22	ns
t_{su}	Setup time	Fast slew rate (see Notes 7 and 9)	Data before CLK↑, $\overline{CLK}$↓	0.75		0.75		ns
		Slow slew rate (see Notes 8 and 9)		0.9		0.9		
t_h	Hold time	Fast slew rate (see Notes 7 and 9)	Data after CLK↑, $\overline{CLK}$↓	0.75		0.75		ns
		Slow slew rate (see Notes 8 and 9)		0.9		0.9		

† For this test condition, V_{DDQ} always is equal to V_{CC}.

NOTES: 5. V_{REF} must be held at a valid input level and data inputs must be held low for a minimum time of t_{act} max, after $\overline{RESET}$ is taken high.
   6. V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after $\overline{RESET}$ is taken low.
   7. For data signal input slew rate ≥1 V/ns.
   8. For data signal input slew rate ≥0.5 V/ns and <1 V/ns.
   9. CLK, $\overline{CLK}$ signals input slew rates are ≥1 V/ns.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V†		V_{CC} = 2.6 V ± 0.1 V†		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			250		250		MHz
t_{pd}‡	CLK and $\overline{CLK}$	Q	1.1	2.6	1.1	2.6	ns
t_{PHL}	$\overline{RESET}$	Q		5		5	ns

† For this test condition, V_{DDQ} always is equal to V_{CC}.

‡ Single bit switching

TEXAS INSTRUMENTS

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE AND CURRENT WAVEFORMS
INPUTS ACTIVE AND INACTIVE TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time with one transition per measurement.
E. $V_{REF} = V_{DDQ}/2$
F. $V_{IH} = V_{REF}$ + 310 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ – 310 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74SSTVF16857GR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SSTVF16857
SN74SSTVF16857GR.B	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SSTVF16857

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTVF16857GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTVF16857GR	TSSOP	DGG	48	2000	356.0	356.0	45.0

8.3
7.9 TYP

A

PIN 1 ID
AREA

1

46X 0.5

48

12.6
12.4
NOTE 3

2X
11.5

24

25

B

6.2
6.0

48X 0.27
0.17

⊕ 0.08Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

1.2
1.0

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL
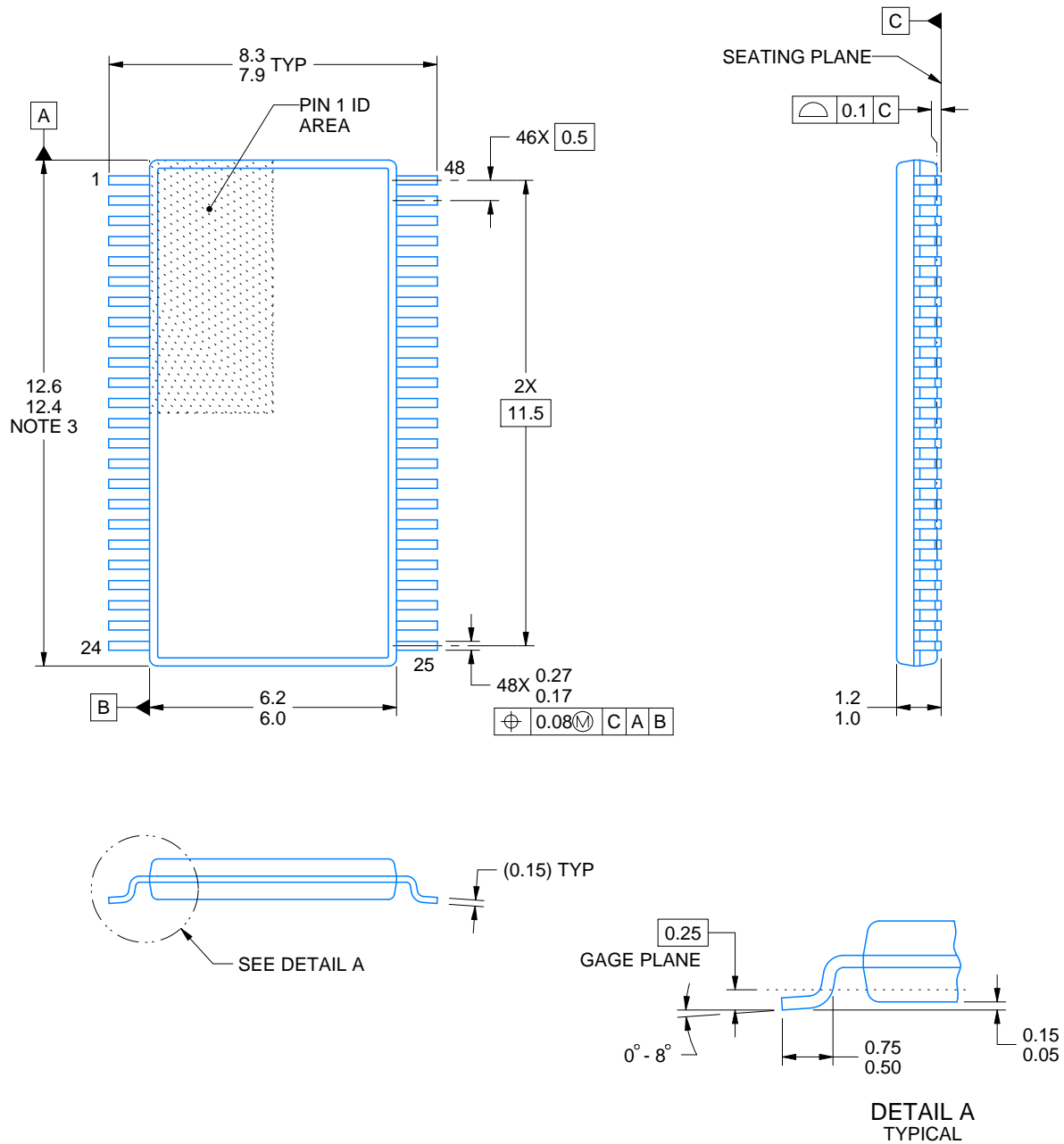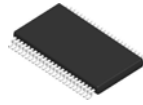
4214859/B   11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

DGG0048A

TSSOP - 1.2 mm max height

48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05)
TYP

SYMM ₵

48

SYMM ₵

24

25

(7.5)
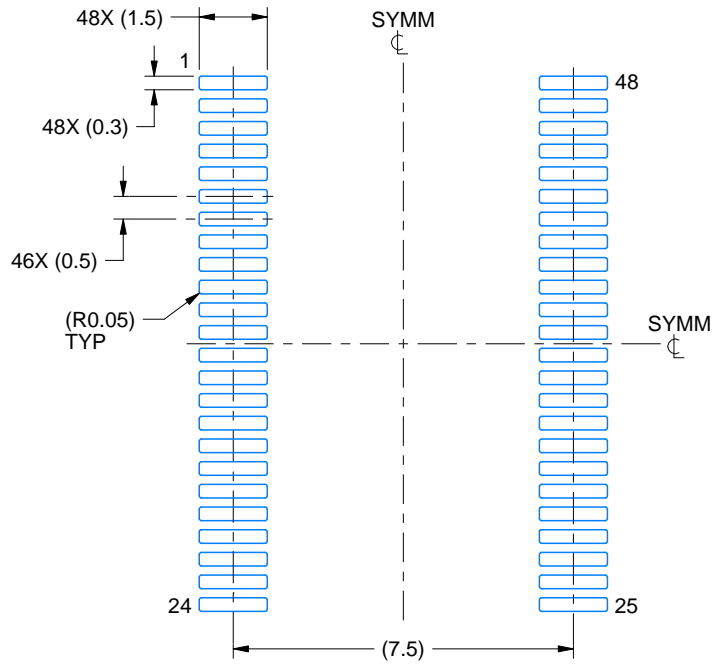
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

**NON SOLDER MASK
DEFINED**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

**SOLDER MASK
DEFINED**
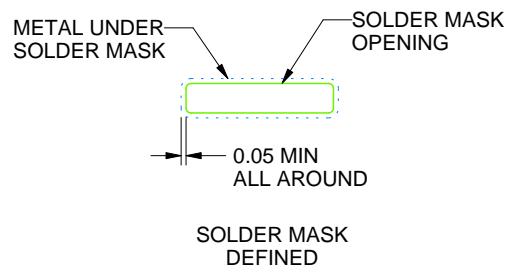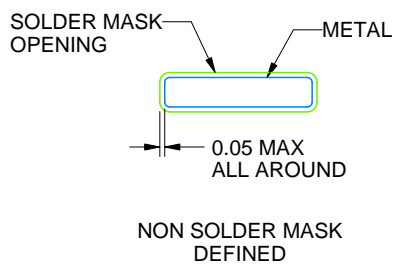
SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05) TYP

SYMM

SYMM

48

24

25

(7.5)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B   11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97
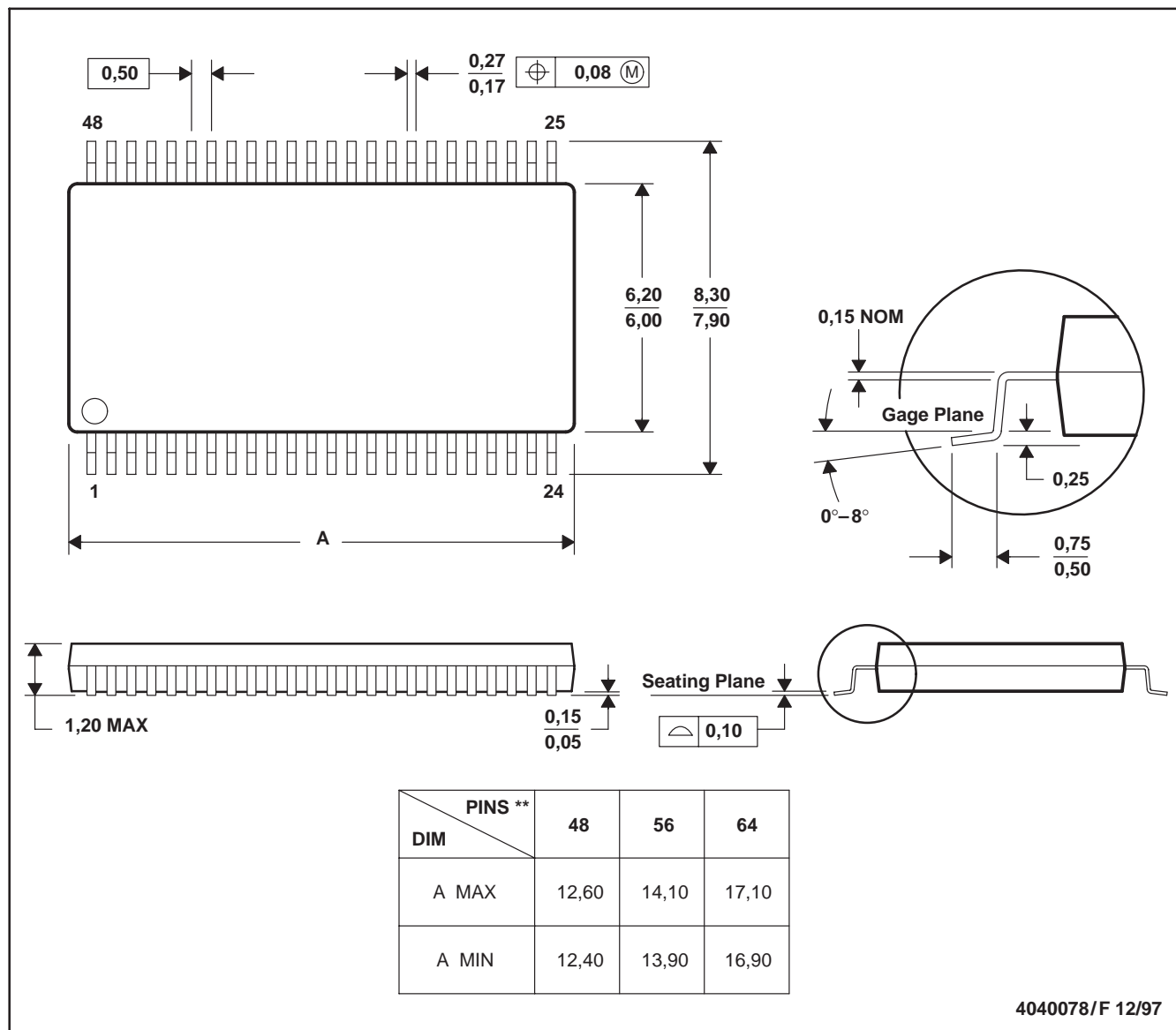
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

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