

## Features

- Bus LVDS Signaling (BLVDS)
- Designed for Double Termination Applications
- Balanced Output Impedance
- Light Bus Loading: 5pF typical
- Glitch-free power up/down (Driver Disabled)
- Operates from a 3.3V supply
- High Signaling Rate Capability: >100Mbps
- Driver:
  - $\pm 250\text{mV}$  Differential Swing into a  $27\Omega$  load
  - Propagation Delay of 1.5ns typ.
  - Low Voltage TTL (LVTTL) Inputs are 5V Tolerant
- Receiver:
  - Accepts  $\pm 50\text{mV}$  (min.) Differential Swing with up to 2.0V ground potential difference
  - Propagation Delay of 3.3ns typical
  - Low Voltage TTL (LVTTL) Outputs
  - Open, Short, and Terminated Fail Safe
- Bus terminal ESD exceeds 10kV
- Industrial Temperature Operation ( $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ )
- Packaging (Pb-free & Green available):
  - 8-lead SOIC (W)
  - 8-lead MSOP (U)

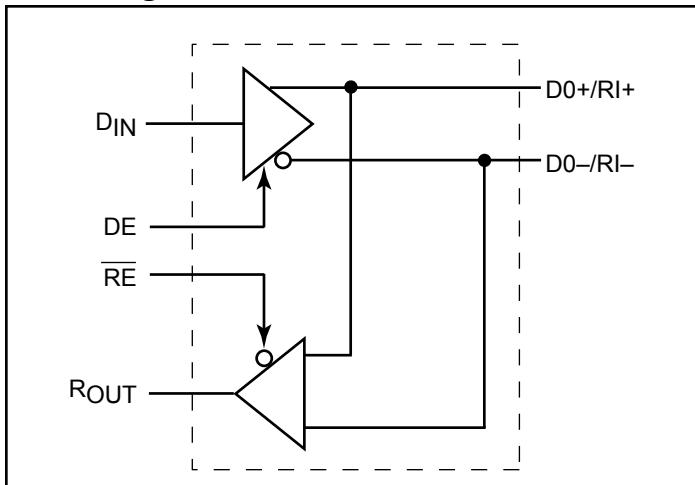
## Description

The PI90LVB010 is a differential line driver and receiver (transceiver) that is similar to the IEEE1596.3 SCI and ANSI/TIA/EIA-644LVDS standards, the difference is that the driver output current is higher. This modification enables true half-duplex operation with more than one LVDS driver or with two line transmission resistors over a  $50\Omega$  differential transmission line. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The logic interface provides maximum flexibility resulting from four separate lines that are provided:  $D_{IN}$ ,  $DE$ ,  $\overline{RE}$ , and  $ROUT$ .

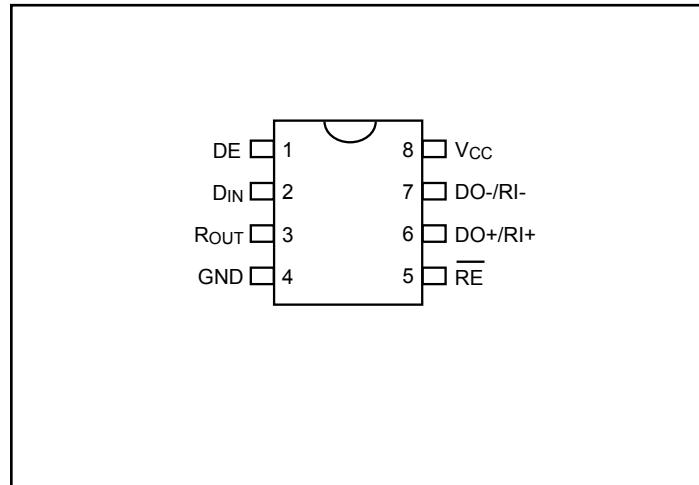
This device also features flow-through which allows easy PCB routing for short stubs between the bus pins and the connector. The driver has 10mA drive capability, allowing it to drive heavily loaded backplanes, with impedance as low as  $27\Omega$ .

The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high-speed operation, while consuming minimal power with reduced EMI. In addition the differential signaling provides common mode noise rejection of  $\pm 1V$ .

## Block Diagram



## Pin Configuration



**Absolute Maximum Ratings<sup>(1,2)</sup>**

Supply Voltage (V <sub>CC</sub> )	.....	6.0V
Enable Input Voltage (DE, $\overline{RE}$ )	.....	-0.3V to (V <sub>CC</sub> +0.3V)
Driver Input Voltage (DIN)	.....	-0.3V to (V <sub>CC</sub> +0.3V)
Receiver Output Voltage (ROUT)	.....	-0.3V to (V <sub>CC</sub> +0.3V)
Bus Pin Voltage (DO/RI $\pm$ )	.....	-0.3V to +3.9V
Driver Short Circuit	.....	Continuous
ESD (HBM 1.5k $\Omega$ , 100pF)	.....	>10kV
Maximum Package Power Dissipation at 20°C	.....	
SOIC	.....	1025mW
Derate SOIC Package	.....	8.2mW/°C

**Note:**

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Functional Mode**

Mode Select	DE	$\overline{RE}$
Driver Mode	H	H
Receiver Mode	L	L
3-State Mode	L	H
Loop Back Mode	H	L

Storage Temperature Range	.....	-65°C to +150°C
Lead Temperature Range (Soldering, 4s)	.....	+260°C

**Recommended Operating Conditions**

	Min.	Max.	Units
Supply Voltage (V <sub>CC</sub> )	3.0	3.6	V
Receiver Input Voltage	0.0	2.9	V
Operating Free-Air Temperature	-40	+85	°C

**Transmitter Mode**

Inputs		Outputs	
DE	DI	DO+	DO-
H	L	L	H
H	H	H	L
H	2 > & > 0.8	X	X
L	X	Z	Z
H	Open	L	H

**Receiver Mode**

Inputs		Outputs
$\overline{RE}$	(RE+) - (RI-)	ROUT
L	L (< -100mV)	L
L	H (> + 100mV)	H
L	100mV > & >-100mV	?
H	X	Z

**Notes:**

1. H = High, L = Low, Z = High Impedance, X = High or Low

**Pin Description**

Pin Name	Pin#	Inputs/Outputs	Description
D <sub>IN</sub>	2	I	TTL Driver Input
DO $\pm$ RI $\pm$	6, 7	I/O	LVDS Driver Outputs/ LVDS Receiver Inputs
ROUT	3	O	TTL Receiver Outputs
$\overline{RE}$	5	I	Receiver Enable TTL Input (Active Low)
DE	1	I	Driver Enable TTL Input (Active High)
GND	4	NA	Ground
V <sub>CC</sub>	8	NA	Power Supply

**DC Electrical Characteristics<sup>(2,3)</sup>** (T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. V<sub>CC</sub> = 3.3V ±0.3V)

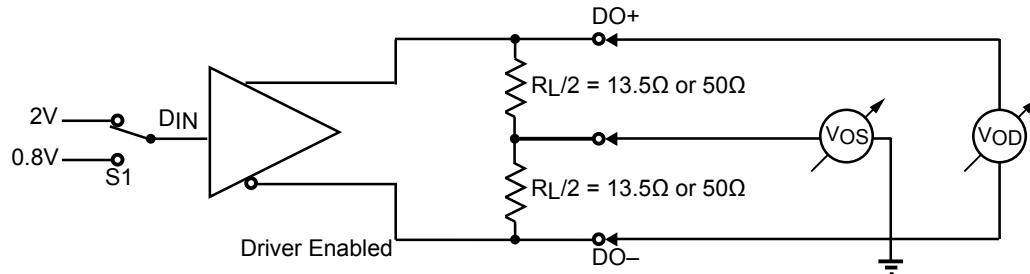
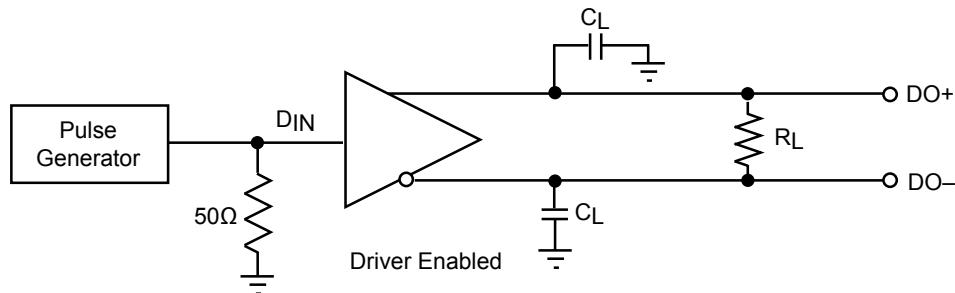
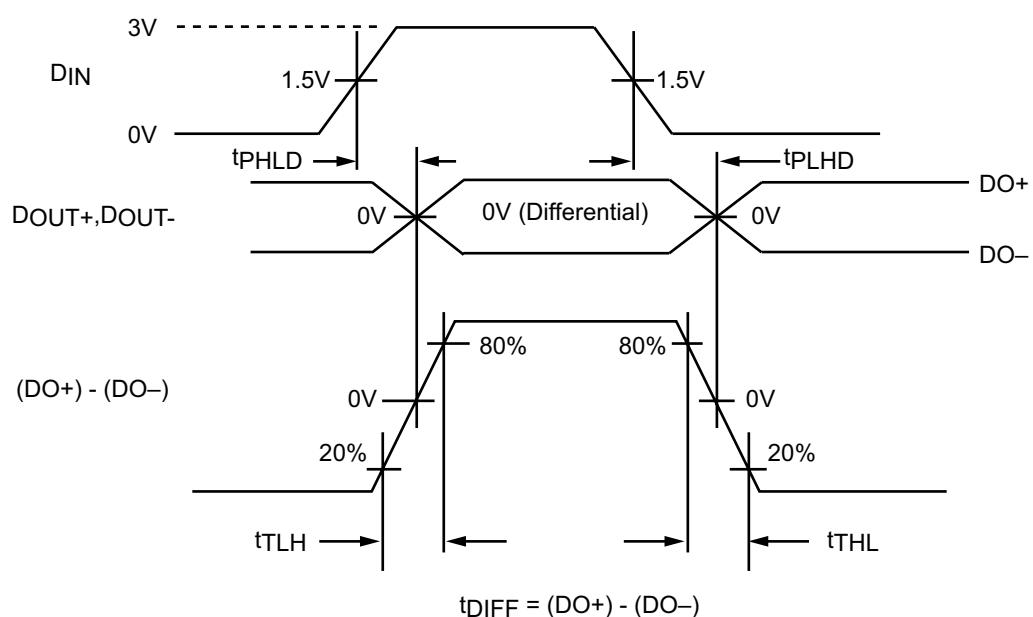
Symbol	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Units
V <sub>OD</sub>	Output Differential Voltage	R <sub>L</sub> = 27Ω, See figure 1	DO+/RI+ DO-/RI-	140	250	360	mV
ΔV <sub>OD</sub>	V <sub>OD</sub> Magnitude Change				3	30	
V <sub>OS</sub>	Offset Voltage			1	1.25	1.65	V
ΔV <sub>OS</sub>	Offset Magnitude Change				5	50	mV
I <sub>OSD</sub>	Output Short Circuit Current	V <sub>O</sub> = 0V, DE = V <sub>CC</sub>			-12	-20	mA
V <sub>OH</sub>	Voltage Output High	V <sub>ID</sub> = +100mV	ROUT	2.8	3		V
		Inputs Open		2.8	3		
		Inputs Shorted		2.8	3		
		Inputs Terminated, R <sub>L</sub> = 27Ω		2.8	3		
V <sub>OL</sub>	Voltage Output Low	I <sub>OL</sub> = 2.0mA, V <sub>ID</sub> = -100mV			0.1	0.4	
I <sub>OS</sub>	Output Short Circuit Current	V <sub>OUT</sub> = 0V, V <sub>ID</sub> = 100V		-5	-35	-85	mA
V <sub>TH</sub>	Input Threshold High	DE = 0V	DO+/RI+ DO-/RI-			100	mV
V <sub>TL</sub>	Input Threshold Low			-100			
I <sub>IN</sub>	Input Current	DE = 0V, V <sub>IN</sub> = 2.4V or 0V		-20	±1	20	μA
		V <sub>CC</sub> = 0V, V <sub>IN</sub> = 2.4V or 0V		-20	±1	20	
V <sub>IH</sub>	Minimum Input High Voltage		IN, DE, RE	2.0		V <sub>CC</sub>	V
V <sub>IL</sub>	Minimum Input Low Voltage				GND	0.8	
I <sub>IH</sub>	Input High Current	V <sub>IN</sub> = V <sub>CC</sub> or 2.4V			±1	10	μA
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = GND or 0.4V			±1	10	
V <sub>CCL</sub>	Input Diode Clamp Voltage	I <sub>CLAMP</sub> = -18mA		-1.5	-0.8		V
I <sub>ICCD</sub>	Power Supply Current	DE = $\overline{RE}$ = V <sub>CC</sub> , R <sub>L</sub> = 27Ω	V <sub>CC</sub>		13	20	mA
I <sub>ICCR</sub>		DE = $\overline{RE}$ = 0V			5	8	
I <sub>ICCZ</sub>		DE = 0V, $\overline{RE}$ = V <sub>CC</sub>			3	7.5	
I <sub>CC</sub>		DE = V <sub>CC</sub> , $\overline{RE}$ = 0V, R <sub>L</sub> = 27Ω			16	22	
C <sub>OUTPUT</sub>	Bus Pin Capacitance		DO+/RI+ DO-/RI-		5		pF

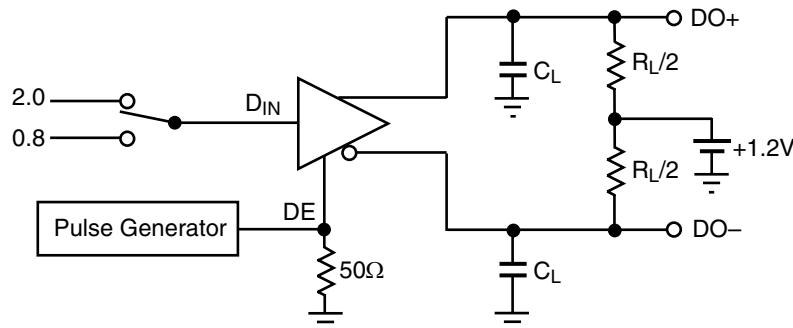
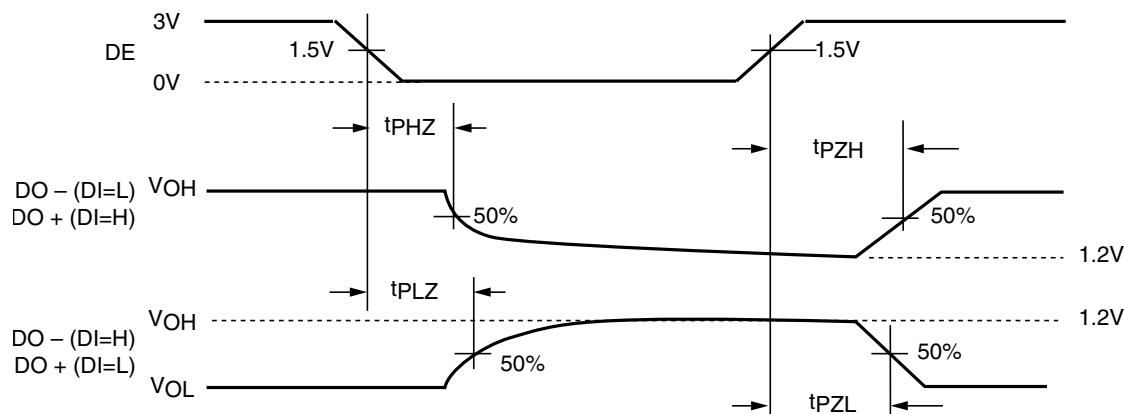
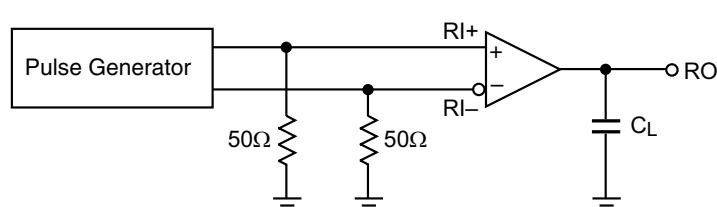
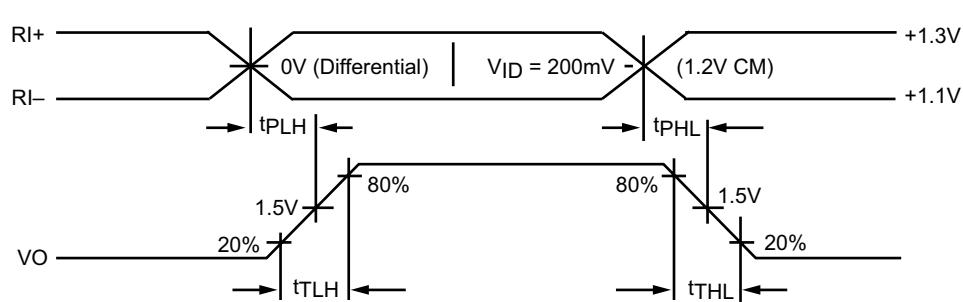
**Notes:**

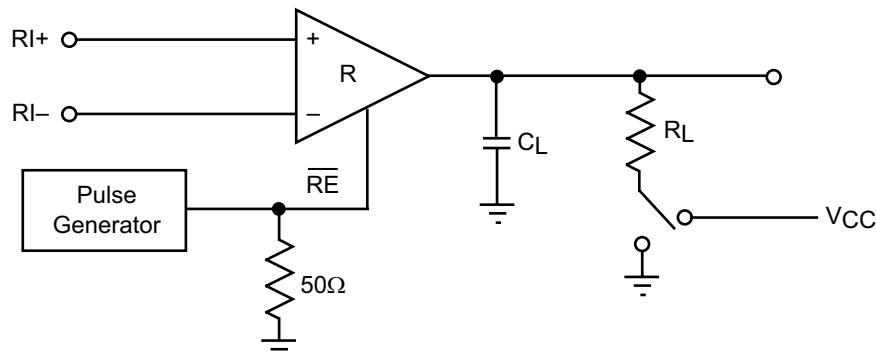
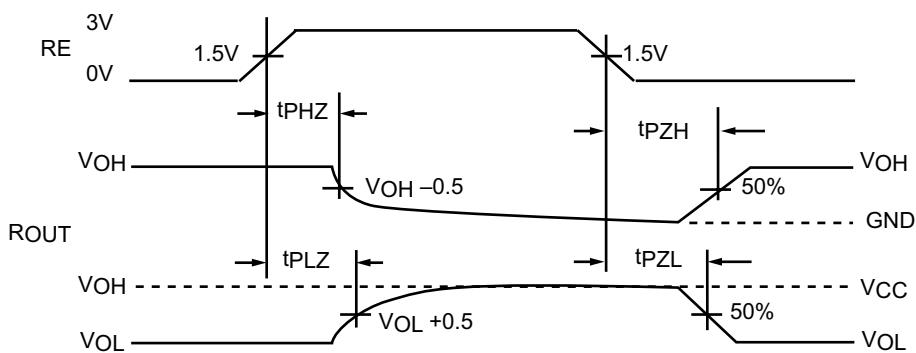
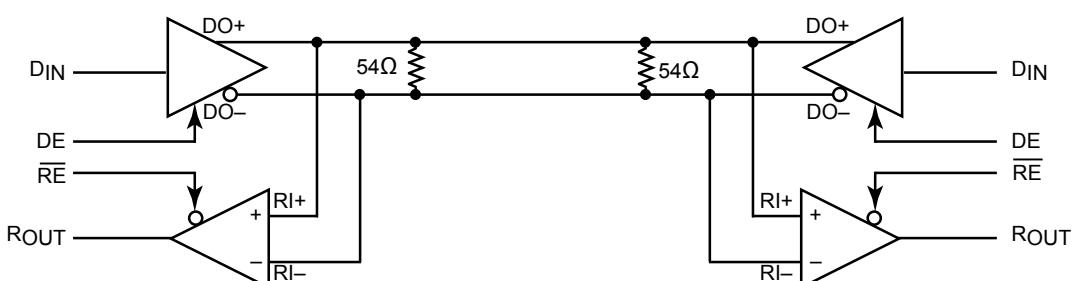
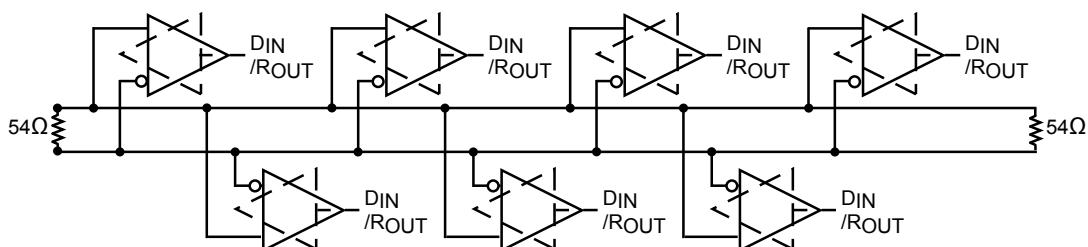
- “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
- All currents into device pins are positive, all currents out of device pins are negative. All voltages are referenced to ground except: V<sub>OD</sub>, V<sub>ID</sub>, V<sub>TH</sub>, and V<sub>TL</sub>, unless otherwise specified.
- All typicals are given for V<sub>CC</sub> = +3.3V or 5.0V and T<sub>A</sub> = +25°C unless otherwise stated.
- ESD Rating: HBM (15kΩ, 100pF) > 2.0kV EAT (0Ω, 200pF) > 300V.
- C<sub>L</sub> includes probe and jig capacitance.
- Generator waveforms for all tests unless otherwise specified: f = 1MHz, Z<sub>O</sub> = 50Ω, t<sub>r</sub>, t<sub>f</sub> ≤ 6.0ns (0% - 100%) on control pins and ≤ 1.0ns for R<sub>I</sub> inputs.
- The PI90LVB010 is a current mode device and only functions with datasheet specification when a resistive load is applied between the driver outputs.
- For receiver disable delays, the switch is set to V<sub>CC</sub> for t<sub>PZL</sub>, and t<sub>PLZ</sub> and to GND for t<sub>PZH</sub> and t<sub>PHZ</sub>.

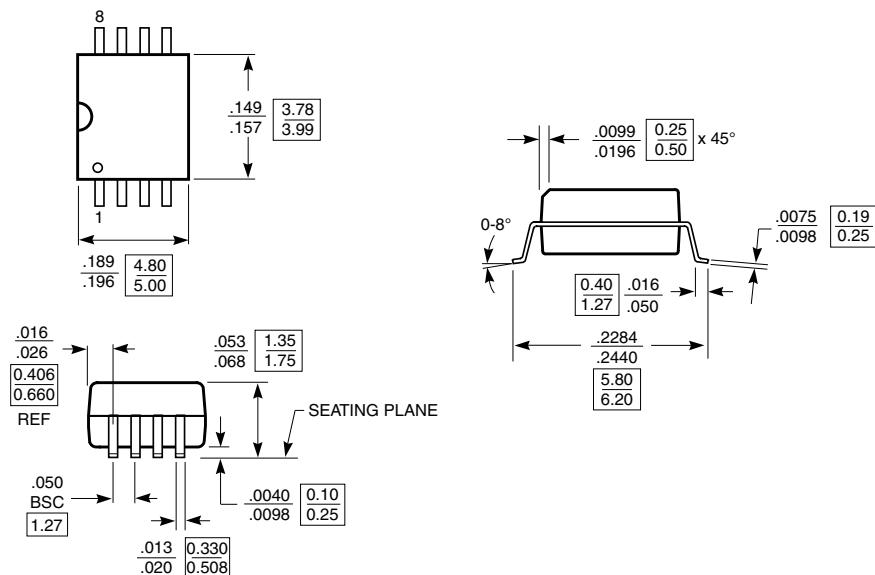
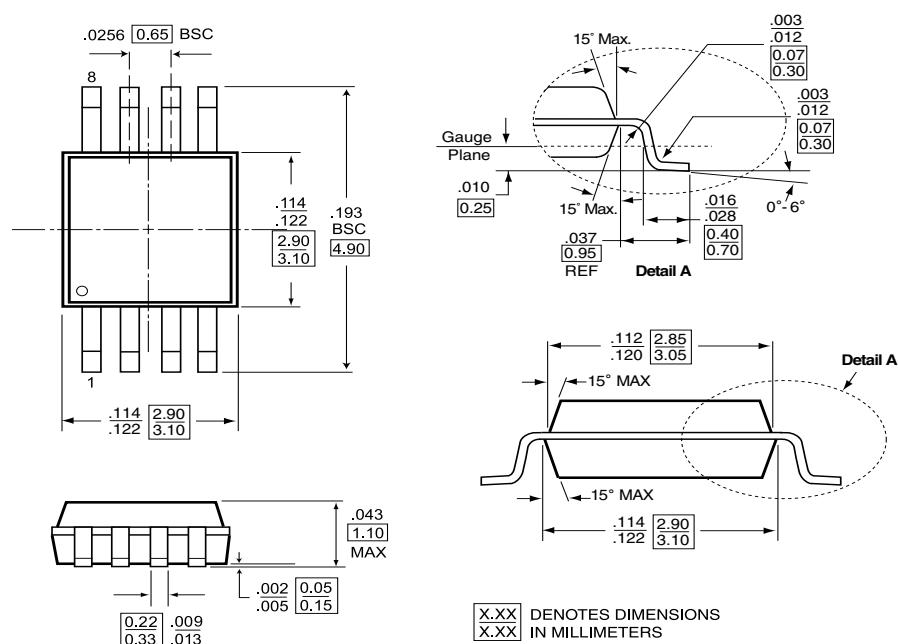
**AC Electrical Characteristics** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ )

Symbol	Paramter	Test Conditions	Min.	Typ.	Max.	Units
<b>Differential Driver Timing Requirement</b>						
$t_{PHLD}$	Differential Propagation Delay High to Low	$R_L = 27\Omega$ $C_L = 10\text{pF}$ Figures 2 & 3	0.7	1.5	2.7	ns
$t_{PLHD}$	Differential Propagation Delay Low to High		0.7	1.5	2.7	
$t_{SKD}$	Differential Skew $  t_{PHLD} - t_{PLHD}  $			0.2	1.0	
$t_{TLH}$	Transition Time Low to High			0.3	0.9	
$t_{THL}$	Transition Time High to Low			0.3	0.9	
$t_{PHZ}$	Disable Time High to Z		0.5	2.6	3.3	
$t_{PLZ}$	Disable Time Low to Z		0.5	2.6	3.3	
$t_{PZH}$	Enable Time Z to High		0.5	2.6	3.3	
$t_{PZL}$	Enable Time Z to Low		0.5	2.6	3.3	
<b>Differential Receiver Timing Requirements</b>						
$t_{PHLD}$	Differential Propagation Delay High to Low	$R_L = 27\Omega$ $C_L = 10\text{pF}$ Figures 6 & 7	1.3	2.1	3.2	ns
$t_{PLHD}$	Differential Propagation Delay Low to High		1.3	2.1	3.2	
$t_{SKD}$	Differential Skew $  t_{PHLD} - t_{PLHD}  $			0.5	2.0	
$t_R$	Rise Time			0.8	1.4	
$t_F$	Fall Time			1.8	1.4	
$t_{PHZ}$	Disable Time High to Z	$R_L = 500\Omega$ $C_L = 10\text{pF}^{(8)}$ Figures 8 & 9	1.5	4.0	6.0	ns
$t_{PLZ}$	Disable Time Low to Z		5.0	4.0	7.0	
$t_{PZH}$	Enable Time Z to High		0.5	2.5	7.0	
$t_{PZL}$	Enable Time Z to Low		0.5	2.5	6.0	

**Test Circuits and Timing Waveforms**

**Figure 1. Differential Driver DC Test Circuit**

**Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit**

**Figure 3. Driver Propagation Delay and Transition Time Waveforms**

**Test Circuits and Timing Waveforms (continued)**

**Figure 4. Driver Three-State Delay Test Circuit**

**Figure 5. Driver Three-State Delay Waveforms**

**Figure 6. Receiver Propagation Delay and Transistion Time Test Circuit**

**Figure 7. Receiver Propagation Delay and Transistion Time Waveforms**

**Test Circuits and Timing Waveforms (continued)**

**Figure 8. Receiver Three-State Delay Test Circuit**

**Figure 9. Receiver Three-State Delay Waveforms**
**Typical Bus Application Configurations**

**Figure 10. Bidirectional Half-Duplex Point-to-Point Applications**

**Figure 11. Multipoint Bus Applications**

**Packaging Mechanical: 8-Pin SOIC (W)**

**Packaging Mechanical: 8-Pin MSOP (U)**


**Ordering Information**

Ordering Code	Package Code	Package Description
PI90LVB010WE	W	Pb-free & Green, 8-pin, SOIC
PI90LVB010UE	U	Pb-free & Green, 8-pin MSOP

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)

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