

Features

- Bus LVDS Signaling (BLVDS)
- Designed for Double Termination Applications
- Balanced Output Impedance
- Light Bus Loading: 5pF typical
- Glitch-free power up/down (Driver Disabled)
- Operates from a 3.3V supply
- High Signaling Rate Capability: >100Mbps
- Driver:
 - $\pm 250\text{mV}$ Differential Swing into a 27Ω load
 - Propagation Delay of 1.5ns typ.
 - Low Voltage TTL (LVTTL) Inputs are 5V Tolerant
- Receiver:
 - Accepts $\pm 50\text{mV}$ (min.) Differential Swing with up to 2.0V ground potential difference
 - Propagation Delay of 3.3ns typical
 - Low Voltage TTL (LVTTL) Outputs
 - Open, Short, and Terminated Fail Safe
- Bus terminal ESD exceeds 10kV
- Industrial Temperature Operation (-40°C to $+85^{\circ}\text{C}$)
- Packaging (Pb-free & Green available):
 - 8-lead SOIC (W)
 - 8-lead MSOP (U)

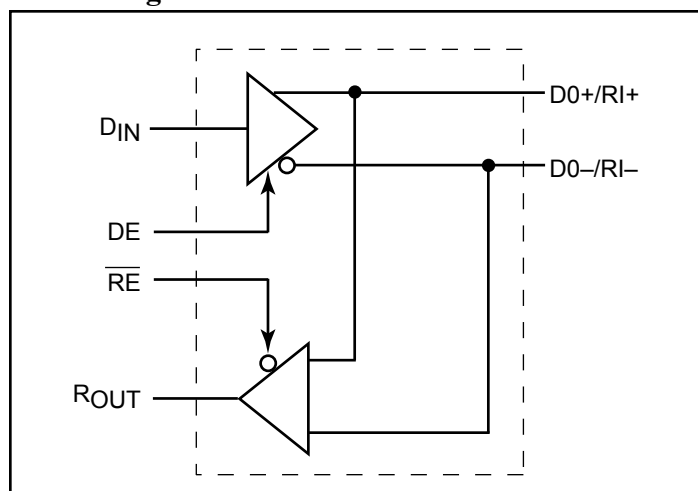
Description

The PI90LVB010 is a differential line driver and receiver (transceiver) that is similar to the IEEE1596.3 SCI and ANSI/TIA/EIA-644LVDS standards, the difference is that the driver output current is higher. This modification enables true half-duplex operation with more than one LVDS driver or with two line transmission resistors over a 50Ω differential transmission line. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The logic interface provides maximum flexibility resulting from four separate lines that are provided: D_{IN} , DE , \overline{RE} , and R_{OUT} .

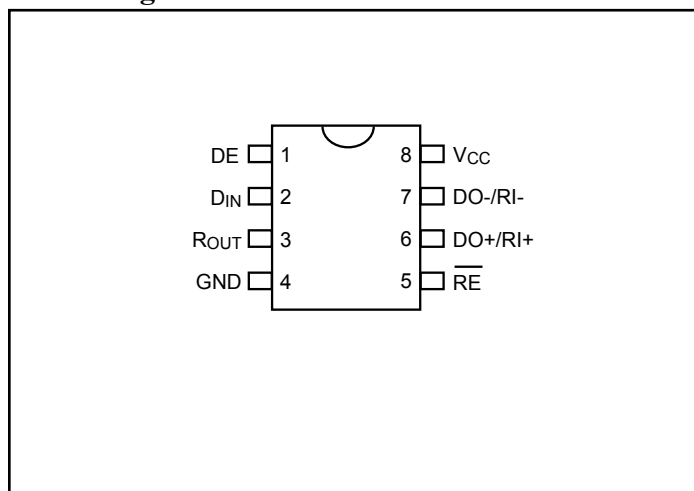
This device also feature flow-through which allows easy PCB routing for short stubs between the bus pins and the connector. The driver has 10mA drive capability, allowing it to drive heavily loaded backplanes, with impedance as low as 27Ω .

The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high-speed operation, while consuming minimal power with reduced EMI. In addition the differential signaling provides common mode noise rejection of $\pm 1\text{V}$.

Block Diagram



Pin Configuration



Absolute Maximum Ratings^(1,2)

Supply Voltage (V _{CC})	6.0V
Enable Input Voltage (DE, $\overline{\text{RE}}$)	−0.3V to (V _{CC} +0.3V)
Driver Input Voltage (DIN)	−0.3V to (V _{CC} +0.3V)
Receiver Output Voltage (R _{OUT})	−0.3V to (V _{CC} +0.3V)
Bus Pin Voltage (DO/RI±)	−0.3V to +3.9V
Driver Short Circuit	Continuous
ESD (HBM 1.5kΩ, 100pF)	>10kV
Maximum Package Power Dissipation at 20°C	
SOIC	1025mW
Derate SOIC Package	8.2mW/°C

Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 4s)	+260°C

Recommended Operating Conditions

	Min.	Max.	Units
Supply Voltage (V _{CC})	3.0	3.6	V
Receiver Input Voltage	0.0	2.9	V
Operating Free-Air Temperature	−40	+85	°C

Note:

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Functional Mode

Mode Select	DE	$\overline{\text{RE}}$
Driver Mode	H	H
Receiver Mode	L	L
3-State Mode	L	H
Loop Back Mode	H	L

Transmitter Mode

Inputs		Outputs	
DE	DI	DO+	DO-
H	L	L	H
H	H	H	L
H	2 > & > 0.8	X	X
L	X	Z	Z
H	Open	L	H

Receiver Mode

Inputs		Outputs
$\overline{\text{RE}}$	(RE+) - (RI-)	R _{OUT}
L	L (< -100mV)	L
L	H (> +100mV)	H
L	100mV > & > -100mV	?
H	X	Z

Pin Description

Pin Name	Pin#	Inputs/Outputs	Description
D _{IN}	2	I	TTL Driver Input
DO± RI±	6, 7	I/O	LVDS Driver Outputs/ LVDS Receiver Inputs
R _{OUT}	3	O	TTL Receiver Outputs
$\overline{\text{RE}}$	5	I	Receiver Enable TTL Input (Active Low)
DE	1	I	Driver Enable TTL Input (Active High)
GND	4	NA	Ground
V _{CC}	8	NA	Power Supply

Notes:

1. H = High, L = Low, Z = High Impedance, X = High or Low

DC Electrical Characteristics^(2,3) ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Parameter	Test Condition		Pin	Min.	Typ.	Max.	Units
V _{OD}	Output Differential Voltage	R _L = 27Ω, See figure 1		DO+/RI+ DO-/RI-	140	250	360	mV
ΔV _{OD}	V _{OD} Magnitude Change					3	30	
V _{OS}	Offset Voltage				1	1.25	1.65	V
ΔV _{OS}	Offset Magnitude Change					5	50	mV
I _{OSD}	Output Short Circuit Current	V _O = 0V, DE = V _{CC}				-12	-20	mA
V _{OH}	Voltage Output High	V _{ID} = +100mV	I _{OH} = -400	R _{OUT}	2.8	3		V
		Inputs Open			2.8	3		
		Inputs Shorted			2.8	3		
		Inputs Terminated, R _L = 27Ω			2.8	3		
V _{OL}	Voltage Output Low	I _{OL} = 2.0mA, V _{ID} = -100mV				0.1	0.4	
I _{OS}	Output Short Circuit Curretn	V _{OUT} = 0V, V _{ID} = 100V			-5	-35	-85	mA
V _{TH}	Input Threshold High	DE = 0V		DO+/RI+ DO-/RI-			100	mV
V _{TL}	Input Threshold Low				-100			
I _{IN}	Input Current	DE = 0V, V _{IN} = 2.4V or 0V		DO+/RI+ DO-/RI-	-20	±1	20	μA
		V _{CC} = 0V, V _{IN} = 2.4V or 0V			-20	±1	20	
V _{IH}	Minimum Input High Voltage			IN, DE, RE	2.0		V _{CC}	V
V _{IL}	Minimum Input Low Voltage				GND		0.8	
I _{IH}	Input High Current	V _{IN} = V _{CC} or 2.4V				±1	10	μA
I _{IL}	Input Low Current	V _{IN} = GND or 0.4V				±1	10	
V _{CL}	Input Diode Clamp Voltage	I _{CLAMP} = -18mA			-1.5	-0.8		V
I _{CCD}	Power Supply Current	DE = $\overline{\text{RE}}$ = V _{CC} , R _L = 27Ω		V _{CC}		13	20	mA
I _{CCR}		DE = $\overline{\text{RE}}$ = 0V				5	8	
I _{CCZ}		DE = 0V, $\overline{\text{RE}}$ = V _{CC}				3	7.5	
I _{CC}		DE = V _{CC} , $\overline{\text{RE}}$ - 0V, R _L = 27Ω				16	22	
C _{OUTPUT}	Bus Pin Capacitance			DO+/RI+ DO-/RI-		5		pF

Notes:

- “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
- All currents into device pins are positive, all currents out of device pins are negative. All voltages are referenced to ground except: V_{OD} , V_{ID} , V_{TH} , and V_{TL} , unless otherwise specified.
- All typicals are given for $V_{CC} = +3.3\text{V}$ or 5.0V and $T_A = +25^\circ\text{C}$ unless otherwise stated.
- ESD Rating: HBM (15k Ω , 100pF) > 2.0kV EAT (0 Ω , 200pF) > 300V.
- C_L includes probe and jig capacitance.
- Generator waveforms for all tests unless otherwise specified: $f = 1\text{MHz}$, $Z_O = 50\Omega$, t_r , $t_f \leq 6.0\text{ns}$ (0% - 100%) on control pins and $\leq 1.0\text{ns}$ for R_I inputs.
- The PI90LVB010 is a current mode device and only functions with datasheet specification when a resistive load is applied between the driver outputs.
- For receiver disable delays, the switch is set to V_{CC} for t_{pZL} , and t_{pLZ} and to GND for t_{pZH} and t_{pHZ} .

AC Electrical Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Paramter	Test Conditions	Min.	Typ.	Max.	Units
Differential Driver Timing Requirement						
tPHLD	Differential Propagation Delay High to Low	R _L = 27Ω Figures 2 & 3 C _L = 10pF	0.7	1.5	2.7	ns
tPLHD	Differential Propagation Delay Low to High		0.7	1.5	2.7	
tSKD	Differential Skew tPHLD - tPLHD			0.2	1.0	
tTLH	Transition Time Low to High			0.3	0.9	
tTHL	Transition Time High to Low			0.3	0.9	
tPHZ	Disable Time High to Z	R _L = 27Ω Figures 4 & 5 C _L = 10pF	0.5	2.6	3.3	
tPLZ	Disable Time Low to Z		0.5	2.6	3.3	
tPZH	Enable Time Z to High		0.5	2.6	3.3	
tPZL	Enable Time Z to Low		0.5	2.6	3.3	
Differential Receicer Timing Requirements						
tPHLD	Differential Propagation Delay High to Low	Figures 6 & 7 C _L = 10pF	1.3	2.1	3.2	ns
tPLHD	Differenital Propagation Delay Low to High		1.3	2.1	3.2	
tSKD	Differential Skew tPHLD - tPLHD			0.5	2.0	
t _R	Rise Time			0.8	1.4	
t _F	Fall Time			1.8	1.4	
tPHZ	Disable Time High to Z	R _L = 500Ω Figures 8 & 9 C _L = 10pF ⁽⁸⁾	1.5	4.0	6.0	
tPLZ	Disable Time Low to Z		5.0	4.0	7.0	
tPZH	Enable Time Z to High		0.5	2.5	7.0	
tPZL	Enable Time Z to Low		0.5	2.5	6.0	

Test Circuits and Timing Waveforms

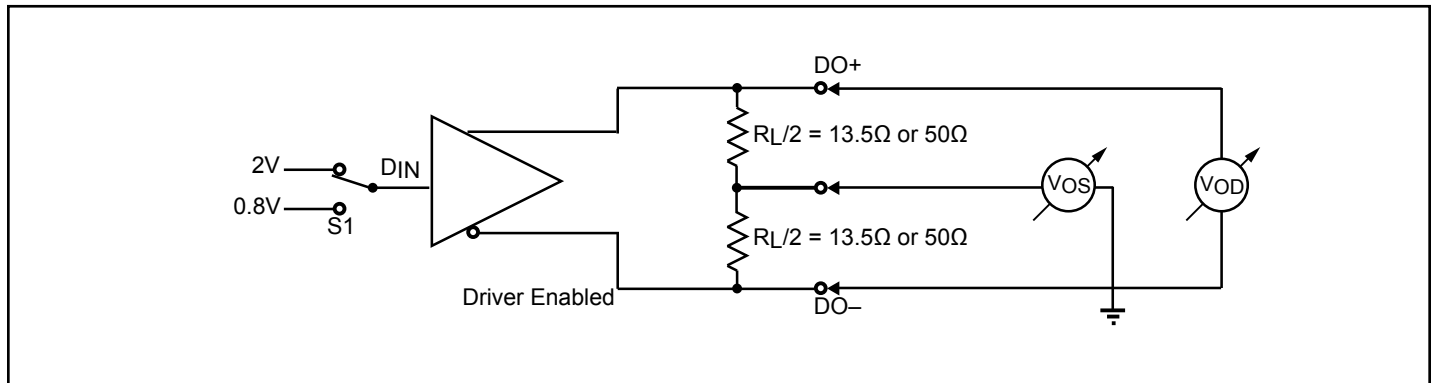


Figure 1. Differential Driver DC Test Circuit

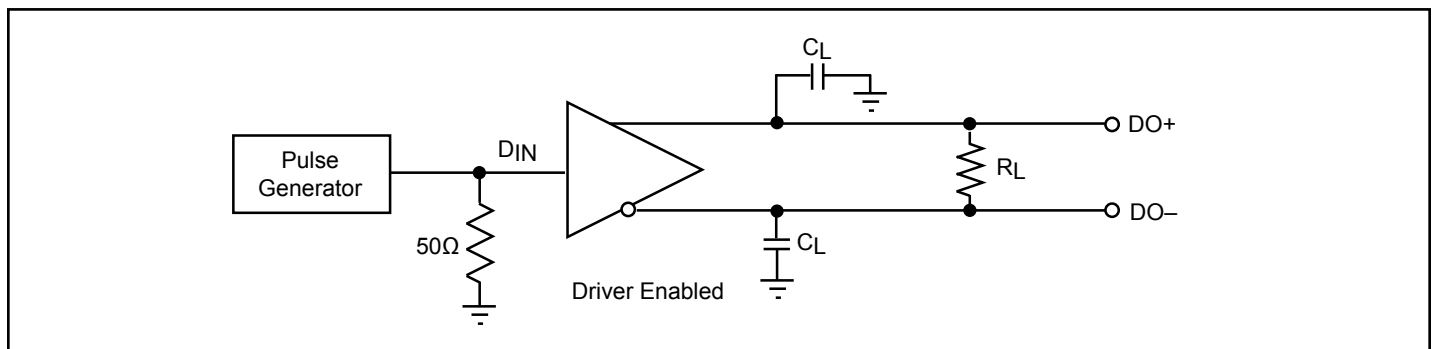


Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit

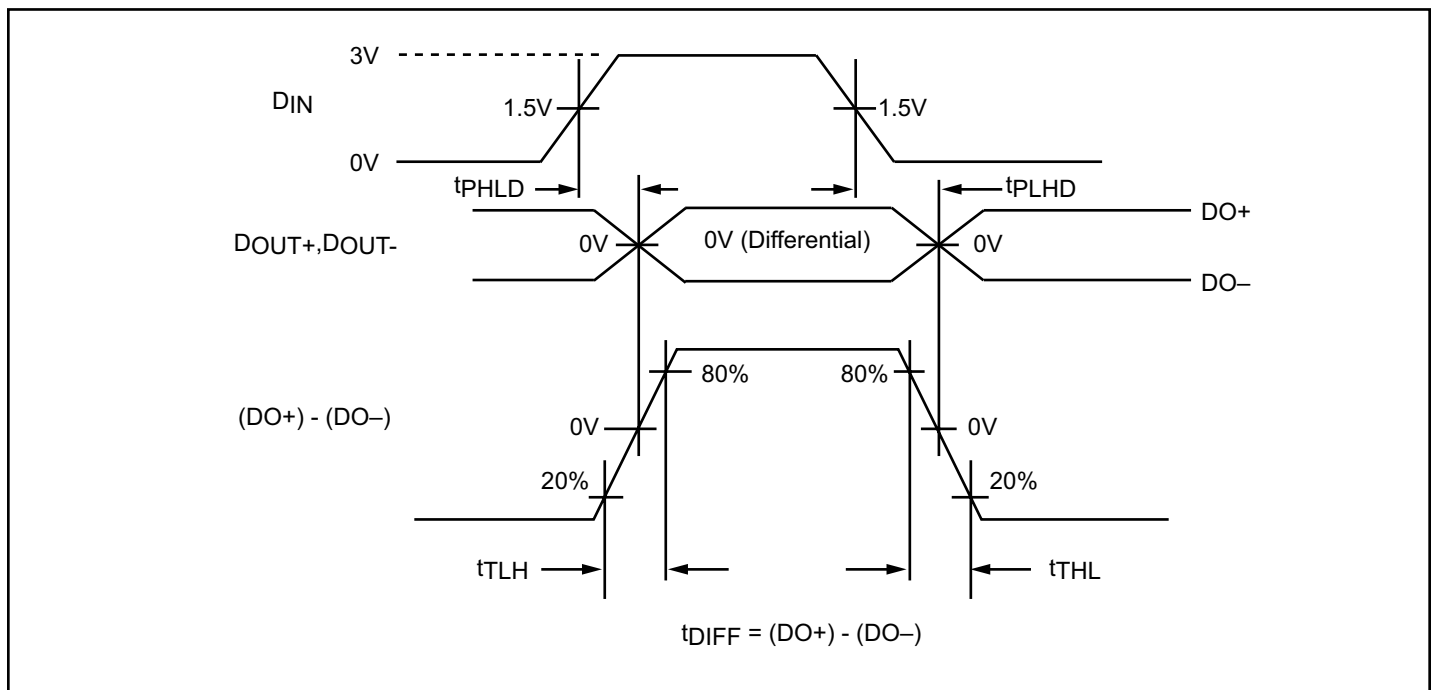
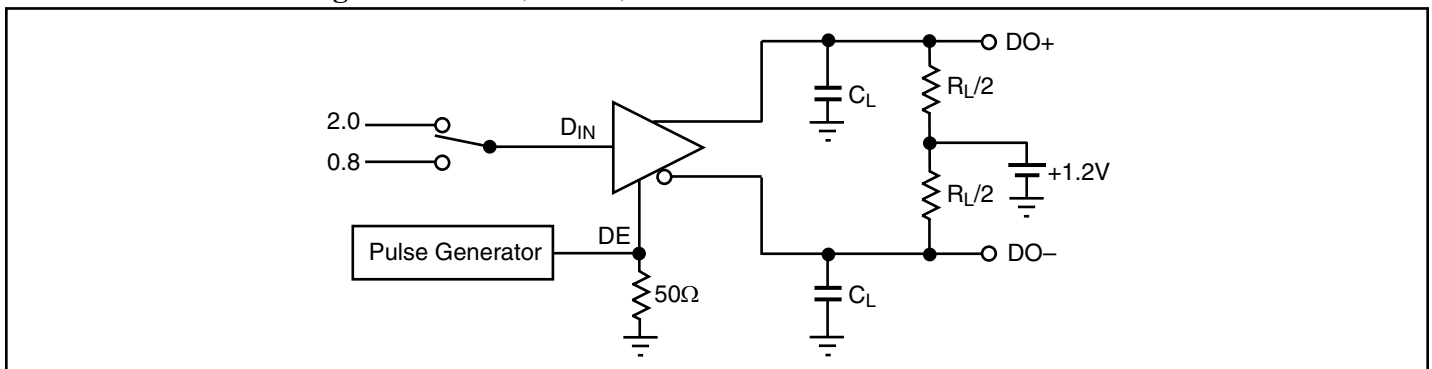
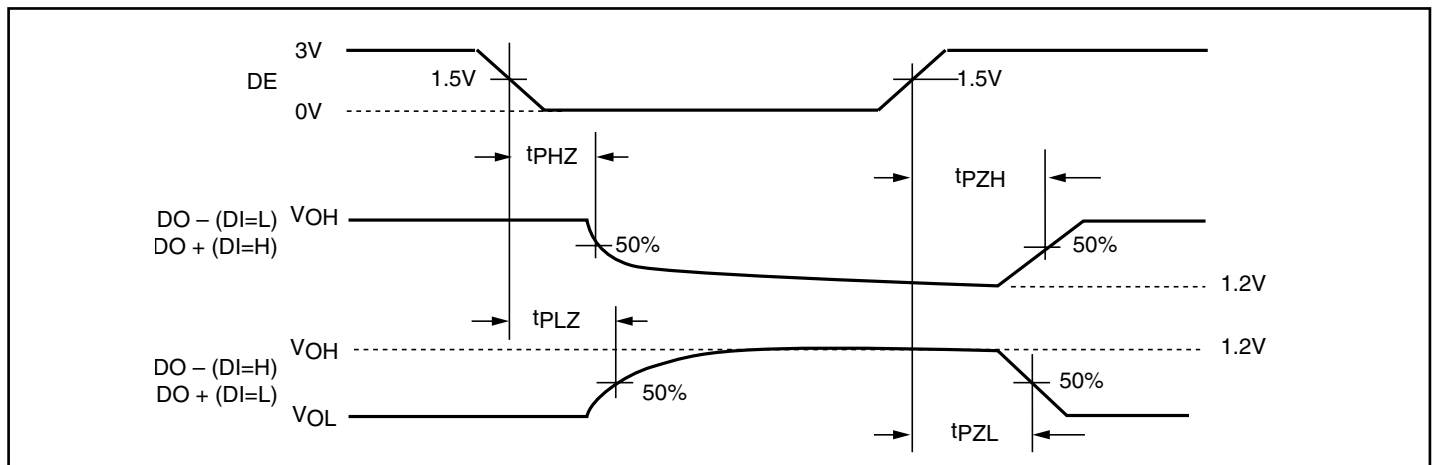
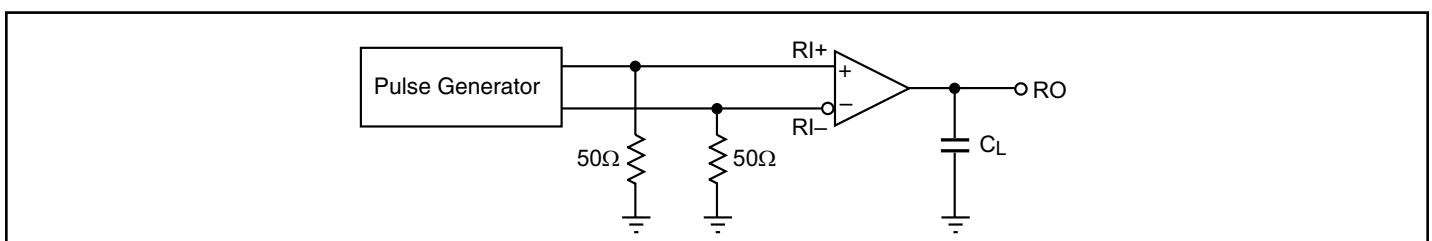
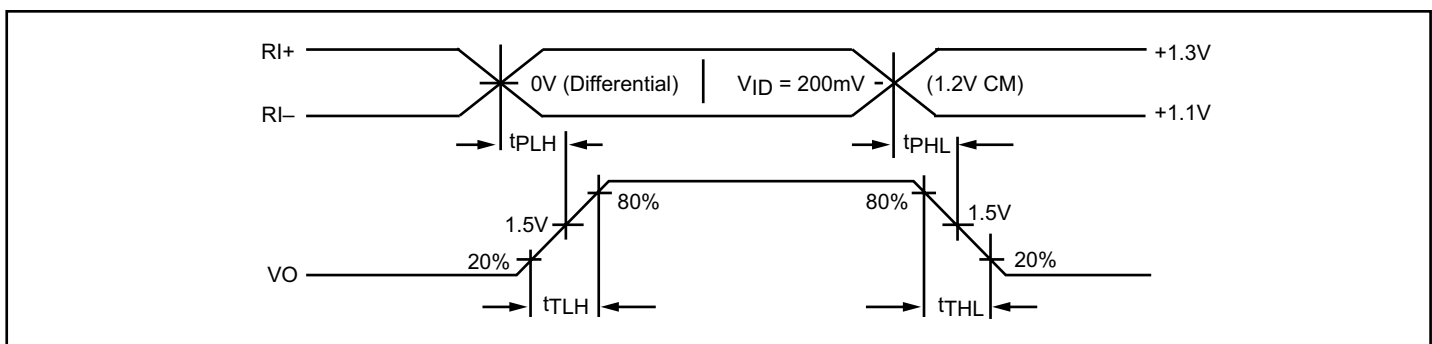
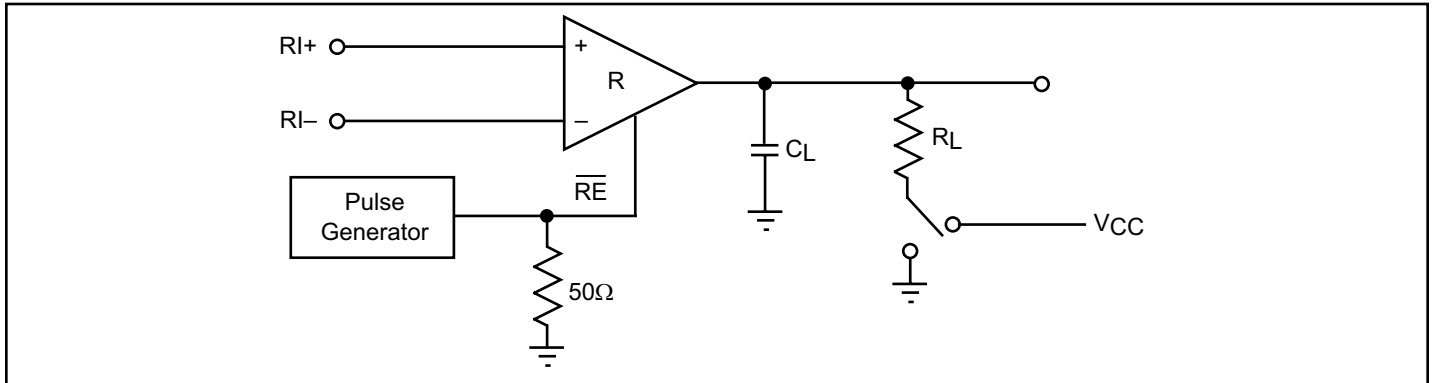
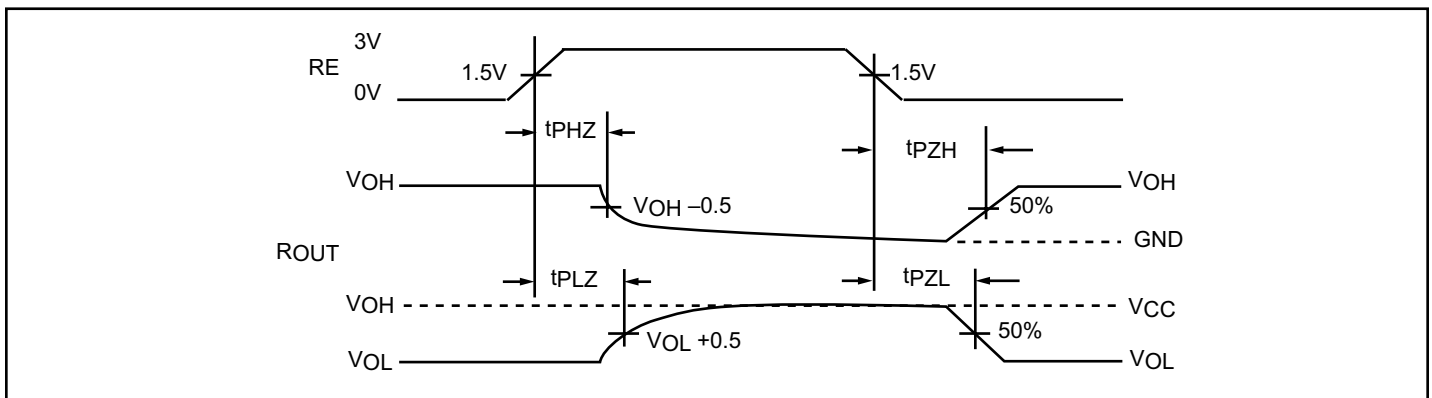
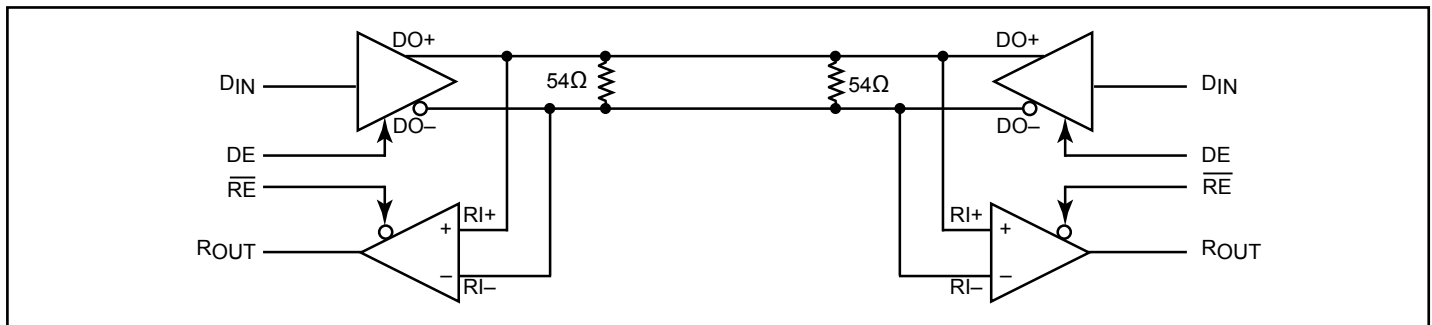
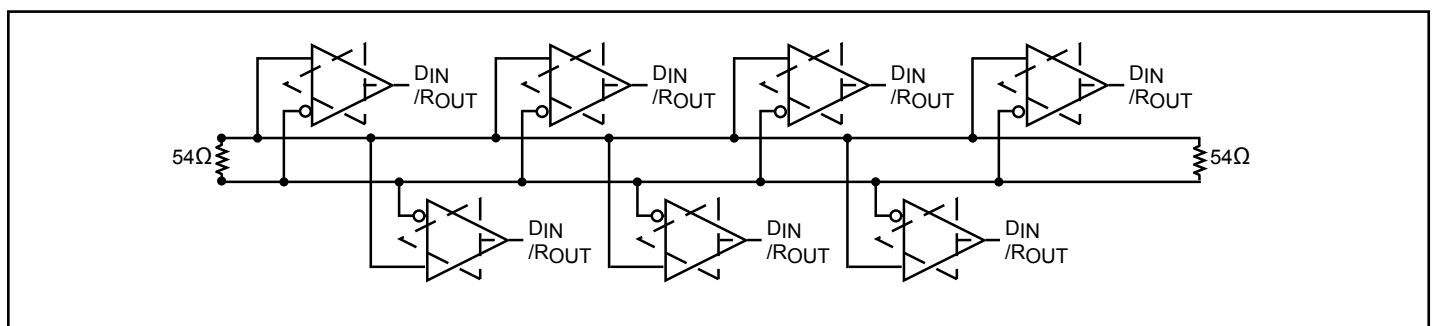
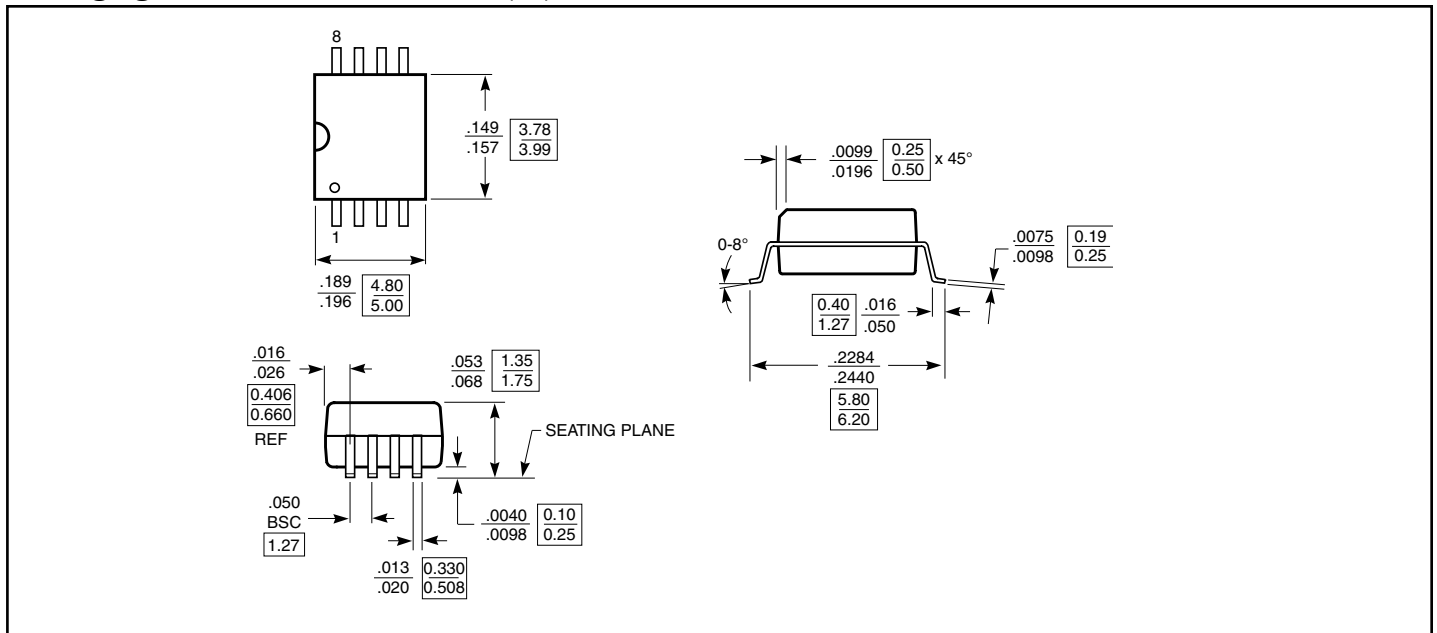
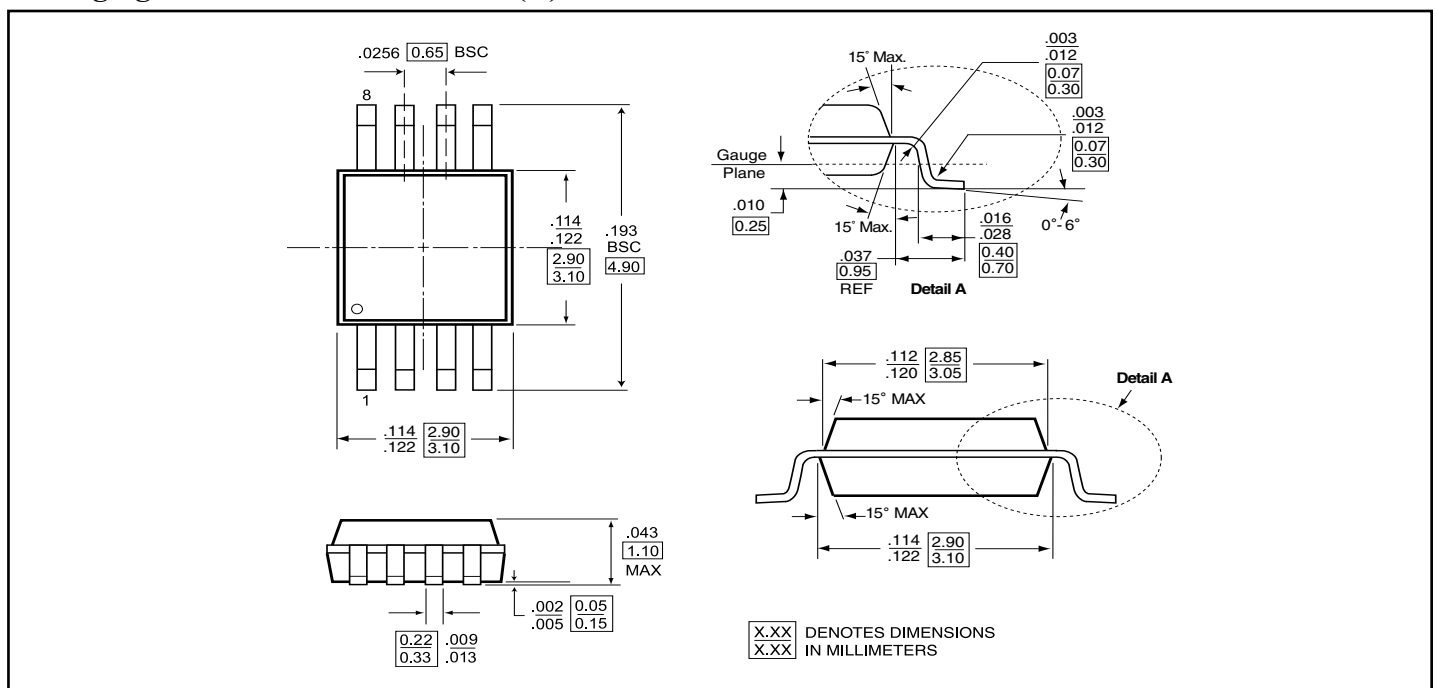


Figure 3. Driver Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Waveforms (continued)

Figure 4. Driver Three-State Delay Test Circuit

Figure 5. Driver Three-State Delay Waveforms

Figure 6. Receiver Propagation Delay and Transistion Time Test Circuit

Figure 7. Receiver Propagation Delay and Transistion Time Waveforms

Test Circuits and Timing Waveforms (continued)

Figure 8. Receiver Three-State Delay Test Circuit

Figure 9. Receiver Three-State Delay Waveforms
Typical Bus Application Configurations

Figure 10. Bidirectional Half-Duplex Point-to-Point Applications

Figure 11. Multipoint Bus Applications

Packaging Mechanical: 8-Pin SOIC (W)

Packaging Mechanical: 8-Pin MSOP (U)


Ordering Information

Ordering Code	Package Code	Package Description
PI90LVB010WE	W	Pb-free & Green, 8-pin, SOIC
PI90LVB010UE	U	Pb-free & Green, 8-pin MSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

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