



STP9NK60ZD - STF9NK60ZD STB9NK60ZD

N-CHANNEL 600V - 0.85Ω - 7A TO-220/TO-220FP/D²PAK

SuperFREDMesh™ MOSFET

ADVANCED DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP9NK60ZD	600 V	< 0.95 Ω	7 A	125 W
STF9NK60ZD	600 V	< 0.95 Ω	7 A	30 W
STB9NK60ZD	600 V	< 0.95 Ω	7 A	125 W

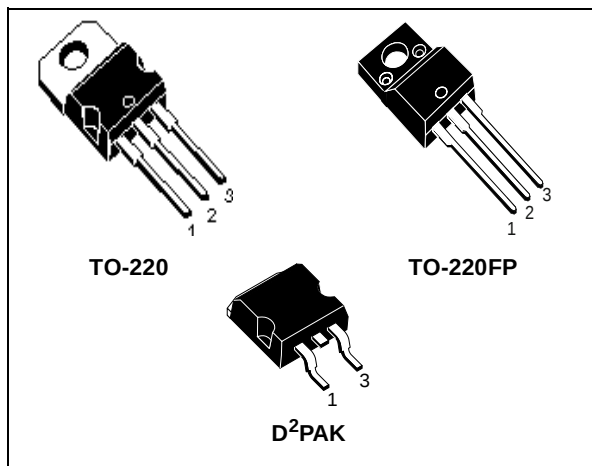
- TYPICAL R_{DS(on)} = 0.85 Ω
- VERY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- LOW INTRINSIC CAPACITANCES
- FAST INTERNAL RECOVERY DIODE

DESCRIPTION

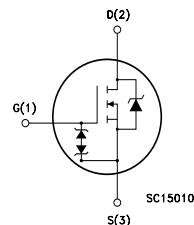
The SuperFREDMesh™ series associates all advantages of reduced on-resistance, zener gate protection and very high dv/dt capability with a Fast body-drain recovery diode. Such series complements the "FDmesh™" Advanced Technology.

APPLICATIONS

- HID BALLAST
- ZVS PHASE-SHIFT FULL BRIDGE CONVERTERS



INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP9NK60ZD	P9NK60ZD	TO-220	TUBE
STF9NK60ZD	F9NK60ZD	TO-220FP	TUBE
STB9NK60ZDT4	B9NK60ZD	D ² PAK	TAPE & REEL

STP9NK60ZD - STF9NK60ZD - STB9NK60ZD

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		TO-220 / D ² PAK	TO-220FP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600		V
V _{GS}	Gate- source Voltage	± 30		V
I _D	Drain Current (continuous) at T _C = 25°C	7	7 (*)	A
I _D	Drain Current (continuous) at T _C = 100°C	4.3	4.3 (*)	A
I _{DM} (•)	Drain Current (pulsed)	28	28 (*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	125	30	W
	Derating Factor	1	0.24	W/°C
V _{ESD(G-S)}	Gate source ESD (HBM-C=100pF, R=1.5KΩ)	4000		V
dv/dt (1)	Peak Diode Recovery voltage slope	15		V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150		°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 7A, di/dt ≤ 500A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j = 25°C

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220 D ² PAK	TO-220FP	Unit
R _{thj-pcb}	Thermal Resistance Junction-pcb Max (When mounted on minimum Footprint)	30		°C/W
R _{thj-case}	Thermal Resistance Junction-case Max	1	4.16	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5		°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	7	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	235	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{GS} =± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

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ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 1mA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 100μA	2.5	3.5	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 3.5 A		0.85	0.95	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 3.5 A		5.3		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1110 135 30		pF pF pF
C _{oss} eq. (3)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 480V		72		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V _{DD} = 300 V, I _D = 3.5 A R _G = 4.7Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		22 17		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 480V, I _D = 7 A, V _{GS} = 10V		41 8.7 21	53	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	V _{DD} = 300 V, I _D = 3.5 A R _G = 4.7Ω V _{GS} = 10 V (Resistive Load see, Figure 3)		42 15		ns ns
t _{r(voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	V _{DD} = 480V, I _D = 7 A, R _G = 4.7Ω, V _{GS} = 10V (Inductive Load see, Figure 5)		11 8 20		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				7 28	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 7 A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 7 A, di/dt = 100A/μs V _{DD} = 30V, T _j = 25°C (see test circuit, Figure 5)		150 663 8.5		ns nC A
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 7 A, di/dt = 100A/μs V _{DD} = 30V, T _j = 150°C (see test circuit, Figure 5)		194 935 9.6		ns nC A

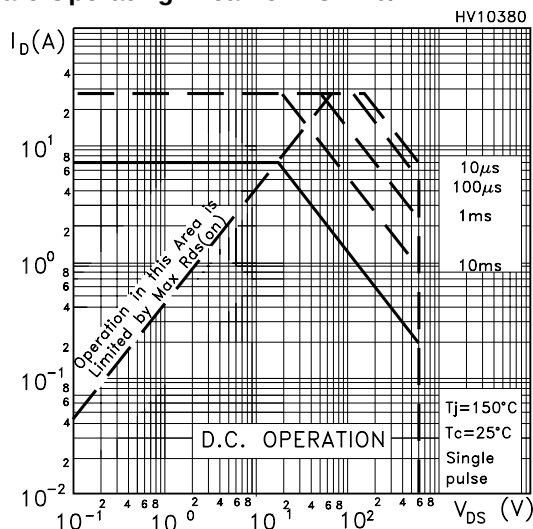
Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

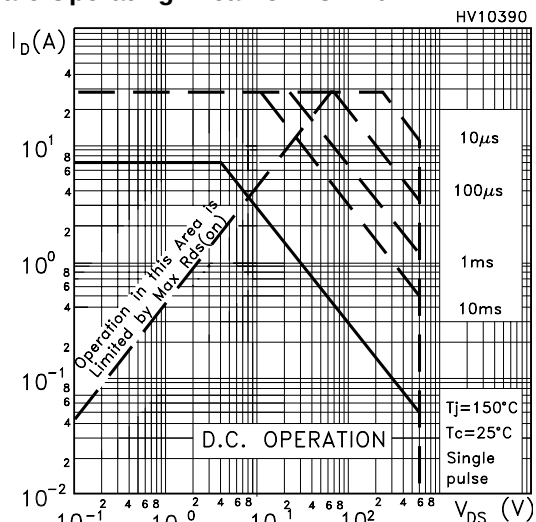
3. C_{oss} eq. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.



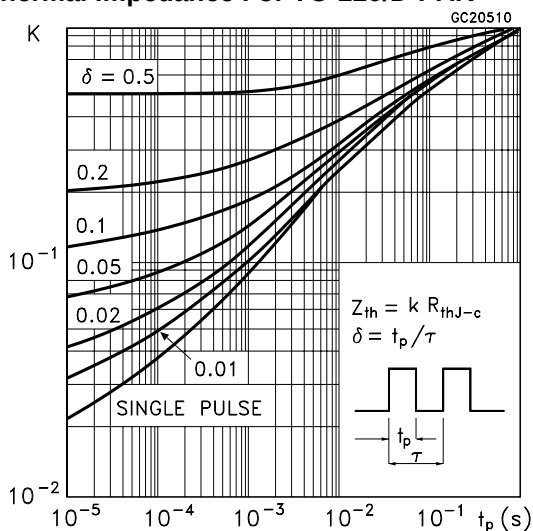
Safe Operating Area For TO-220/D²PAK



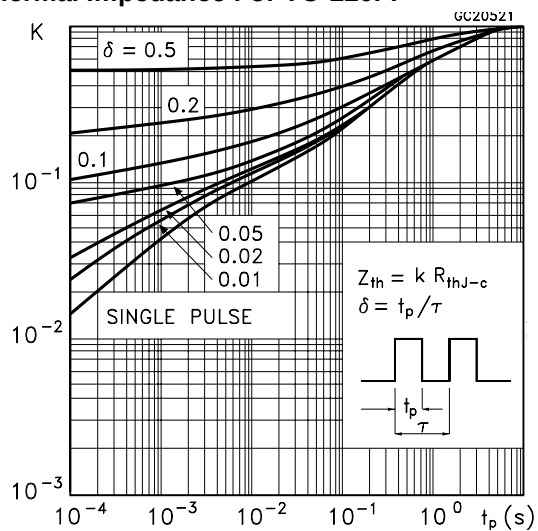
Safe Operating Area For TO-220FP



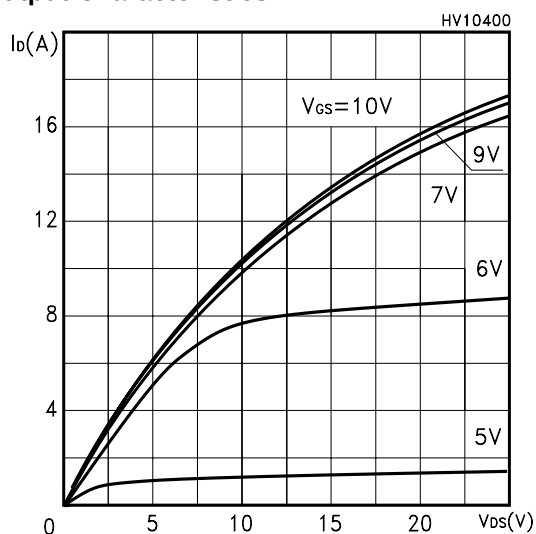
Thermal Impedance For TO-220/D²PAK



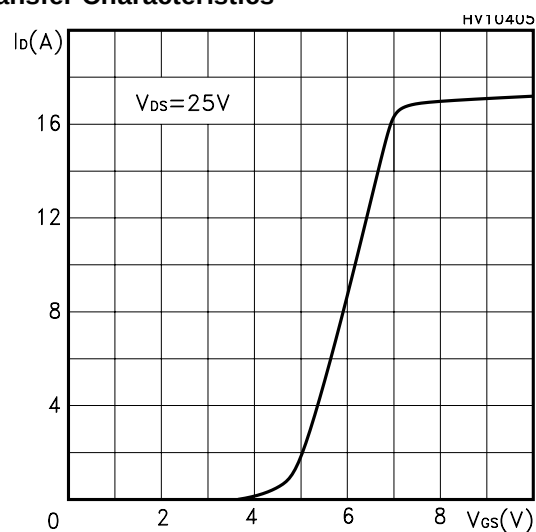
Thermal Impedance For TO-220FP



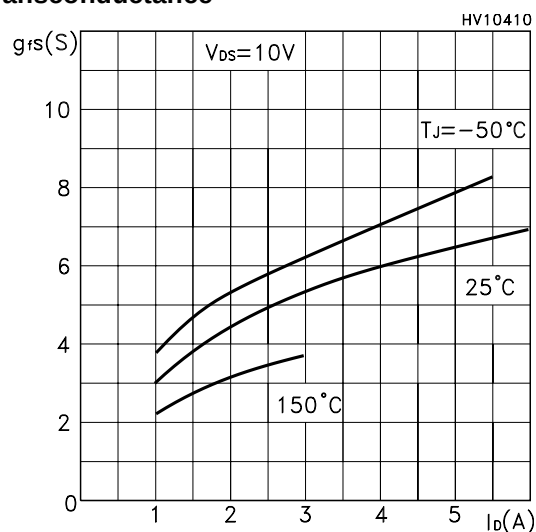
Output Characteristics



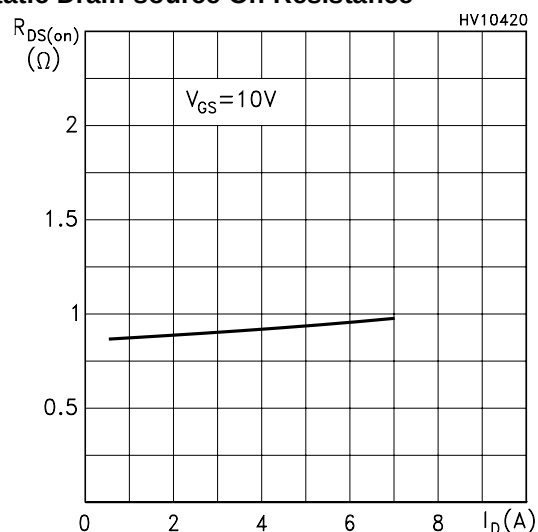
Transfer Characteristics



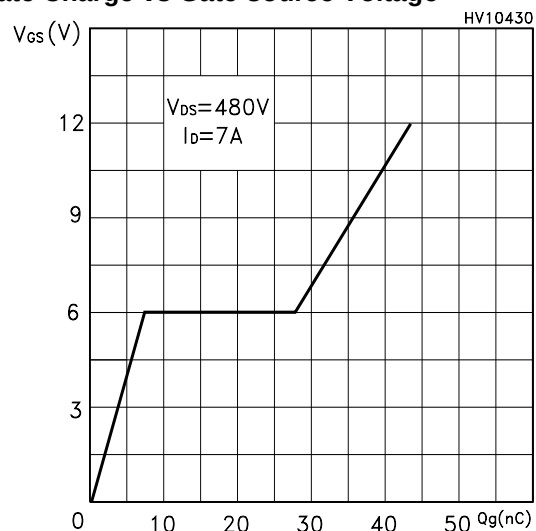
Transconductance



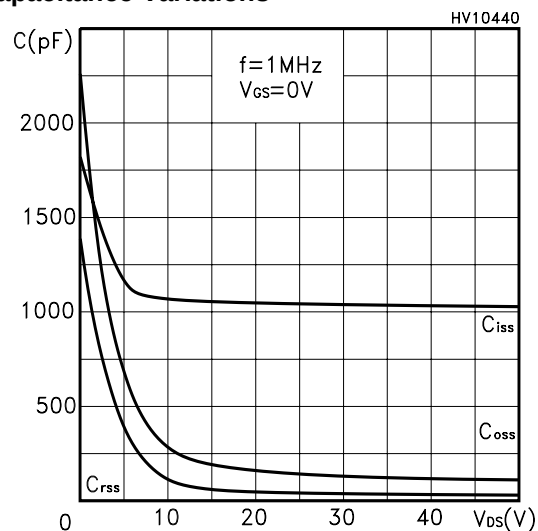
Static Drain-source On Resistance



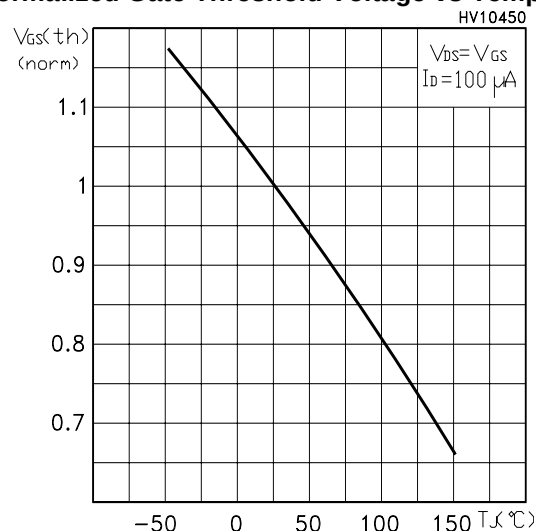
Gate Charge vs Gate-source Voltage



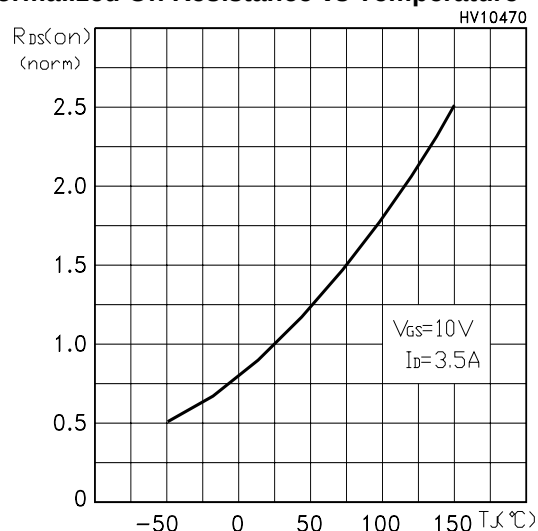
Capacitance Variations



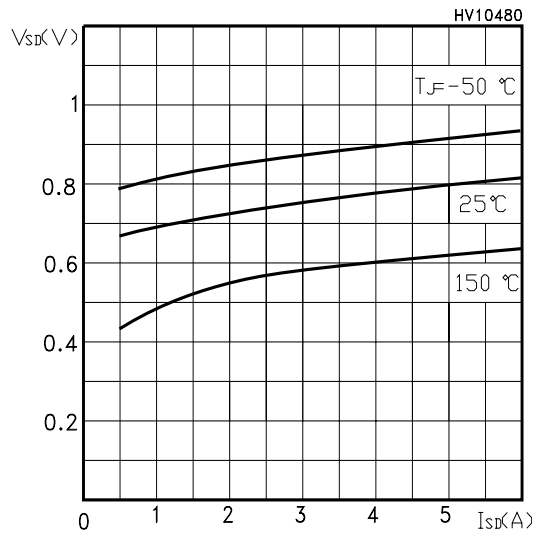
Normalized Gate Threshold Voltage vs Temp.



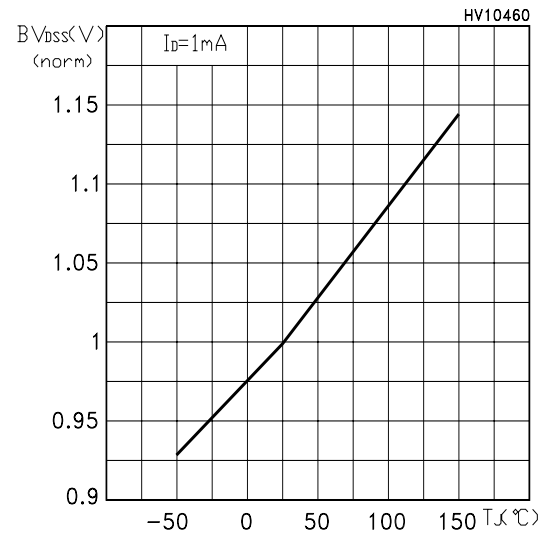
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature

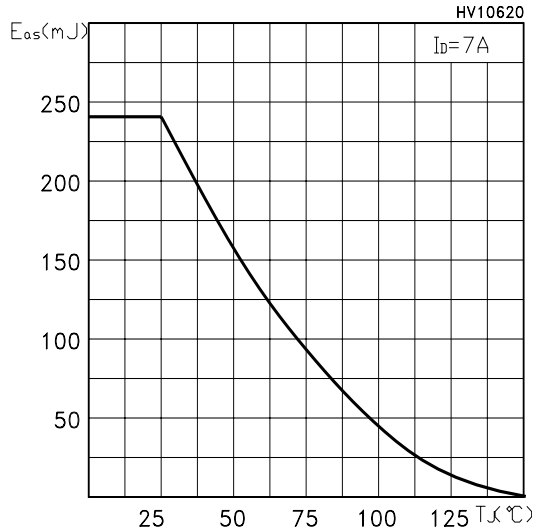


Fig. 1: Unclamped Inductive Load Test Circuit

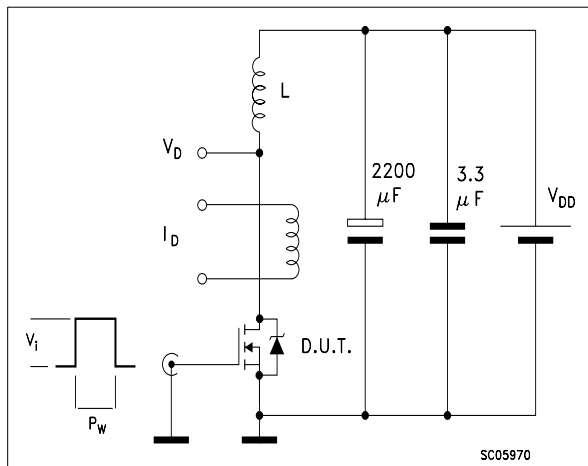


Fig. 2: Unclamped Inductive Waveform

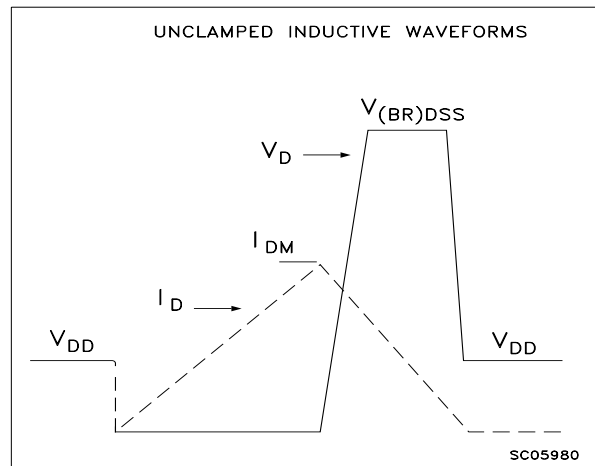


Fig. 3: Switching Times Test Circuit For Resistive Load

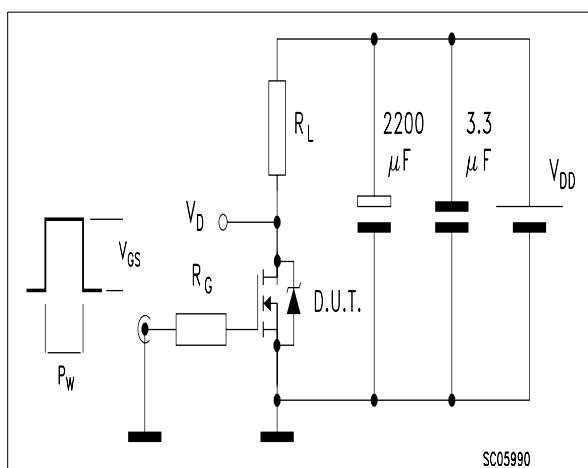


Fig. 4: Gate Charge test Circuit

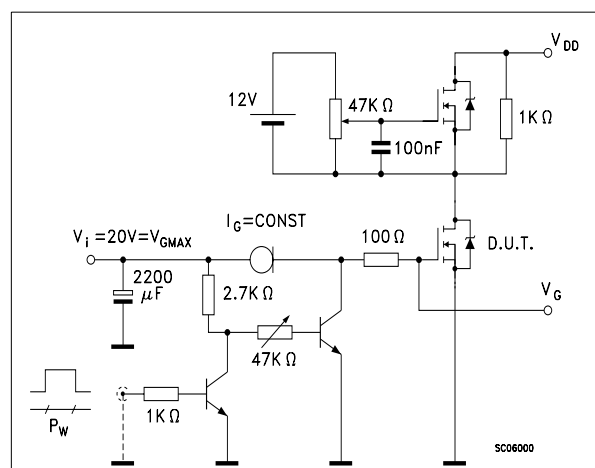
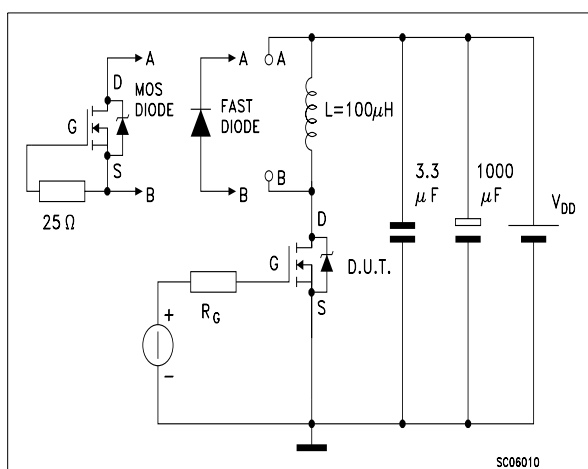
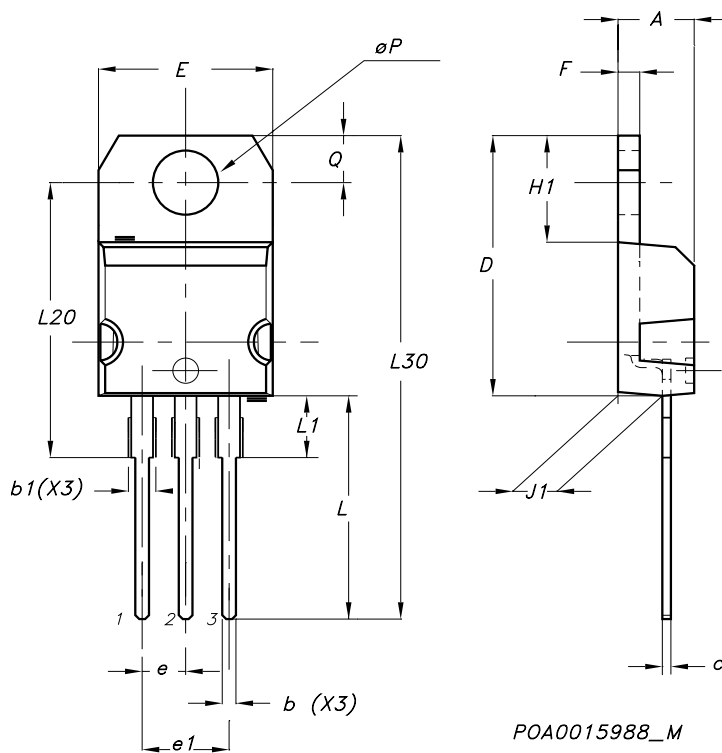


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



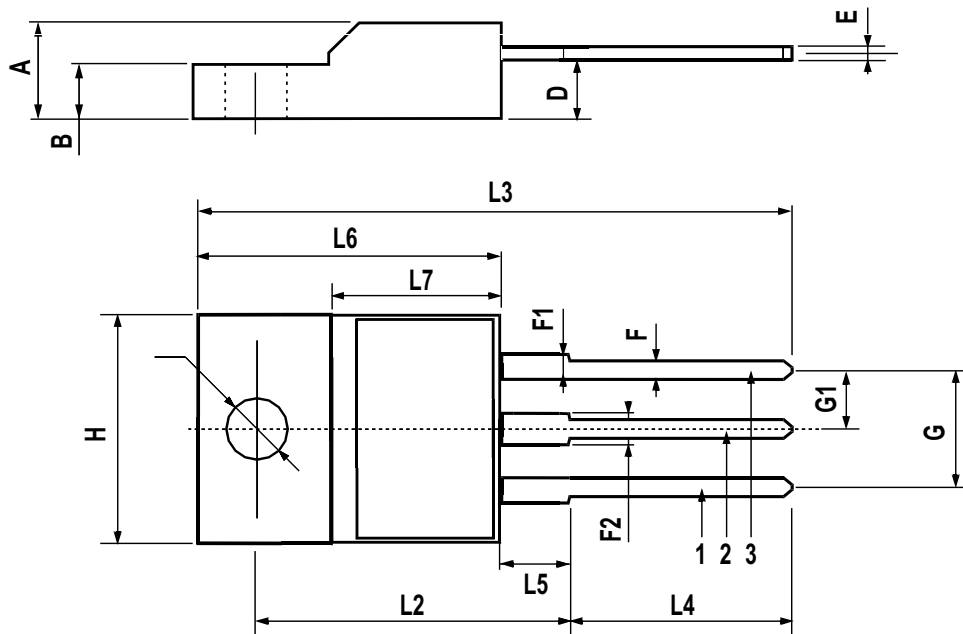
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



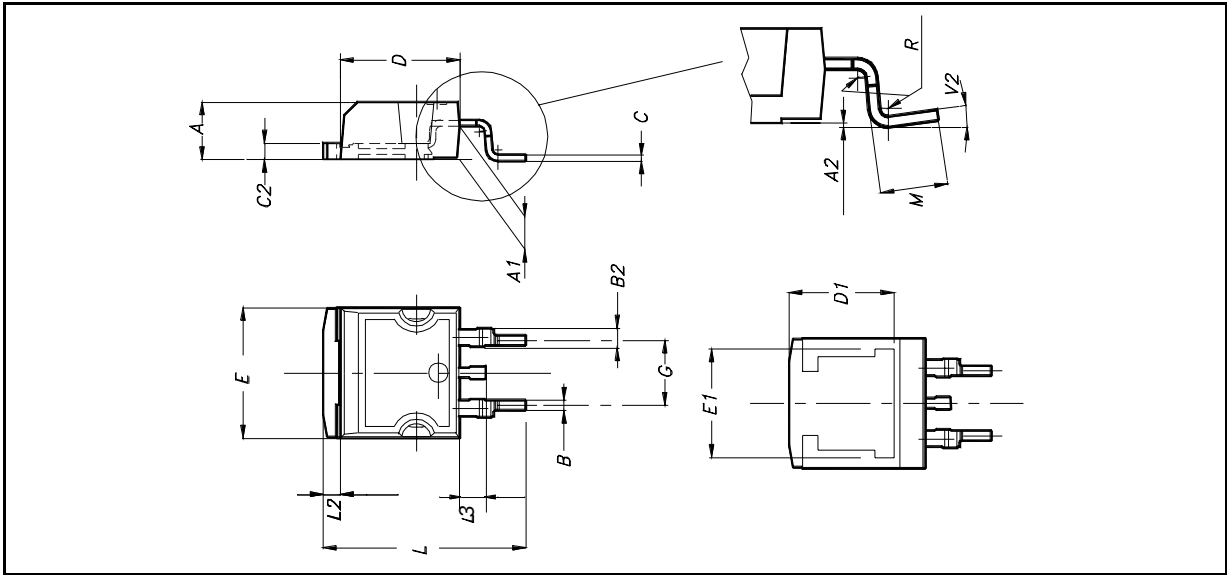
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.5	0.045		0.067
F2	1.15		1.5	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126

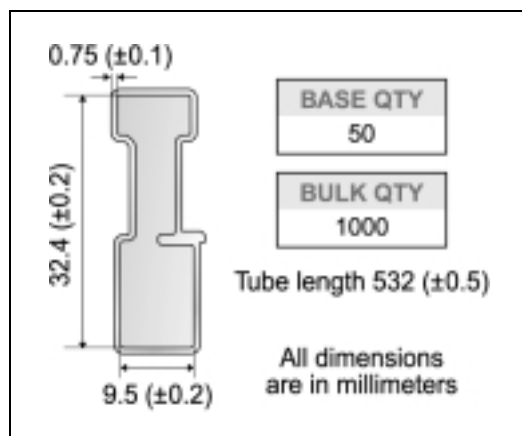
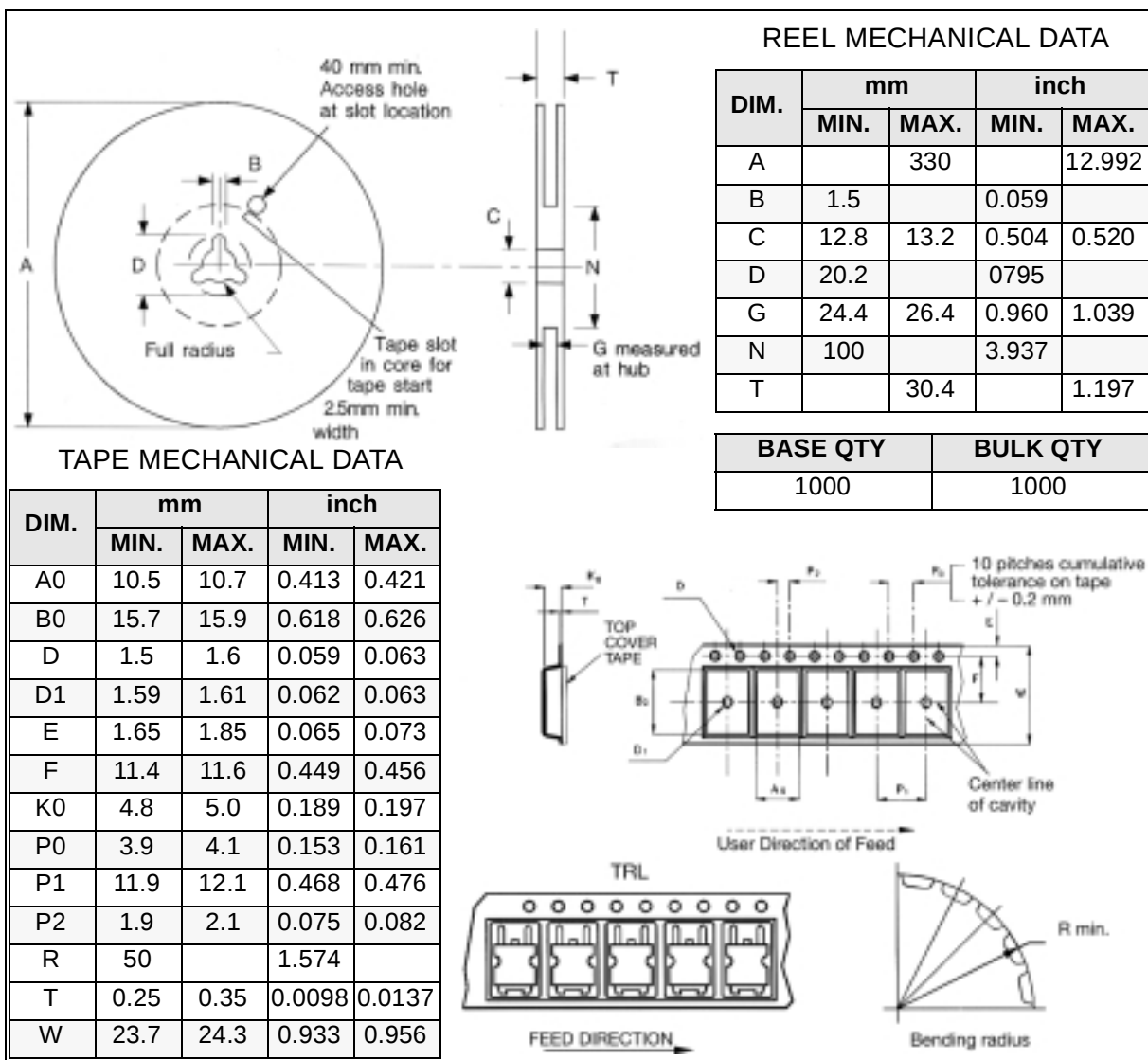


D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°			



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