Evaluation Board for 16/14/12-Bit, 6-Channel Simultaneous Sampling ADC

Preliminary Technical Data

EVAL-AD7656-1/AD7657-1/AD7658-1

FEATURES

Full-featured evaluation board for the AD7656-1/AD7657-1/AD7658-1
Compatibility with the EVAL-CONTROL BRD2
Standalone capability
Various linking options

GENERAL DESCRIPTION

This data sheet describes the setup and use of the AD7656-1/AD7657-1/AD7658-1 evaluation board. The AD7656-1/AD7657-1/AD7658-1 are 16/14/and 12-bit, 6-channel simultaneous sampling 250 kSPS ADCs. The AD7656-1/AD7657-1/AD7658-1 contain six 16/14/12-bit, low power, SAR ADCs respectively. The AD7656-1/AD7657-1/AD7658-1 operates from a single 4.75 V to 5.25 V supply and dual ±12 V power supply and features throughput rates of up to 250 kSPS. Full details on the AD7656-1/AD7657-1/AD7658-1 are available in the AD7656-1/AD7657-1/AD7658-1 data sheet available from Analog Devices, Inc. and should be consulted in conjunction with this data sheet when using the evaluation board.

On-board components for the EVAL-AD7656-1/AD7657-1/AD7658-1 include an AD797 op amp and an AD780 pin programmable, 2.5 V or 3 V ultra high precision, band gap reference.

Various link options are described in Table 1 and Table 2.

FUNCTIONAL BLOCK DIAGRAM

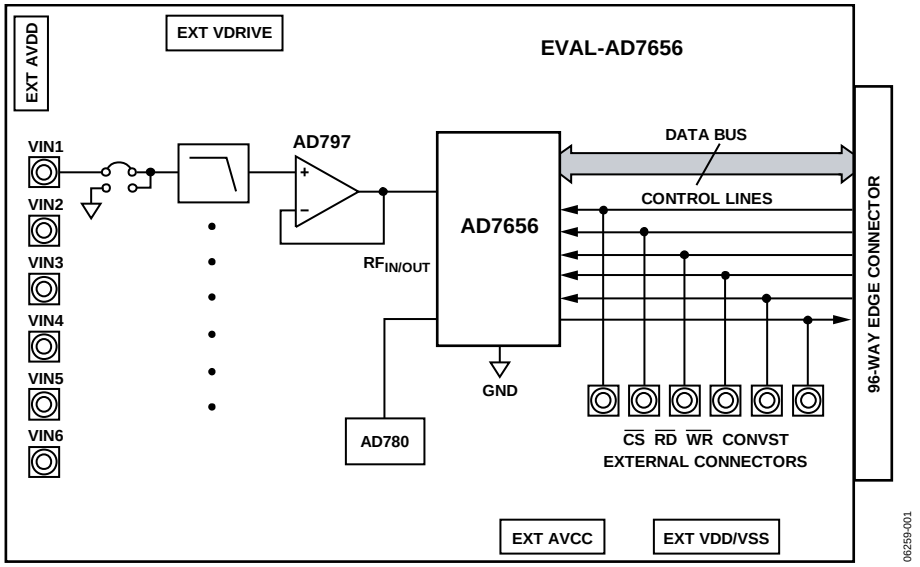

Figure 1.

Rev. PrA

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EVALUATION BOARD HARDWARE

POWER SUPPLIES

When this evaluation board is used with the EVAL-CONTROL BRD2, all supplies are provided from the control board through the 96-way connector. When the board is used as a standalone unit, external supplies must be provided. The evaluation board has the following nine power supply inputs:

- EXT_AV_{DD}
- AGND
- +12 V
- −12 V
- AGND
- VDRIVE
- DGND
- DVDD
- DGND

If the evaluation board is used in standalone mode, a 4.75 V to 5.25 V supply must be connected to the EXT_AV_{DD} input. The +12 V and −12 V supplies are required for the op amps and for the high voltage analog input section on the AD7656-1/AD7657-1/AD7658-1. These supplies are decoupled to the ground plane with 10 µF tantalum and 0.1 µF multilayer ceramic capacitors at the points where they enter the board. The supply pins of all the op amps and
the reference are also decoupled with 10 µF tantalum and 0.1 µF ceramic capacitors, as are the V_{DD}, V_{SS}, and AV_{CC} pins of the AD7656-1/AD7657-1/AD7658-1.

LINK OPTIONS

Link options must be selected for the required operating setup before using the evaluation board. The functions of the link options are summarized in Table 1.

Table 1. Link Option Functions

Link No.	Function
LK1	Controls the program $\overline{H}$/S SEL pin on the AD7656-1/AD7657-1/AD7658-1. In Position A, the AD7656-1/AD7657-1/AD7658-1 operates in software mode. In Position B, the AD7656-1/AD7657-1/AD7658-1 operates in hardware mode.
LK2	Selects the source of the REFIN voltage to be applied to the REFIN pin of the AD7656-1/AD7657-1/AD7658-1. In Position A, the AD780/ADR431 supplies the +2.5 V reference to the AD7656-1/AD7657-1/AD7658-1. The signal from the AD780/ADR431 is unbuffered. In Position B, the REF_{IN} is a buffered signal from the AD780/ADR431.
LK3	Selects the source of the $\overline{WR}/REF_{EN/\overline{DIS}}$ signal for the AD7656-1/AD7657-1/AD7658-1. In Position A, the $\overline{WR}/REF_{EN/\overline{DIS}}$ signal is taken from C9 of the 96-way connector to the EVAL-CONTROL BRD2. In Position B, the $\overline{WR}/REF_{EN/\overline{DIS}}$ signal is taken from the external $\overline{WR}$ SMB connector. In Position C, the $\overline{WR}/REF_{EN/\overline{DIS}}$ signal is taken from DGND, thus disabling the internal reference when operating in hardware mode. In Position D, the $\overline{WR}/REF_{EN/\overline{DIS}}$ signal is taken from VDRIVE, thus enabling the internal reference when operating in hardware mode.
LK4, LK5, LK14, LK15, LK17, LK18	Ties the op amp input to AGND at the VIN1 to VIN6 input sockets. When inserted, the AD797 positive input is tied to AGND. When removed, the positive input to the op amp is tied to the SMB input sockets for V1 to V6.
LK6	Selects the analog input range for the AD7656-1/AD7657-1/AD7658-1. In Position A, the analog input range for the AD7656-1/AD7657-1/AD7658-1 is ±5 V. In Position B, the analog input range for the AD7656-1/AD7657-1/AD7658-1 is ±10 V.
LK7	Places the AD7656-1/AD7657-1/AD7658-1 in $\overline{STBY}$ mode. In Position A, the AD7656-1/AD7657-1/AD7658-1 remains fully powered up at all times. In Position B, the AD7656-1/AD7657-1/AD7658-1 enters standby mode.
LK8	Selects the source of the RESET signal to the AD7656-1/AD7657-1/AD7658-1. In Position A, RESET is tied to VDRIVE, thus resetting the AD7656-1/AD7657-1/AD7658-1 In Position B, RESET is tied to AGND. In Position C, RESET comes from the FL1 flag, from the DSP through the 96-way connector (B1).
LK9	Sets the configuration of the parallel interface to word or byte mode. In Position A, the AD7656-1/AD7657-1/AD7658-1 operates in byte mode. In Position B, the AD7656-1/AD7657-1/AD7658-1 operates in word mode.

Link No.	Function
LK10	Selects the destination for the BUSY signal from the AD7656-1/AD7657-1/AD7658-1. In Position A, the BUSY signal is sent to the 96-way connector (C17). In Position B, the BUSY signal is sent to the J14 SMB BUSY connector.
LK11, LK34, LK35	Selects the source of the CONVST A, B, C signal. In Position A, the CONVST A, B, C signal is taken from the J32/J33/J34 CONVST A/B/C SBM connectors, respectively. In Position B, the CONVST A, B, C signal is taken from the 96-way connector (A17).
LK12	Selects the source of the VDRIVE supply for the AD7656-1/AD7657-1/AD7658-1. In Position A, the VDRIVE is taken from the DVCC supply voltage. In Position B, the VDRIVE is taken from the external J5 connector.
LK13	Selects the source of the reference for the AD7656-1/AD7657-1/AD7658-1 when the internal reference is disabled. In Position A, the AD780 is selected as the reference for the AD7656-1/AD7657-1/AD7658-1. In Position B, the ADR431 is selected as the reference for the AD7656-1/AD7657-1/AD7658-1.
LK16	Selects the source of the DVCC supply. In Position A, the DVCC for the AD7656-1/AD7657-1/AD7658-1 is taken from the 96-way connector (A8, B8, C8). In Position B, the DVCC for the AD7656-1/AD7657-1/AD7658-1 is taken from the J7 external connector. In Position C, the DVCC for the AD7656-1/AD7657-1/AD7658-1 is taken from the AVCC supply.
LK19	Selects the source of the AVCC supply. In Position A, the AVCC supply is taken from the 96-way connector (A32, B32, C32). In Position B, the AVCC is taken from the J6 external connector.
LK20	Selects the source of the V_{DD} supply for the AD7656-1/AD7657-1/AD7658-1 and the AD797 op amps. In Position A, the V_{DD} supply is taken from the 96-way connector (C30). In Position B, V_{DD} is taken from the J8 external connector.
LK21	Selects the source of the V_{SS} supply for the AD7656-1/AD7657-1/AD7658-1 and the AD797 op amps. In Position A, the V_{SS} supply is taken from the 96-way connector (A30). In Position B, V_{SS} is taken from the J8 external connector.
LK22	Selects the source of the $\overline{CS}$ signal. In Position A, the $\overline{CS}$ signal comes from the J11 external connector. In Position B, the $\overline{CS}$ signal comes from the 96-way connector (C10).
LK23	Selects the source of the $\overline{RD}$ signal for the AD7656-1/AD7657-1/AD7658-1. In Position A, the $\overline{RD}$ signal is taken from the 96-way connector (A9). In Position B, the $\overline{RD}$ signal is taken from the J12 external connector.
LK24	Controls application of a buffered reference signal to the REFCAP A, B, and C pins. A buffered reference signal can only be selected when the internal reference and reference buffers are disabled. When inserted, the buffered reference signal is applied to the REFCAP A, B, and C pins. The solder links between the REFCAP pins must be inserted for this mode. When removed, the internal reference buffers are enabled and the buffered reference signal is available at the REFCAP A, B, and C pins.
LK25	Selects the destination of the DB10/DOUT C interface line. In Position A, the DB10/DOUT C pin is tied to Pin 33 of U2. In Position B, the DB10/DOUT C pin is tied to the J17 external connector.
LK26	Sets the function of the DB7/HBEN/DCEN pin. In Position A, the pin acts as a DB7 of the 16-bit parallel bus connecting to Pin 37 of U2. In Position B, the pin is tied to VDRIVE. When in parallel byte mode, HBEN is set high, selecting the MSB data byte to come first from the AD7656-1/AD7657-1/AD7658-1. In serial mode, DCEN is set high, placing the device into daisy chain mode. In Position C, this pin is tied to DGND. When in parallel byte mode, HBEN is set low, selecting the LSB data byte to come first from the AD7656-1/AD7657-1/AD7658-1. In serial mode, DCEN is set low, keeping the AD7656-1/AD7657-1/AD7658-1 in serial mode only.
LK27	Selects the destination for the DB9/DOUT B. In Position A, the DB9/DOUT B is tied to Pin 35 of U2.

Link No.	Function
	In Position B, the DB9/DOUT B is tied to the 96-way connector (C1). In Position C, the DB9/DOUT C is tied to the J16 external connector.
LK28	Selects the destination for the DB8/DOUT A. In Position A, the DB8/DOUT A is tied to Pin 36 of U2. In Position B, the DB8/DOUT A is tied to the 96-way connector (C5). In Position C, the DB8/DOUT A is tied to the J15 external connector.
LK29	Selects the destination for the DB14/ $REFBUF_{EN/\overline{DIS}}$. In Position A, the DB14 is tied to Pin 27 of U2. In Position B, the DB14 is tied to VDRIVE. In serial mode, this position is used to disable the internal reference buffers. In Position C, the DB14 is tied to DGND. In serial mode, this position is used to enable the internal reference buffers.
LK30	Selects the destination of DB6 and the source of the SCLK signal in serial mode. In Position A, DB6 is connected to Pin 38 of U2. In Position B, the SCLK signal is taken from the 96-way connector (A7), serial mode only. In Position C, the SCLK signal is taken from the J19 external connector.
LK31	Selects the destination of DB2 and the source of the SEL C signal in serial mode. In Position A, DB2 is connected to Pin 44 of U2. In Position B, the SEL C signal is connected to VDRIVE, configuring the AD7656-1/AD7657-1/AD7658-1 with three DATA OUTPUT lines in serial mode. In Position C, the SEL C signal is connected to DGND, configuring the AD7656-1/AD7657-1/AD7658-1 with two/one DATA OUTPUT line(s) in serial mode.
LK32	Selects the destination of DB1 and the source of the SEL B signal in serial mode. In Position A, DB1 is connected to Pin 46 of U2. In Position B, the SEL B signal is connected to VDRIVE, configuring the AD7656-1/AD7657-1/AD7658-1 with two DATA OUTPUT lines in serial mode. In Position C, the SEL B signal is connected to DGND, configuring the AD7656-1/AD7657-1/AD7658-1 with one DATA OUTPUT line in serial mode.
LK33	Selects the destination of DB0 and the source of the SEL A signal in serial mode. In Position A, DB0 is connected to Pin 47 of U2. In Position B, the SEL A signal is connected to VDRIVE, configuring the AD7656-1/AD7657-1/AD7658-1 with one DATA OUTPUT line in serial mode. In Position C, the SEL C signal is connected to DGND. This option is not allowed in serial mode.
LK36, LK37	When inserted, CONVST A, CONVST B, and CONVST C are tied together.
LK38	Programs the interface on the AD7656-1/AD7657-1/AD7658-1. In Position A, the AD7656-1/AD7657-1/AD7658-1 operates in serial mode. In Position B, the AD7656-1/AD7657-1/AD7658-1 operates in parallel mode.
LK39	Programs the O/P Select pin on the AD780. When this link is inserted, the AD780 outputs a 3 V reference voltage. When removed, the AD780 outputs a 2.5 V reference.
LK40	Allows the user to apply an external reference to the REFIN/REFOUT pin on the AD7656-1/AD7657-1/AD7658-1. When this link is inserted, the reference source for the AD7656-1/AD7657-1/AD7658-1 comes from the AD780/ADR431 (the internal reference must be disabled). When removed, the internal reference is enabled and is available at the REFIN/REFOUT pin.
J21, J22, J24, J26, J28, J30	Solder link options that select between a buffered or unbuffered signal from the V1 to V6 SMB inputs to be applied to V1 to V6 on the AD7656-1/AD7657-1/AD7658-1. In Position A, a buffered signal is applied to the analog input pins on the AD7656-1/AD7657-1/AD7658-1. In Position B, an unbuffered signal is applied to the analog input pins on the AD7656-1/AD7657-1/AD7658-1.

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as required by the operating mode. Table 2 shows the positions in which all the links are set when the evaluation board is packaged. The board is set up for parallel mode operation.

Operating in ±10 V Mode

Note that the V_{DD} and V_{SS} supplies for the ±10 V range need to be ±15 V for the AD797. To ensure ±15 V supplies from the controller board, LK1 and LK2 on the EVAL-CONTROL BRD2 must be removed.

Table 2. Initial Link Positions

Link No.	Position	Function
LK1	B	Hardware mode selected.
LK2	A	AD780 supplies the reference to the AD7656-1/AD7657-1/AD7658-1.
LK3	D	Internal reference enabled.
LK4, LK5, LK14, LK15, LK17, LK18	Inserted	Inputs to AD797 op amps gounded. These must be removed when signals are applied to the V1 to V6 SMB sockets.
LK6	B	±10 V range selected for the AD7656-1/AD7657-1/AD7658-1.
LK7	A	AD7656-1/AD7657-1/AD7658-1 remains fully powered up.
LK8	C	RESET is taken from the 96-way connector.
LK9	B	AD7656-1/AD7657-1/AD7658-1 interface operates in word mode.
LK10	A	BUSY signal goes to the 96-way connector.
LK11, LK34, LK35	B	CONVST A,B,C is taken from the 96-way connector.
LK12	A	VDRIVE is taken from the DVCC supply.
LK13	A	AD780 is the external reference source.
LK16	A	DVCC is taken from the 96-way connector.
LK19	A	AVCC is taken from the 96-way connector.
LK20	A	V_{DD} is taken from the 96-way connector.
LK21	A	V_{SS} is taken from the 96-way connector.
LK22	B	$\overline{CS}$ comes from the 96-way connector.
LK23	A	$\overline{RD}$ comes from the 96 Way Connector.
LK24	Removed	Internal reference and reference buffers are enabled.
LK25	A	DB10 is tied to Pin 33 of U2.
LK26	A	DB7 is tied to Pin 37 of U2.
LK27	A	DB9 is tied to Pin 35 of U2.
LK28	A	DB8 is tied to Pin 36 of U2.
LK29	A	DB14 is tied to Pin 27 of U2.
LK30	A	DB8 is tied to Pin 38 of U2.
LK31	A	DB2 is tied to Pin 44 of U2.
LK32	A	DB1 is tied to Pin 46 of U2.
LK33	A	DB0 is tied to Pin 47 of U2.
LK36, LK37	Removed	CONVST signals are not connected together.
LK38	B	AD7656-1/AD7657-1/AD7658-1 operates in serial mode.
LK39	Removed	AD780 outputs a 2.5 V reference.
LK40	Removed	AD7656-1/AD7657-1/AD7658-1 operates with internal reference.
J21, J22, J24, J26, J28, J30	A	All input signals are buffered.

OPERATING WITH THE EVAL-CONTROL BRD2

The evaluation board can be operated in a standalone mode or operated in conjunction with the EVAL-CONTROL BRD2. All supplies and control signals that operate the AD7656-1/AD7657-1/AD7658-1 are provided by the EVAL-CONTROL BRD2 when it is run under the control of the AD7656-1/AD7657-1/AD7658-1 evaluation board package. The EVAL-CONTROL BRD2 can also operate with all Analog Devices evaluation boards that contain the letters CB in their part numbers. The software for the AD7656-1/AD7657-1/AD7658-1 evaluation board is limited to a 170 kSPS throughput rate. This is a limitation of the software and not the AD7656-1/AD7657-1/AD7658-1.

The evaluation board software should be installed on the PC, and the evaluation board and EVAL-CONTROL BRD2 should be connected together, before the EVAL-CONTROL BRD2 is connected to the PC, as follows:

1. Install the EVAL-AD7656-1/AD7657-1/AD7658-1 evaluation board software (see the Evaluation Board Software section).
2. Connect the evaluation board and the EVAL-CONTROL BRD2 via the 96-way connector.
3. Apply power to the EVAL-CONTROL BRD2 via a 12 V transformer. At this stage, the red LED on the EVAL-CONTROL BRD2 should be flashing, which indicates that the EVAL-CONTROL BRD2 is functional and ready to receive instructions.
4. Connect the printer port between the PC and EVAL-CONTROL BRD2.

CONNECTING TO THE EVALUATION BOARD

Interfacing for the evaluation board is via a 96-way connector, J1. J1 is used to connect the AD7656-1/AD7657-1/AD7658-1 evaluation board to the EVAL-CONTROL BRD2 or to another system. The pinout for the J1 connector is shown in Figure 2, and its pin designations are given in Table 4.

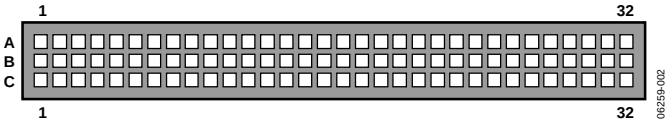

Figure 2. Pin Configuration for the 96-Way Connector J1

Table 3. 96-Way Connector Pin Signals

Signal	Description
TFS0, RFS	Transmit/Receive Frame Sync 0. These two outputs are connected to the $\overline{CS}$ pin of the AD7656-1/AD7657-1/AD7658-1 in serial mode.
SCLK	Serial Clock 0. This serial clock is connected to the SCLK pin on the AD7656-1/AD7657-1/AD7658-1 in serial mode.
DR0	Data Receive 0. This input is connected to the DOUT pin of the AD7656-1/AD7657-1/AD7658-1 in serial mode.
DT0	Data Transmit 0. This output is connected to the DCIN pin on the AD7656-1/AD7657-1/AD7658-1 in serial mode.
AGND	Analog Ground. These lines are connected to the analog ground plane on the evaluation board.
DGND	Digital Ground. These lines are connected to the digital ground plane on the evaluation board.
AVCC	Analog +5 V Supply. These lines are connected to the AVCC supply line on the AD7656-1/AD7657-1/AD7658-1 evaluation board.
DVCC	Digital +5 V Supply.
DB0 to DB15	Digital Parallel Data Bus.
$\overline{CS}$	Used as the $\overline{CS}$ signal for the parallel interface.
$\overline{RD}$	Used as the $\overline{RD}$ signal for the parallel interface.
$\overline{WR}$	Used as the $\overline{WR}$ signal for the parallel interface.
FL0	Used for the CONVST pins.
FL1	Used for the reset pulse.
−12 V/−15 V	−12 V Supply. This line is connected to the −12 V supply line on the evaluation board via LK21.
+12 V/+15 V	+12 V Supply. This line is connected to the +12 V supply line on the evaluation board via LK20.

Table 4. Pin Designations for the 96-Way Connector J1

Pin No.	Row A	Row B	Row C
1		FL1	
2		DB0	
3	SCLK1	DB1	SCLK1
4	DGND	DGND	DGND
5	DT0	DB2	DR0
6	TFS0	DB3	RFS0
7	SCLK0	DB4	SCLK0
8	DVCC	DVCC	DVCC
9	$\overline{RD}$	DB5	$\overline{WR}$
10		DB6	$\overline{CS}$
11		DB7	
12	DGND	DGND	DGND
13		DB8	
14		DB9	
15		DB10	
16	DGND	DGND	DGND
17	FL0	DB11	$\overline{IRQ2}$
18	DB12	DB13	DB14
19			DB15
20	DGND	DGND	DGND
21	AGND	AGND	AGND
22	AGND	AGND	AGND
23	AGND	AGND	AGND
24	AGND	AGND	AGND
25	AGND	AGND	AGND
26	AGND	AGND	AGND
27		AGND	
28		AGND	
29		AGND	
30	−12 V/−15 V	AGND	+12 V/+15 V
31			
32	AVCC	AVCC	AVCC

APPLYING POWER TO THE EVAL-CONTROL BRD2

The 96-way connector on the EVAL-AD7656-1/AD7657-1/AD7658-1 plugs directly into the 96-way connector on the EVAL-CONTROL BRD2. No power supplies are required in the system. The EVAL-CONTROL BRD2 generates all the required supplies for itself and the AD7656-1/AD7657-1/AD7658-1 evaluation board and is powered from a 12 V ac transformer. This is a standard 12 V ac transformer capable of supplying 1 A current and is available as an accessory from Analog Devices under the following part numbers:

- EVAL-110VAC-US (for use in the U.S. or Japan)
- EVAL-220VAC-UK (for use in the U.K.)
- EVAL-220VAC-EU (for use in Europe)

These transformers are also available from other suppliers including Digikey (U.S.) and Campbell Collins (U.K.)

CONNECTING THE EVAL-CONTROL BRD2 TO A PC

Connection between the EVAL-CONTROL BRD2 and the parallel port of a PC is via an IEEE 1284 compliant cable, which is provided as part of the EVAL-CONTROL BRD2 package. See the manual that accompanies the EVAL-CONTROL BRD2 for more details on this package.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-AD7656-1/AD7657-1/AD7658-1 evaluation kit includes a CD-ROM that contains software for controlling and evaluating the performance of the AD7656-1/AD7657-1/AD7658-1 when it operates with the EVAL-CONTROL BRD2.

When the CD is inserted into the PC, an installation program automatically begins. This program installs the evaluation software, the data sheet for the AD7656-1/AD7657-1/AD7658-1 evaluation board, the data sheet for the AD7656-1/AD7657-1/AD7658-1, and the data sheet for the EVAL-CONTROL BRD2 onto the user's machine. All literature on the CD is in Adobe Portable Documentation Format (PDF) and requires Acrobat Reader to be viewed or printed. The user interface on the PC is a dedicated program written especially for the AD7656-1/AD7657-1/AD7658-1 when operated with the EVAL-CONTROL BRD2.

The software that controls the EVAL-CONTROL BRD2, and therefore the AD7656-1/AD7657-1/AD7658-1, has two windows. The main window, shown in Figure 3, is the window that appears when the software is run. It is used to access the **Load Configuration** window, where you can load a configuration file and choose the sampling frequency and the number of samples to take from the evaluation board (see Figure 4). The main window is also used to read the predetermined frequency and number of samples and to display time information for them.

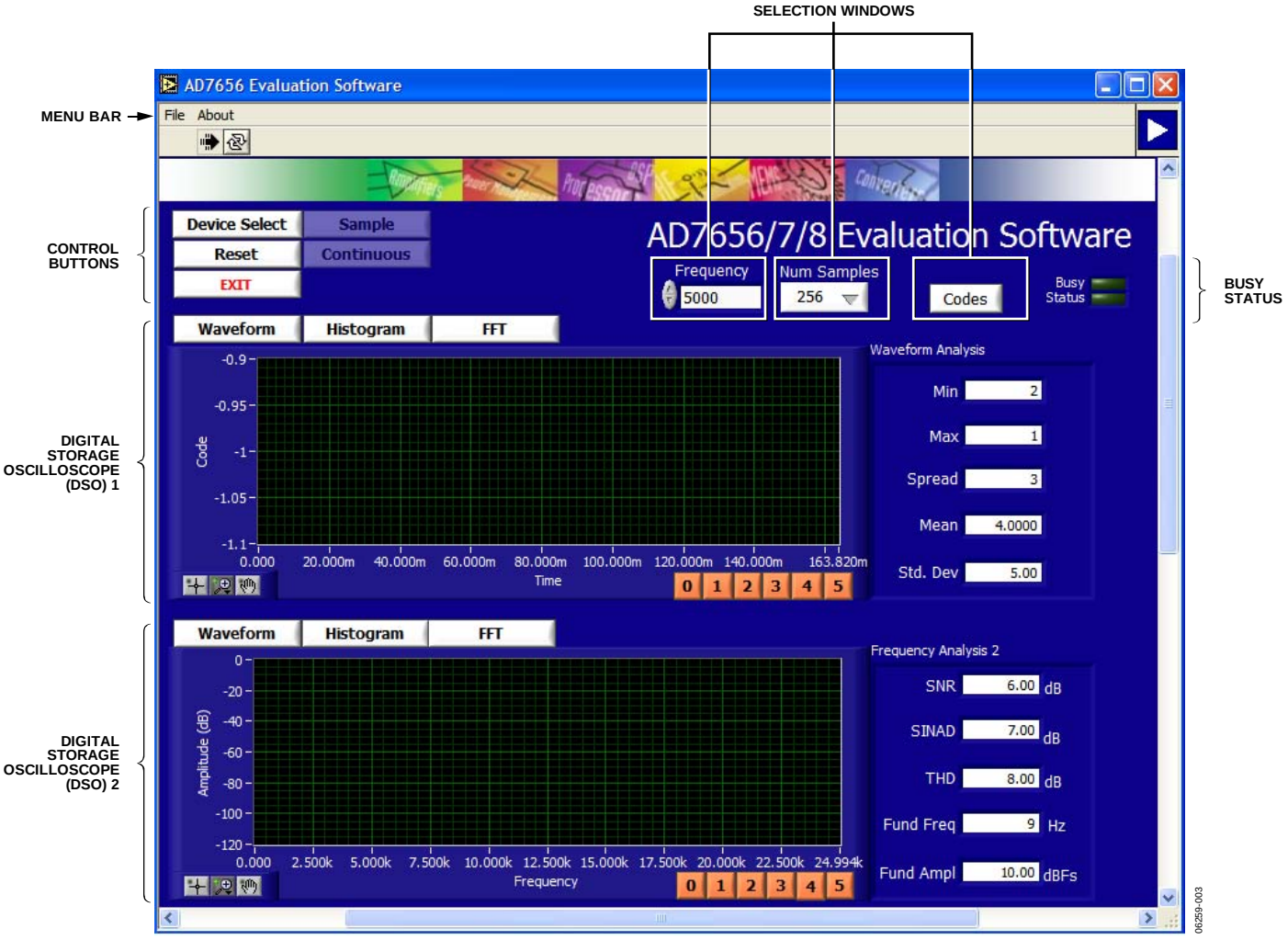

Figure 3. AD7656-1/AD7657-1/AD7658-1 Evaluation Software, Main Window

CONFIGURING THE EVALUATION BOARD

The **Load Configuration** window is used to change the required configuration file for the evaluation board and load the changes. This window is shown in Figure 4.

The configuration file is a text-based file that gives the software detailed information about the AD7656-1/AD7657-1/AD7658-1 evaluation board and the connection to the EVAL-CONTROL BRD2, such as the number of bits, the maximum sampling rate, maximum sampling rate, and power supply requirements. The configur-ation file also gives the software the name of the DSP program file that it should download to the EVAL-CONTROL BRD2.

CHANGING AND LOADING THE CONFIGURATION FILE

To change the configuration file, follow these steps:

1. After the software is installed and running, click the **Device Select** control button in the main window. This displays the **Load Configuration** window (see Figure 4).
2. The **Select a Configuration File** list box at the top left of the window lists the available configuration files. The file for the AD7656-1/AD7657-1/AD7658-1 evaluation board is listed in this box, and part information and program information are displayed in the **Part Name** box and the **Program Name** box. To change the settings for the configuration file, change the values for any of the following controls by entering a number in the box or using the up/down arrow buttons:
   - **Sample Frequency**
   - **Max Sample Frequency**
   - **Num Samples**
   - **Num Bits**
   - **Input V Max**
   - **Input V Min**
   - **AVDD**
   - **DVDD**
   - **±12 V**
   - **Bus**
3. After changing the settings, click **OK**. The EVAL-CONTROL BRD2 is reset.

Note that the sample frequency and the number of samples can also be changed in the main window (see the Taking and Reading Samples with the Evaluation Board section).

Figure 4. AD7656-1/AD7657-1/AD7658-1 Evaluation Software, Load Configuration Window

Software Configuration File

The following is a typical software configuration file (*.cfg):

```
[EVAL-CONTROL BOARD]
partname:AD7656
programname:AD7656.PRG

samplefrequency:50000
maxsamplefrequency:250000
samples:8192

+/-12V:on
dvdd:5:on
avdd:5:on
bus:on
;options 2scomp, binary
dataformat:2scomp
numberofbits:16
inputVmax:+10
inputVmin: -10
[endofconfig]
```

TAKING AND READING SAMPLES WITH THE EVALUATION BOARD

The main window is used to display and read samples and additionally control the EVAL-CONTROL BRD2 and the AD7656-1/AD7657-1/AD7658-1 evaluation board.

As shown in Figure 3, the main window consists of three main sections. The top section contains a menu bar, controls, and a status indicator. The middle and bottom sections contain digital storage oscilloscopes (DSOs).

Menu Bar

File Menu

Load Raw Data. Loads data that was saved by the software during a previous session.

Save Raw Data. Saves the current set of sample data points. The data can be reloaded to the evaluation board at a later date or can be used by other programs for further analysis.

Save Binary Data. Saves the current set of sample data points. The data is saved in binary format as a text file. This method can be useful for examining code flicker, looking for stuck bits, and other analysis.

Exit. Quits the program.

About Menu

The **About** drop-down menu provides information about the current version of the software.

Controls

Device Select. Opens the Load Configuration window (see the Configuring the Evaluation Board section).

Sample. Starts the sampling process (see the Taking Samples section).

Reset. Resets the evaluation board.

Continuous. Repeats the sampling process.

Exit. Exits the program.

Frequency. Changes the sampling frequency and displays the speed at which the evaluation board is running, which you can change.

Num Samples. Changes the number of samples to upload.

Codes/Volts. Determines whether data is displayed in codes or in volts.

Busy Status. Indicates whether the evaluation board is busy.

Digital Storage Oscilloscopes (DSO)

The upper DSO displays a waveform, a histogram, or a fast Fourier transform (FFT). When samples are uploaded from the evaluation board, they are displayed here. At the bottom left of the DSO are zoom options that can be used to zoom in and out while viewing a sample. To the right of this DSO, information about the sample taken, such as minimum and maximum position or velocity, spread, mean, and standard deviation, is displayed.

The lower DSO, by default, displays an FFT, which can be used to examine frequency patterns. A waveform or a histogram of performance in response to dc inputs can also be displayed. At the bottom left of the DSO are zoom options that can be used to zoom in and out while viewing a sample. To the right of the DSO, information about the sample taken, such as signal-to-noise ratio and other ac specifications, is displayed.

Taking Samples

When the **Sample** button in the main window is clicked, **Stop** replaces **Sample**, and the EVAL-CONTROL BRD2 is instructed to take the required number of samples at the required frequency from the evaluation board. The AD7656-1/AD7657-1/AD7658-1 evaluation board runs up to 170 kSPS. You can choose the sampling frequency up to this rate and the number of samples to be taken.

The samples taken are then uploaded and displayed. An FFT and a histogram are also calculated and displayed. When the **Continuous** button in the main window is clicked, the software repeats the process indefinitely until the **Stop** button is clicked.

EVALUATION BOARD SCHEMATICS AND ARTWORK

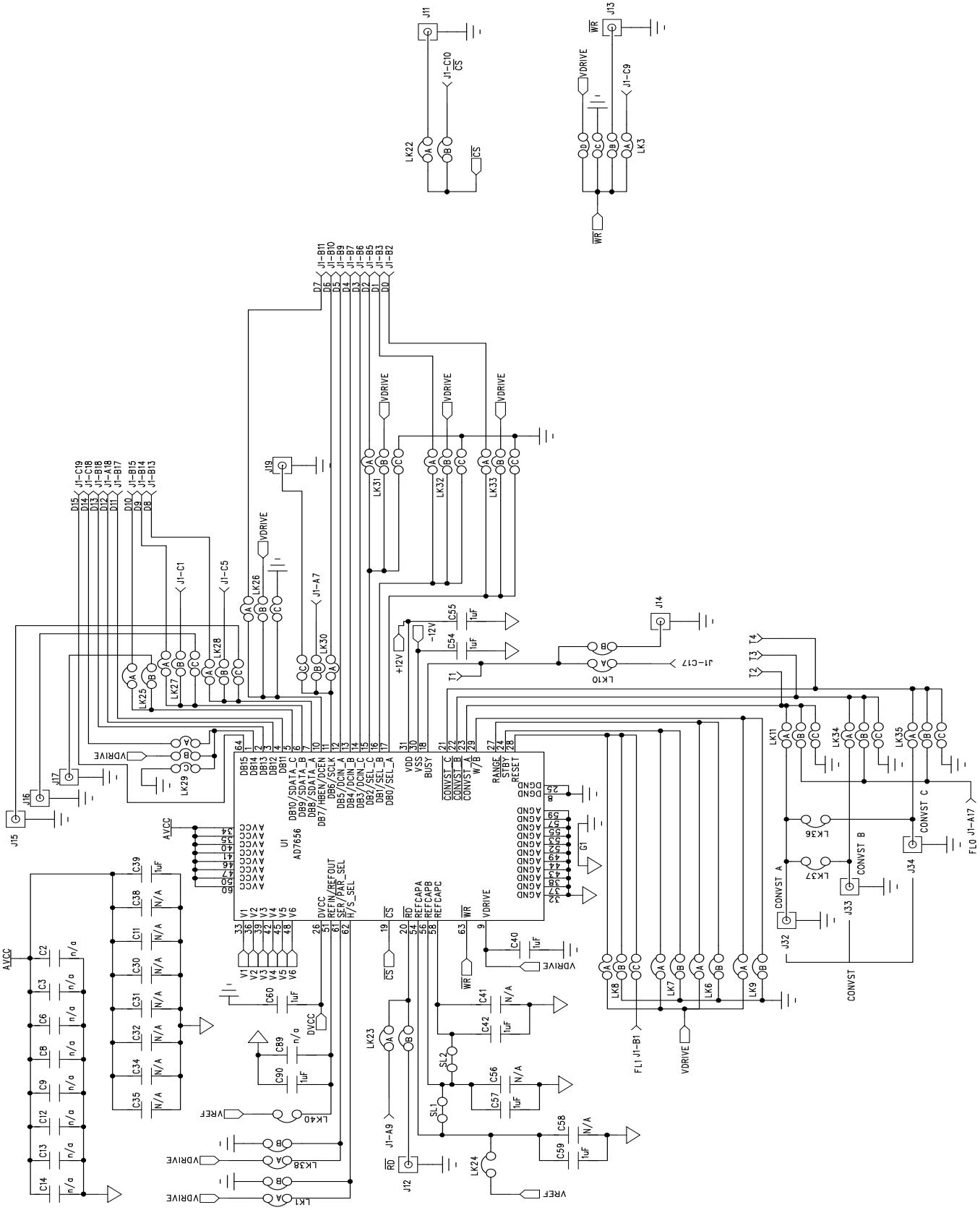

Figure 5. AD7656-1/AD7657-1/AD7658-1 Evaluation Board Schematic 1

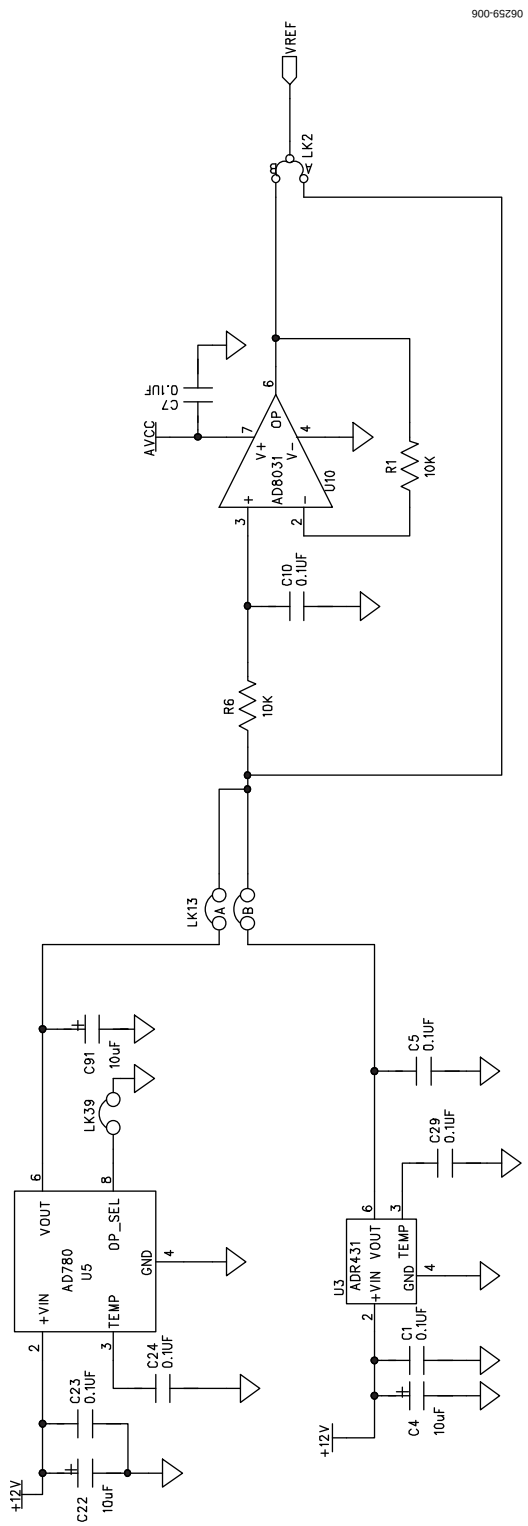

Figure 6. AD7656-1/AD7657-1/AD7658-1 Evaluation Board Schematic 2

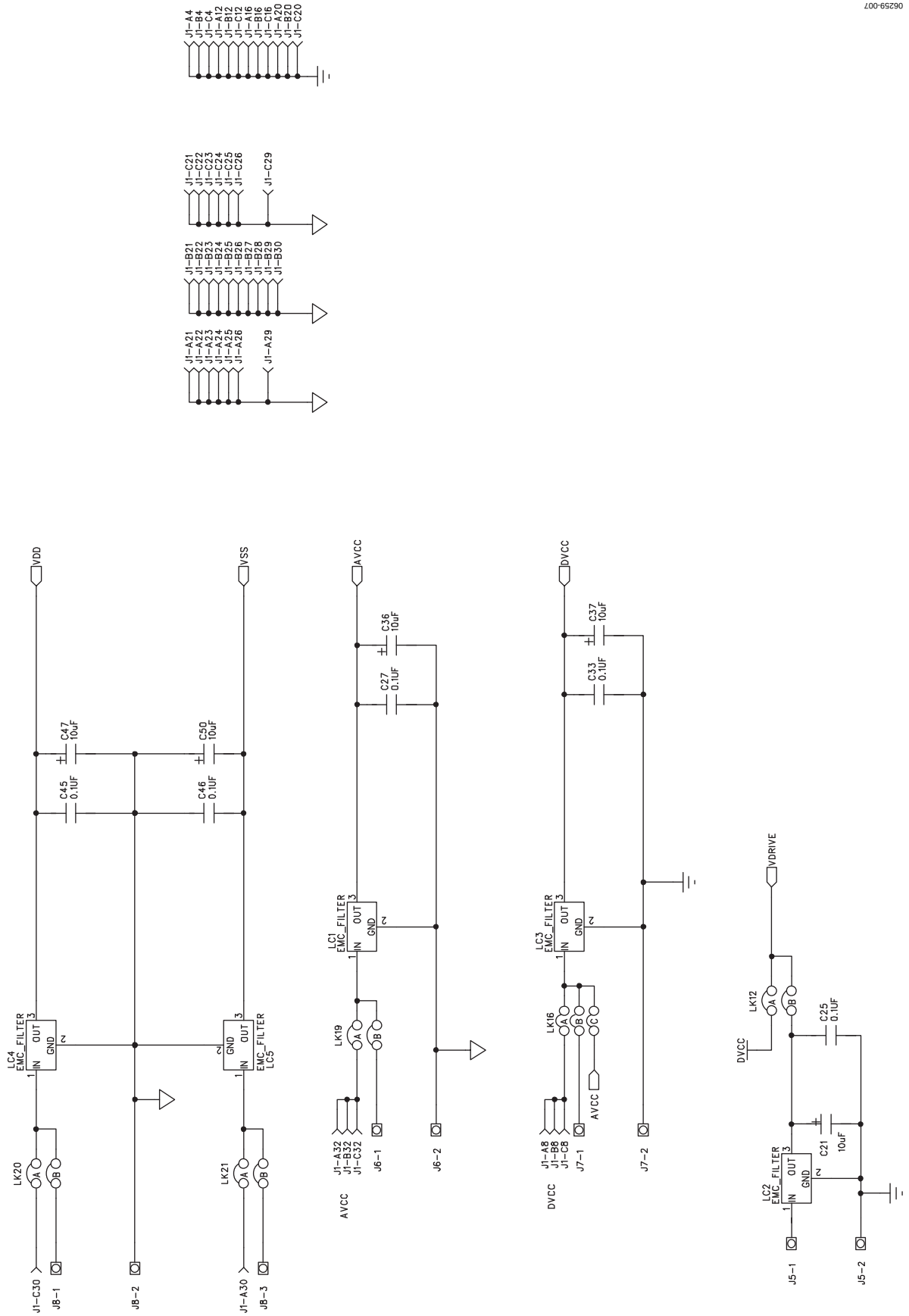

Figure 7. AD7656-1/AD7657-1/AD7658-1 Evaluation Board Schematic 3

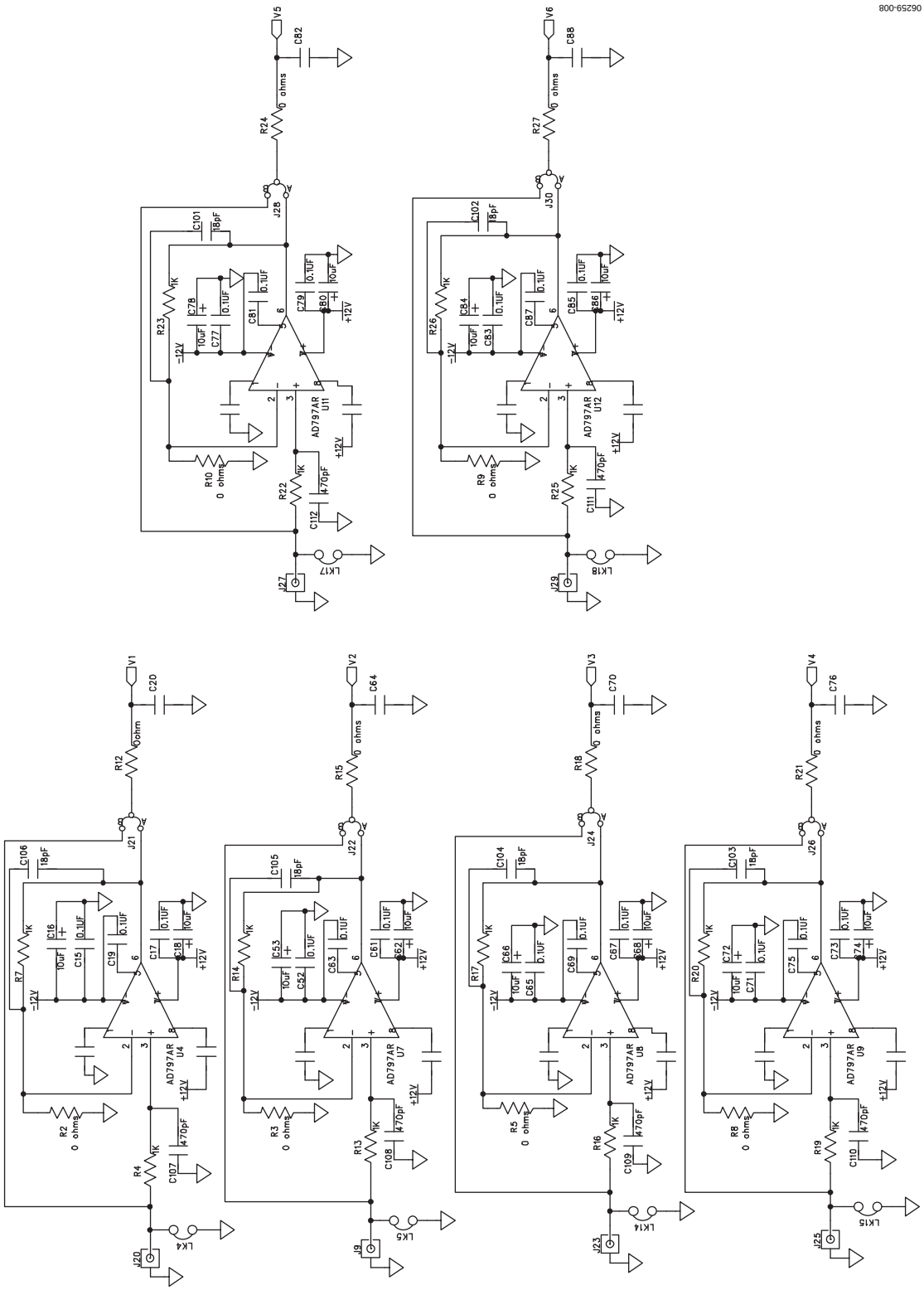

Figure 8. AD7656-1/AD7657-1/AD7658-1 Evaluation Board Schematic 4

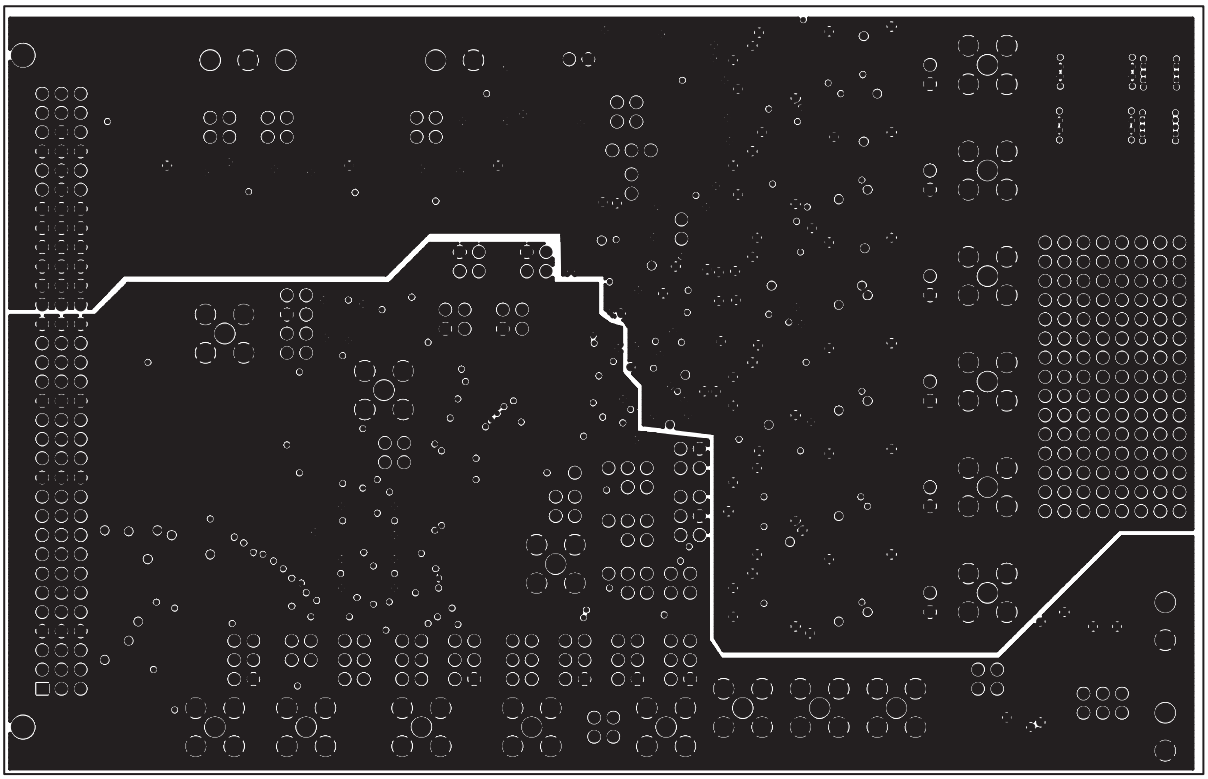

Figure 9. Inner Layer Ground Planes

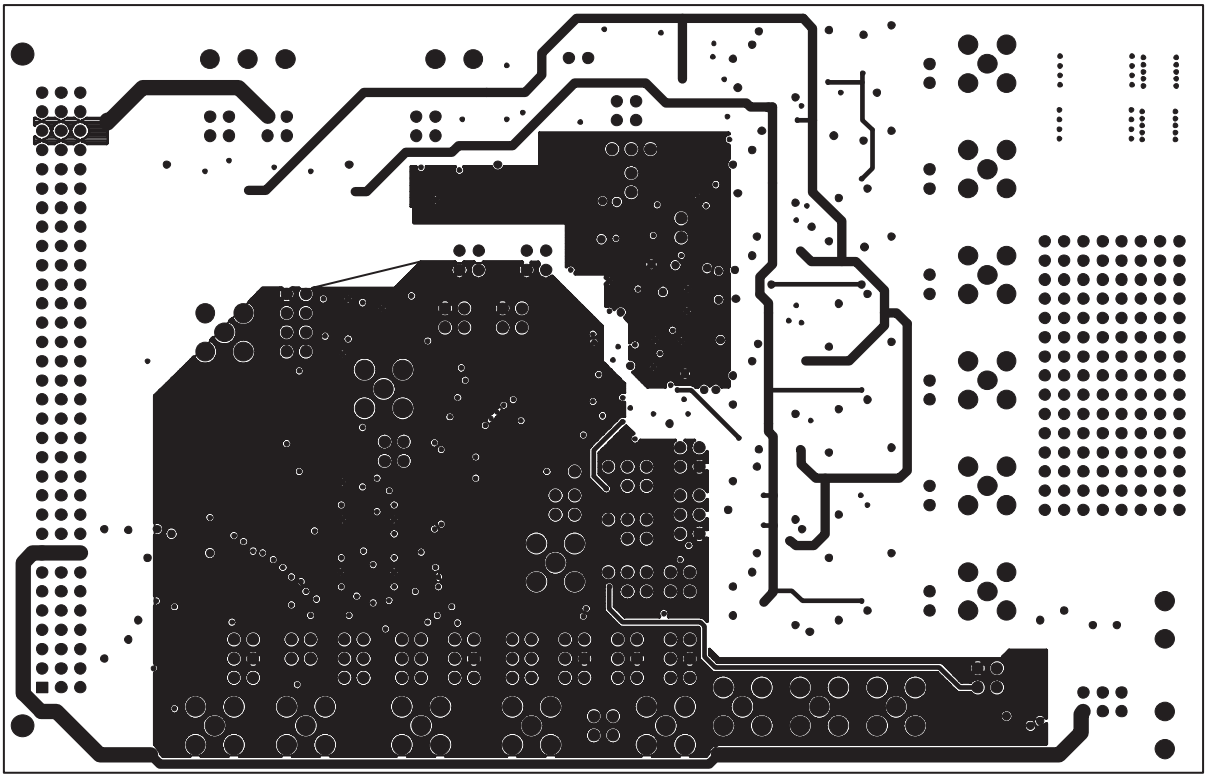

Figure 10. Bottom Layer Etch

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
EVAL-AD7656-1CBZ[1]	AD7656-1 Evaluation Board
EVAL-AD7657-1CBZ[1]	AD7657-1 Evaluation Board
EVAL-AD7658-1CBZ[1]	AD7658-1 Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

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EB07870-0-10/08(PrA)