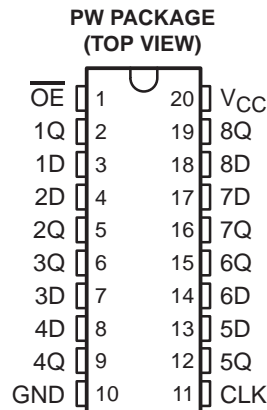


SN74LV374A-Q1 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCLS468B – FEBRUARY 2003 – REVISED MAY 2004

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Typical V_{OLP} (Output Ground Bounce) $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $>2.3\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

† Contact factory for details. Q100 qualification data available on request.



description/ordering information

The SN74LV374A is an octal edge-triggered D-type flip-flop designed for 2-V to 5.5-V V_{CC} operation.

This device features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV374ATPWRQ1	LV374ATQ

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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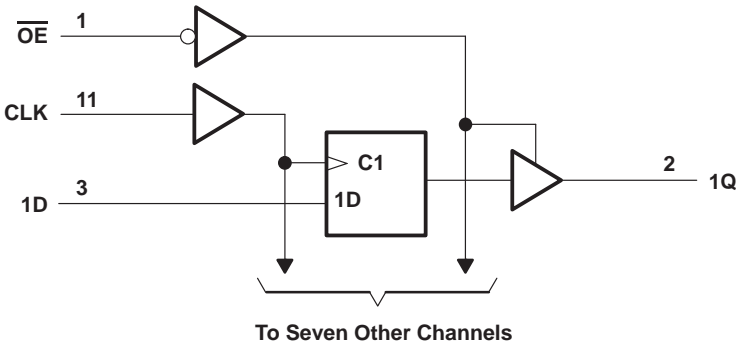
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FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3)	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	High or low state	0 V_{CC}	V
		3-state	0 5.5	
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$	–50	μA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	–2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	–8	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	–16	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$	50	μA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	8	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	16	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	200	ns/V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	100	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	20	
T_A	Operating free-air temperature	–40	105	$^{\circ}\text{C}$

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -50\text{ }\mu\text{A}$	2 V to 5.5 V	$V_{CC}-0.1$			V
	$I_{OH} = -2\text{ mA}$	2.3 V	2			
	$I_{OH} = -8\text{ mA}$	3 V	2.48			
	$I_{OH} = -16\text{ mA}$	4.5 V	3.8			
V_{OL}	$I_{OL} = 50\text{ }\mu\text{A}$	2 V to 5.5 V			0.1	V
	$I_{OL} = 2\text{ mA}$	2.3 V			0.4	
	$I_{OL} = 8\text{ mA}$	3 V			0.44	
	$I_{OL} = 16\text{ mA}$	4.5 V			0.55	
I_I	$V_I = 5.5\text{ V or GND}$	0 to 5.5 V			± 1	μA
I_{OZ}	$V_O = V_{CC}\text{ or GND}$	5.5 V			± 5	μA
I_{CC}	$V_I = V_{CC}\text{ or GND, } I_O = 0$	5.5 V			20	μA
I_{off}	$V_I\text{ or }V_O = 0\text{ to }5.5\text{ V}$	0			5	μA
C_i	$V_I = V_{CC}\text{ or GND}$	3.3 V		2.9		pF



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timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
t_W	Pulse duration, CLK high or low	5		5.5		ns
t_{su}	Setup time, data before CLK \uparrow	4.5		4.5		ns
t_h	Hold time, data after CLK \uparrow	2		2		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
t_W	Pulse duration, CLK high or low	5		5		ns
t_{su}	Setup time, data before CLK \uparrow	3		3		ns
t_h	Hold time, data after CLK \uparrow	2		2		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			$C_L = 50\text{ pF}$	55	110		50		MHz
t_{pd}	CLK	Q		8.3	16.2		1	18.5	ns
t_{en}	\overline{OE}	Q		7.7	14.5		1	17.5	
t_{dis}	\overline{OE}	Q		5.9	14		1	16	
$t_{sk(o)}$					1.5				

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			$C_L = 50\text{ pF}$	85	170		75		MHz
t_{pd}	CLK	Q		5.9	10.1		1	13.5	ns
t_{en}	\overline{OE}	Q		5.5	9.6		1	13	
t_{dis}	\overline{OE}	Q		4	8.8		1	10	
$t_{sk(o)}$					1				



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noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.5	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	21.1	pF
			5 V	22.8	



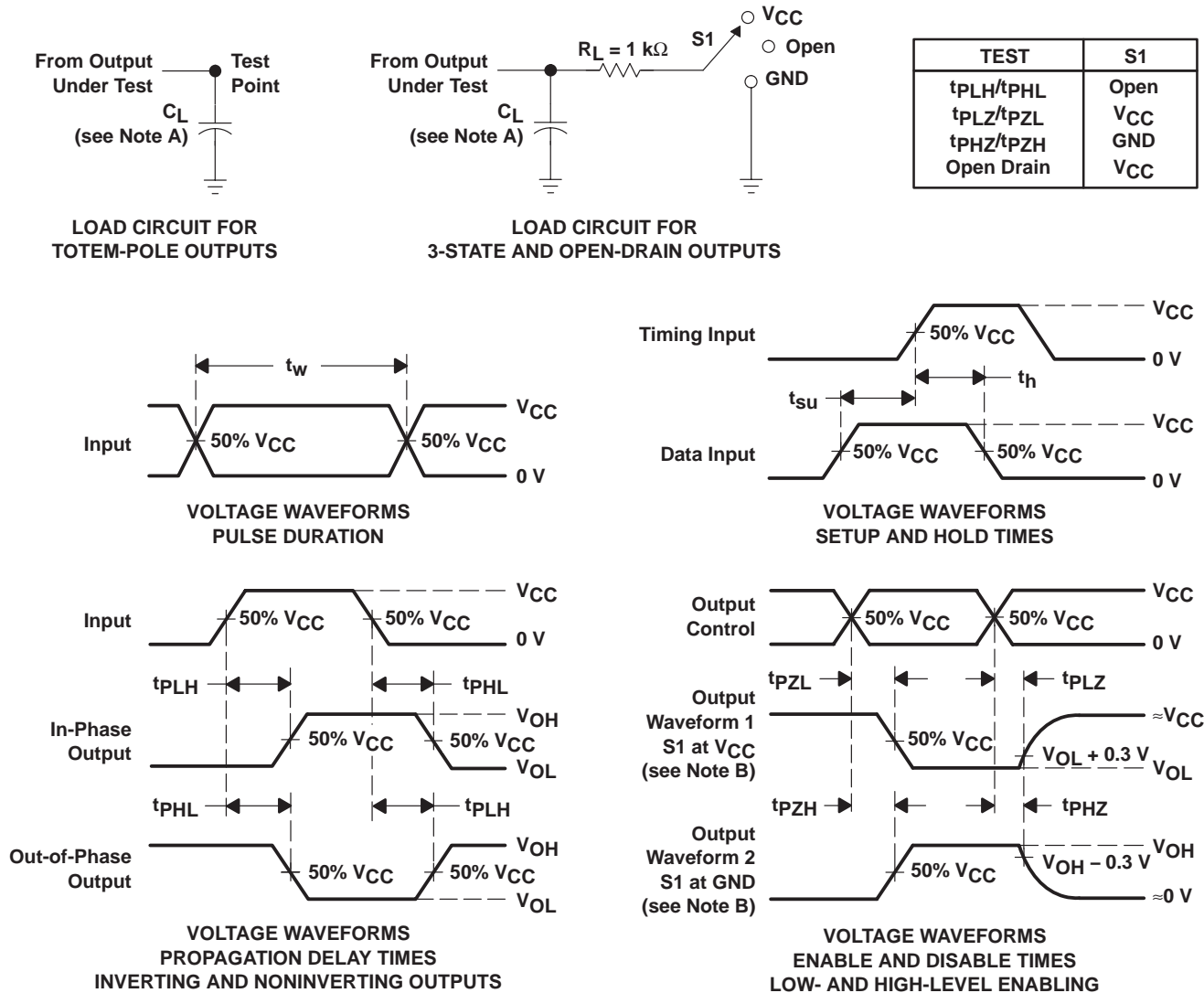
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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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