

✓ **54S/74S109** 011525
 ✓ **54LS/74LS109** 011524

DUAL J $\bar{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '109 consists of two high speed, completely independent transition clocked J $\bar{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J $\bar{K}$ design allows operation as a D flip-flop (refer to '74 data sheet) by connecting the J and $\bar{K}$ inputs together. The '109 is functionally equivalent to the 9024.

TRUTH TABLE

INPUTS		OUTPUTS	
@ t_n		@ $t_n + 1$	
J	K	Q	$\bar{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

Asynchronous Inputs:

LOW input to $\bar{S}_D$ sets Q to HIGH level
 LOW input to $\bar{C}_D$ sets Q to LOW level
 Clear and Set are independent of clock
 Simultaneous LOW on $\bar{C}_D$ and $\bar{S}_D$
 makes both Q and $\bar{Q}$ HIGH

t_n = Bit time before clock pulse.
 $t_n + 1$ = Bit time after clock pulse.
 H = HIGH Voltage Level
 L = LOW Voltage Level

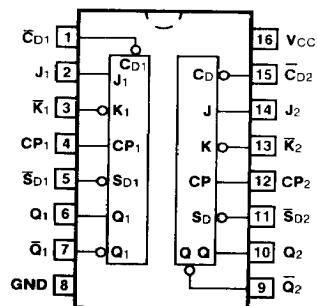
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C to } +70^\circ \text{C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%$, $T_A = -55^\circ \text{C to } +125^\circ \text{C}$	
Plastic DIP (P)	A	74S109PC, 74LS109PC		9A
Ceramic DIP (D)	A	74S109DC, 74LS109DC	54S109DM, 54LS109DM	6A
Flatpak (F)	A	74S109FC, 74LS109FC	54S109FM, 54LS109FM	3I

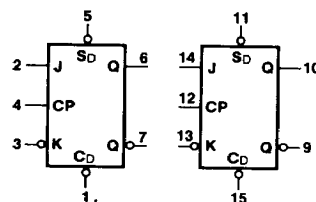
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$J_1, J_2, \bar{K}_1, \bar{K}_2$	Data Inputs	1.25/1.25	0.5/0.25
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	2.5/2.5	1.0/0.5
$\bar{C}_D1, \bar{C}_D2$	Direct Clear Inputs (Active LOW)	5.0/5.0	1.0/1.0
$\bar{S}_D1, \bar{S}_D2$	Direct Set Inputs (Active LOW)	2.5/2.5	1.0/0.5
$Q_1, Q_2, \bar{Q}_1, \bar{Q}_2$	Outputs	25/12.5	10/5.0 (2.5)

CONNECTION DIAGRAM PINOUT A

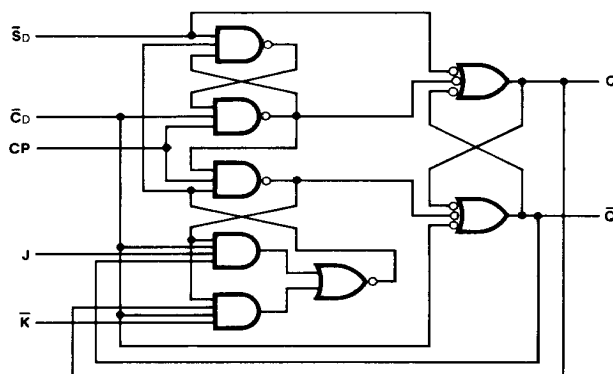


LOGIC SYMBOL



V_{CC} = Pin 16
 GND = Pin 8

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current	52		8.0		mA	$V_{CC} = \text{Max}, V_{CP} = 0 \text{ V}$

AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ \text{C}$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$			
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	75		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\bar{Q}_n$	9.0 11		25 35		ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q_n or $\bar{Q}_n$	6.0 12		15 35		ns	$V_{CP} \geq 2.0 \text{ V}$ Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to Q_n or $\bar{Q}_n$	6.0 12		15 24		ns	$V_{CP} \leq 0.8 \text{ V}$ Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ \text{C}$

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time J_n or $\bar{K}_n$ to CP_n	6.0		18		ns	Fig.3-6
t_h (H) t_h (L)	Hold Time J_n or $\bar{K}_n$ to CP_n	0		0		ns	
t_w (H) t_w (L)	CP_n Pulse Width	7.0 6.5		20 13.5		ns	Fig. 3-8
t_w (L)	$\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ Pulse Width LOW	6.0		15		ns	Fig. 3-10