BLS7G2729L-350P; BLS7G2729LS-350P

LDMOS S-band radar power transistor

Rev. 5 — 16 May 2014 Product data sheet

1. Product profile

1.1 General description

350 W LDMOS power transistor for S-band radar applications in the frequency range from 2.7 GHz to 2.9 GHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 300 μs; δ = 10 %; I_{Dq} = 200 mA; in a class-AB production test circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D	t_r	t_f
	(GHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
pulsed RF	2.7 to 2.9	32	350	13	50	8	5

1.2 Features and benefits

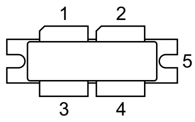
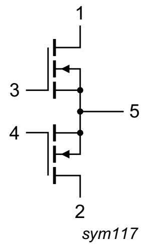
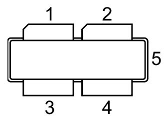
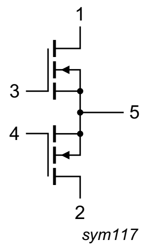
- High efficiency
- Excellent ruggedness
- Designed for S-band operation (2.7 GHz to 2.9 GHz)
- Excellent thermal stability
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- S-band radar applications in the frequent range 2.7 GHz to 2.9 GHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLS7G2729L-350P (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLS7G2729LS-350P (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS7G2729L-350P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLS7G2729LS-350P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	65	V
V_{GS}	gate-source voltage	–0.5	+11	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	T_{case} = 85 °C; P_L = 350 W		
		t_p = 100 μs; δ = 10 %	0.07	K/W
		t_p = 200 μs; δ = 10 %	0.09	K/W
		t_p = 300 μs; δ = 10 %	0.10	K/W
		t_p = 100 μs; δ = 20 %	0.09	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.2 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 220 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	39	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 11.0 A	-	16.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 7.7 A	-	0.065	-	Ω

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 300 μs; δ = 10 %; RF performance at V_{DS} = 32 V; I_{Dq} = 200 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 350 W	11	13	-	dB
RL_{in}	input return loss	P_L = 350 W	-	−10	-	dB
η_D	drain efficiency	P_L = 350 W	46	50	-	%
$P_{droop(pulse)}$	pulse droop power	P_L = 350 W	-	0	0.5	dB
t_r	rise time	P_L = 350 W	-	8	50	ns
t_f	fall time	P_L = 350 W	-	5	50	ns

7. Test information

7.1 Ruggedness in class-AB operation

The BLS7G2729L-350P and BLS7G2729LS-350P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 200 mA; P_L = 350 W; t_p = 300 μs; δ = 10 %.

7.2 Impedance information

Table 8. Typical impedance

f	Z_S [1]	Z_L [1]
GHz	Ω	Ω
2.7	2.8 – j8.7	1.8 – j5.1
2.8	3.9 – j8.2	2.1 – j5.4
2.9	4.8 – j9.3	1.5 – j5.7

[1] Impedances are taken at a single halve of the push-pull transistor

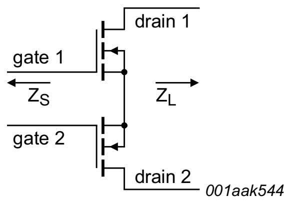
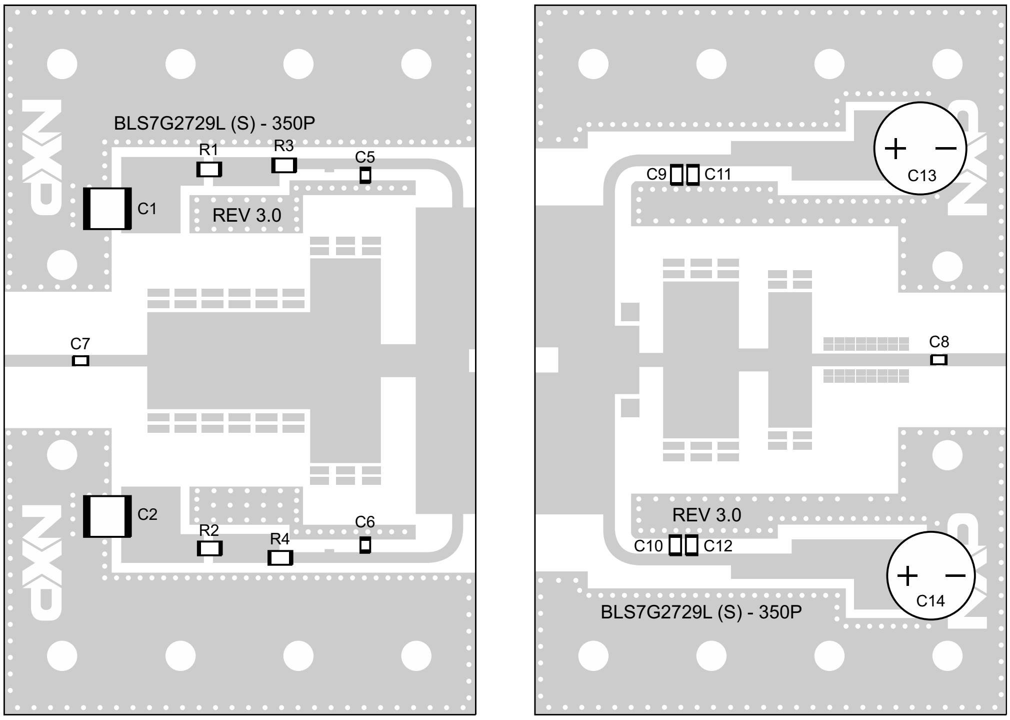


Fig 1. Definition of transistor impedance

7.3 Test circuit information



aaa-007604

Printed-Circuit Board (PCB): Rogers RO6006; ε_r = 6.45 F/m; thickness = 0.635 mm; thickness copper plating = 35 µm.

The vias can be used as a reference to place components.

The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided. See Table 9 for list of components.

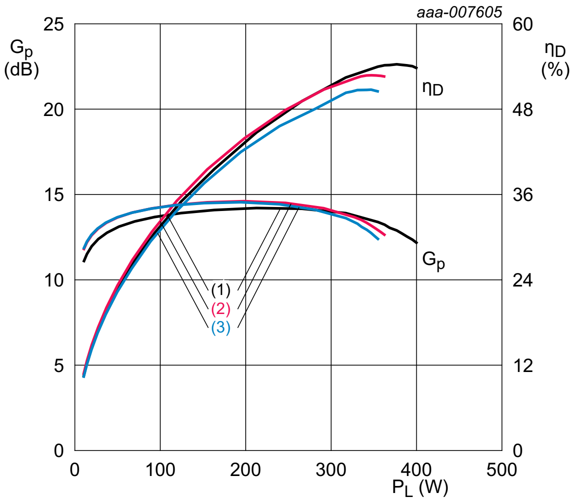
Fig 2. Component layout

Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2	SMD capacitor	4.7 µF, 50 V	
C5, C6	multilayer ceramic chip capacitor	12 pF	ATC800A
C7, C8	multilayer ceramic chip capacitor	20 pF	ATC800A
C9, C10	multilayer ceramic chip capacitor	12 pF	ATC800A
C11, C12	multilayer ceramic chip capacitor	1 nF	ATC700A
C13, C14	electrolytic capacitor	220 µF, 63 V	
R1, R2	SMD resistor	9.1 Ω	SMD 0805
R3, R4	SMD resistor	8 Ω	SMD 0805

7.4 Graphical data



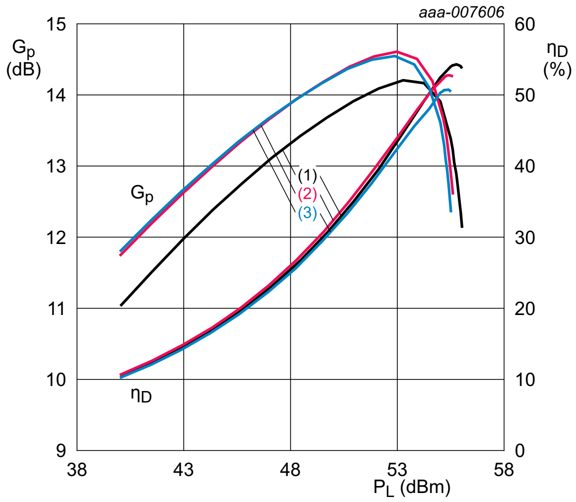
V_{DS} = 32 V; I_{Dq} = 200 mA.

(1) f = 2.7 GHz

(2) f = 2.8 GHz

(3) f = 2.9 GHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



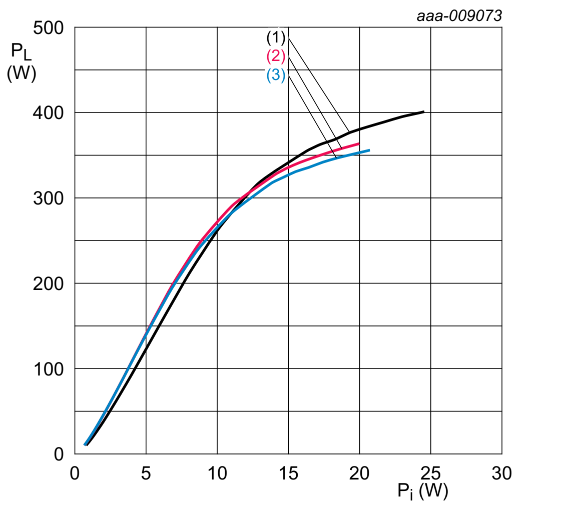
V_{DS} = 32 V; I_{Dq} = 200 mA.

(1) f = 2.7 GHz

(2) f = 2.8 GHz

(3) f = 2.9 GHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



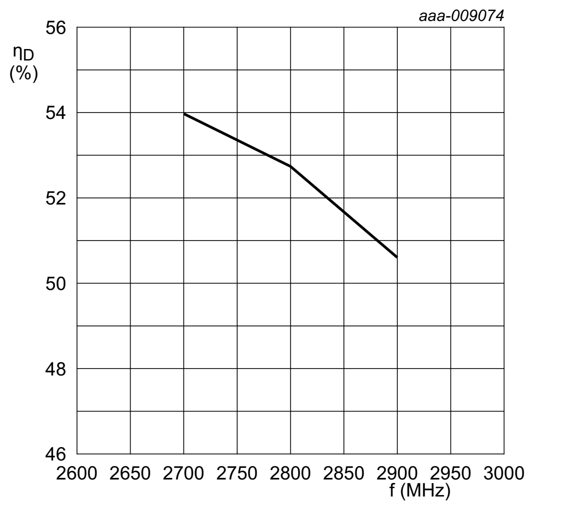
V_{DS} = 32 V; I_{Dq} = 200 mA; t_p =300 µs; δ = 10 %.

(1) f = 2.7 GHz

(2) f = 2.8 GHz

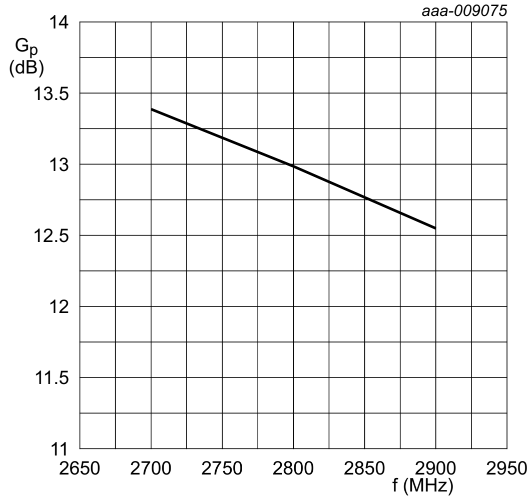
(3) f = 2.9 GHz

Fig 5. Output power as a function of input power; typical values



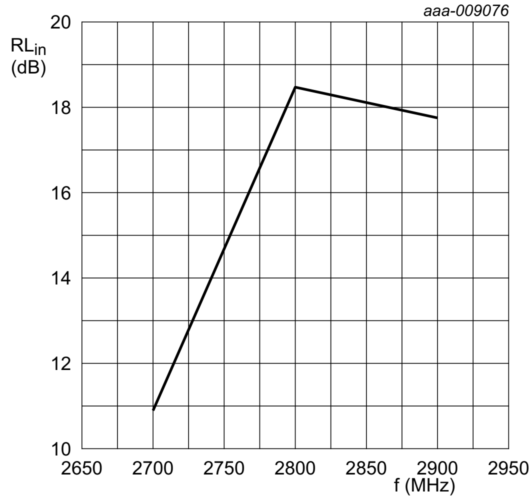
V_{DS} = 32 V; I_{Dq} = 200 mA; t_p = 300 µs; δ = 10 %; P_L = 350 W.

Fig 6. Drain efficiency as a function of frequency; typical values



V_{DS} = 32 V; I_{Dq} = 200 mA; t_p = 300 μs; δ = 10 %;
P_L = 350 W.

Fig 7. Power gain as a function of frequency; typical values

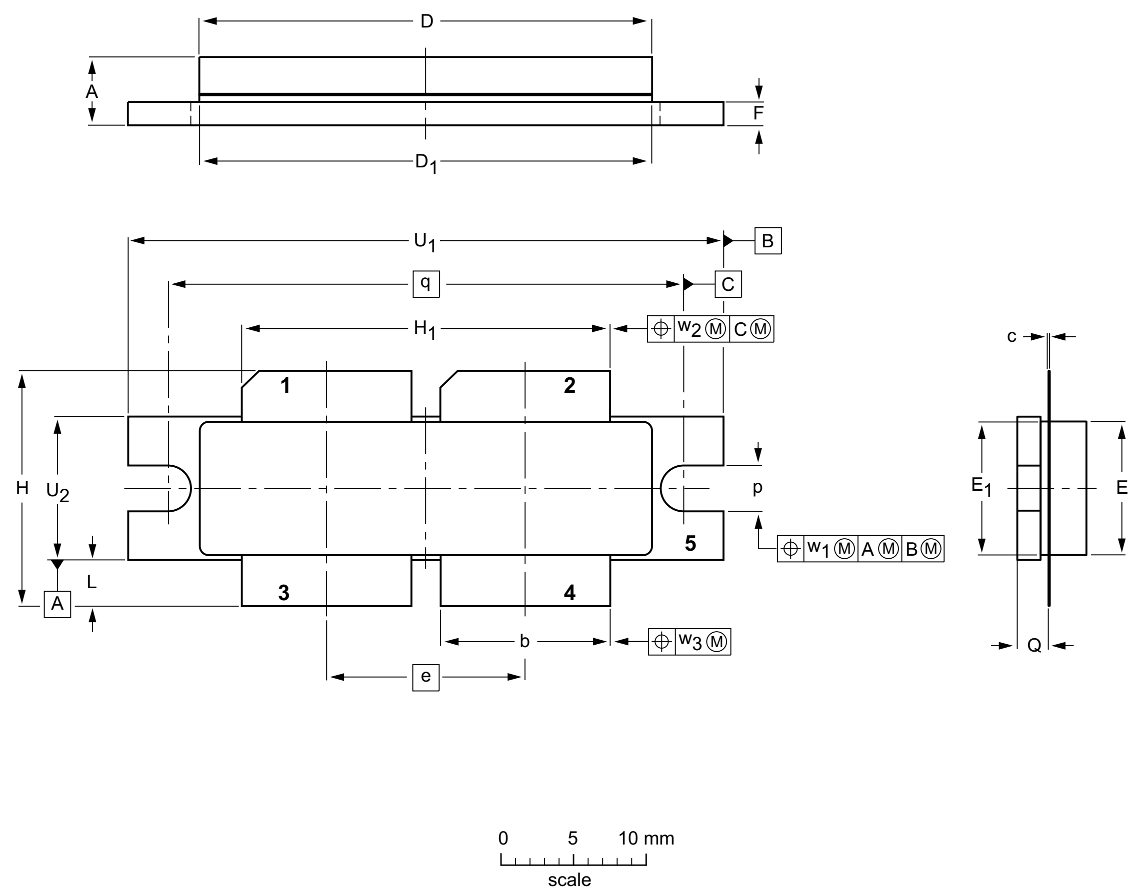


V_{DS} = 32 V; I_{Dq} = 200 mA; t_p = 300 μs; δ = 10 %;
P_L = 350 W.

Fig 8. Input return loss as a function of frequency; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

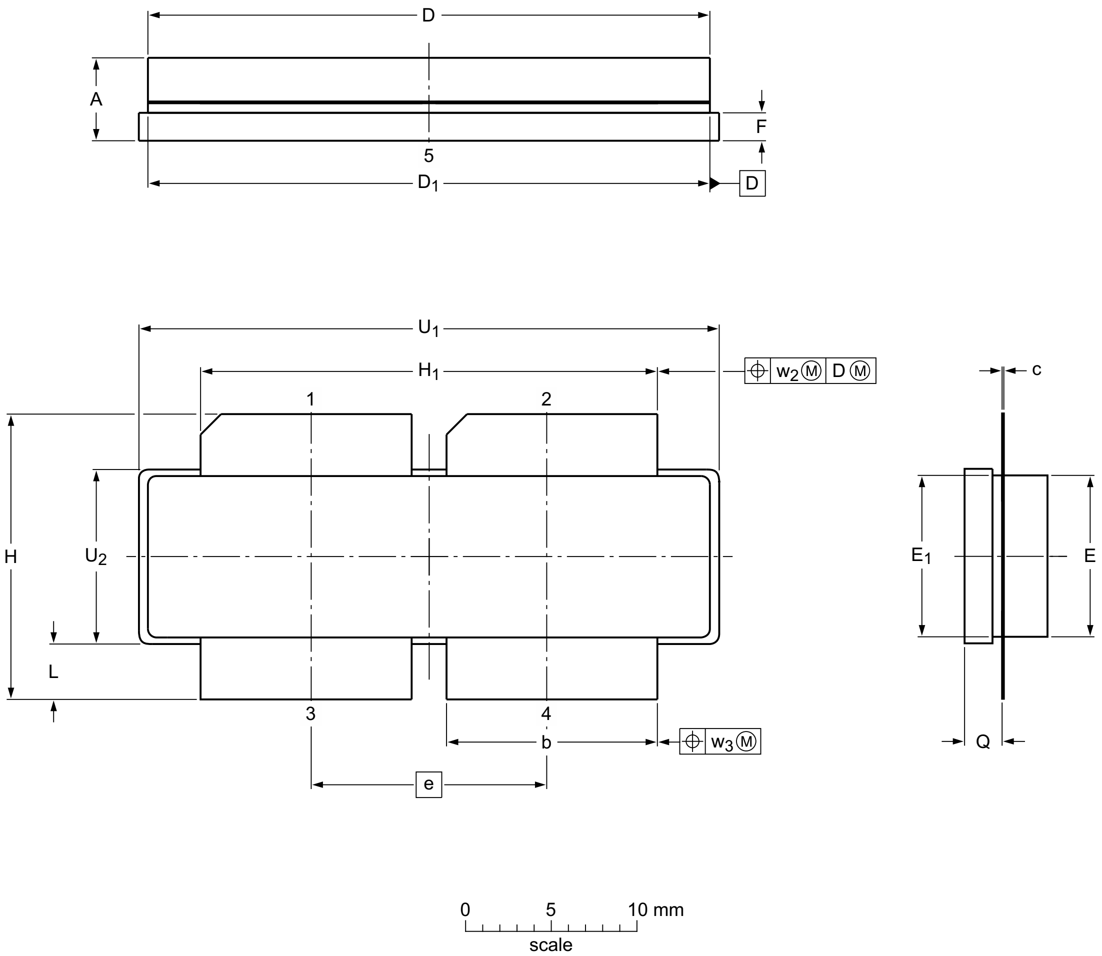
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 9. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 10. Package outline SOT539B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
S-band	Short wave Band
SMD	Surface-Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS7G2729L-350P_LS-350P v.5	20140516	Product data sheet	-	BLS7G2729L-350P_LS-350P v.4
Modifications:	• Figure 3 on page 6: figure has been corrected.			
BLS7G2729L-350P_LS-350P v.4	20130923	Product data sheet	-	BLS7G2729L-350P_LS-350P v.3
BLS7G2729L-350P_LS-350P v.3	20130712	Objective data sheet	-	BLS7G2729L-350P_LS-350P v.2
BLS7G2729L-350P_LS-350P v.2	20130506	Objective data sheet	-	BLS7G2729L-350P_LS-350P v.1
BLS7G2729L-350P_LS-350P v.1	20110524	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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