CS42516

110 dB, 192 kHz 6-Ch Codec with S/PDIF Receiver

Features

- Six 24-bit D/A, Two 24-bit A/D Converters
- 110 dB DAC / 114 dB ADC Dynamic Range
- -100 dB THD+N
- System Sampling Rates up to 192 kHz
- S/PDIF Receiver compatible with EIAJ CP1201 and IEC-60958
- 8:2 S/PDIF Input MUX
- Recovered S/PDIF CLK or OMCK System Clock selection
- ADC High Pass Filter for DC offset calibration
- Digital Output Volume Control with Soft ramp
- Digital +/-15dB Input Gain Adjust for ADC
- Differential Analog Architecture
- Supports logic levels between 5 V and 1.8 V

General Description

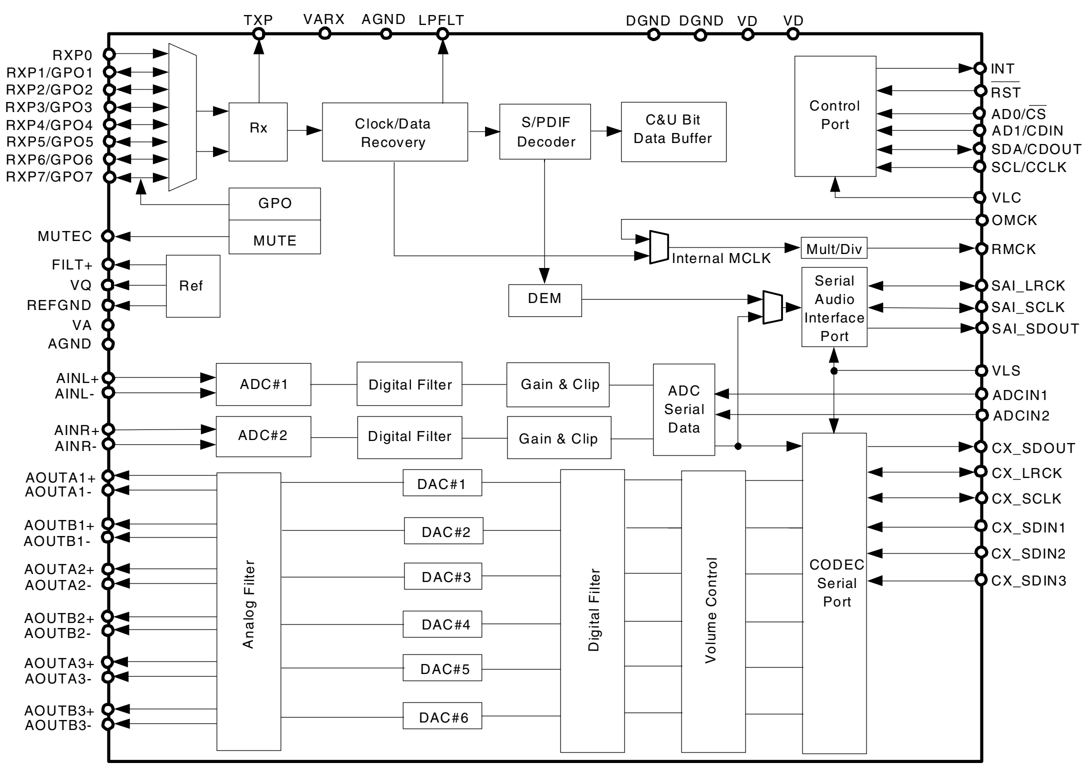
The CS42516 codec provides two analog-to-digital and six digital-to-analog delta-sigma converters, as well as an integrated S/PDIF receiver, in a 64-pin LQFP package.

The CS42516 integrated S/PDIF receiver supports up to eight inputs and clock recovery circuitry. The internal stereo ADC is capable of independent channel gain control for single-ended or differential analog inputs. All six channels of DAC provide digital volume control and differential analog outputs.

The CS42516 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, digital speaker and automotive audio systems.

ORDERING INFORMATION

CS42516-CQ	-10° to 70° C	64-pin LQFP
CS42516-IQ	-40° to 85° C	64-pin LQFP
CDB42518	Evaluation Board	



Advance Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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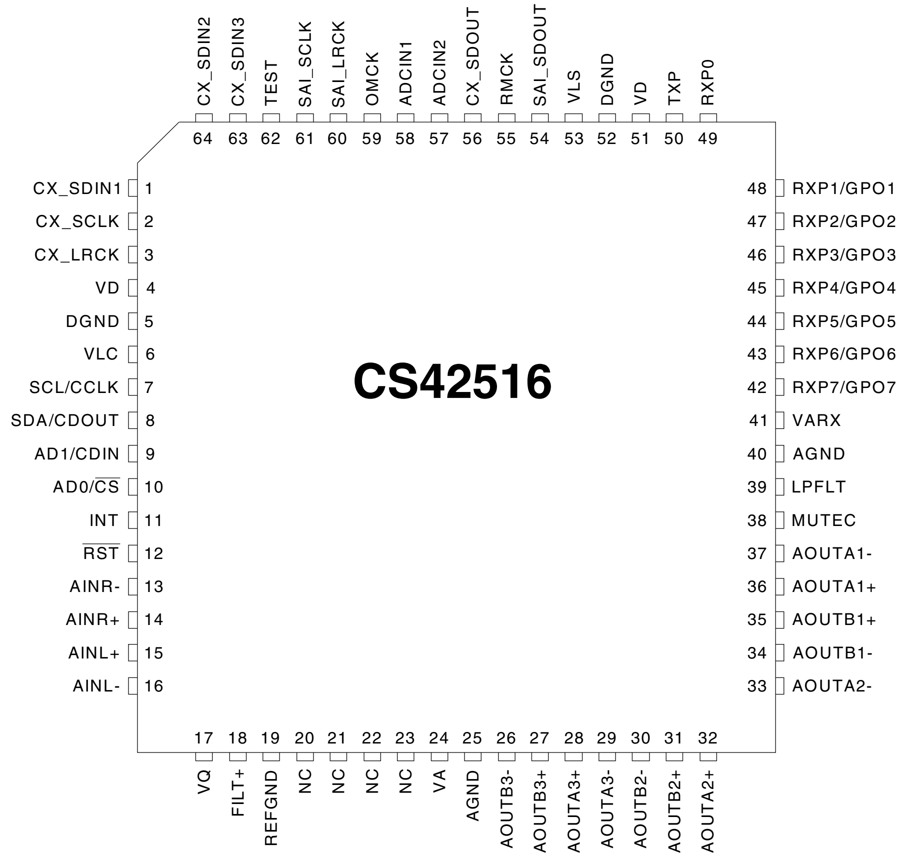
1 PIN DESCRIPTIONS



Pin Name	#	Pin Description
CX_SDIN1 **CX_SDIN2** **CX_SDIN3**	1 64 63	**Codec Serial Audio Data Input** (*Input*) - Input for two’s complement serial audio data.
CX_SCLK	2	**CODEC Serial Clock** *(Input/Output)* - Serial clock for the CODEC serial audio interface.
CX_LRCK	3	**CODEC Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the CODEC serial audio data line.
VD	4 51	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	5 52	**Digital Ground** (*Input*) - Ground reference. Should be connected to digital ground.
VLC	6	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port.
SCL/CCLK	7	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I^2C mode as shown in the Typical Connection Diagram.
SDA/CDOUT	8	**Serial Control Data** (*Input/Output*) **-** SDA is a data I/O line in I^2C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	9	**Address Bit 1 (I^2C)/Serial Control Data (SPI)** (*Input*) - AD1 is a chip address pin in I^2C mode; CDIN is the input data line for the control port interface in SPI mode.

AD0/$\overline{\text{CS}}$	10	**Address Bit 0 (I²C)/Control Port Chip Select (SPI)** *(Input)* **-** AD0 is a chip address pin in I²C mode; $\overline{\text{CS}}$ is the chip select signal in SPI mode.
INT	11	**Interrupt** *(Output)* **-** The CS42516 will generate an interrupt condition as per the Interrupt Mask register. See “Interrupts” on page 32 for more details.
$\overline{\text{RST}}$	12	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
AINR- **AINR+**	13 14	**Differential Right Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
AINL+ **AINL-**	15 16	**Differential Left Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins.
VQ	17	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
REFGND	19	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
NC	20 21 22 23	**No Connect Pins** - Do not make any connection to these pins.
AOUTA1 +,- **AOUTB1 +,-** **AOUTA2 +,-** **AOUTB2 +,-** **AOUTA3 +,-** **AOUTB3 +,-**	36,37 35,34 32,33 31,30 28,29 27,26	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VA **VARX**	24 41	**Analog Power** (*Input*) - Positive power supply for the analog section.
AGND	25 40	**Analog Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MUTEC	38	**Mute Control** (*Output*) - The Mute Control pin is tri-state following an initial power-on condition or whenever the PDN bit is set to a ‘1’, forcing the codec into power-down mode. The signal will remain in tri-state as long as the part is in power-down mode. The Mute Control pin goes to the selected “active” state during reset, muting, or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
LPFLT	39	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and ground.
RXP7/GPO7 **RXP6/GPO6** **RXP5/GPO5** **RXP4/GPO4** **RXP3/GPO3** **RXP2/GPO2** **RXP1/GPO1**	42 43 44 45 46 47 48	**S/PDIF Receiver Input/ General Purpose Output** (*Input/Output*) - Receiver inputs for S/PDIF encoded data. The CS42516 has an internal 8:2 multiplexer to select the active receiver port, according to the Receiver Mode Control 2 register. These pins can also be configured as general purpose output pins, or Mute Control outputs according to the RXP/General Purpose Pin Control registers.
RXP0	49	**S/PDIF Receiver Input** (*Input*) - Dedicated receiver input for S/PDIF encoded data.
TXP	50	**S/PDIF Transmitter Output** (*Output*) - S/PDIF encoded data output, mapped directly from one of the receiver inputs as indicated by the Receiver Mode Control 2 register.
VLS	53	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial port interfaces.

SAI_SDOUT	54	**Serial Audio Interface Serial Data Output** (*Output*) - Output for two's complement serial audio PCM data from the S/PDIF incoming stream. This pin can also be configured to transmit the output of the internal and external ADCs.
RMCK	55	**Recovered Master Clock** (*Output*) - Recovered master clock output from the PLL which is locked to the incoming S/PDIF stream.
CX_SDOUT	56	**CODEC Serial Data Output** (*Output*) - Output for two's complement serial audio data from the internal and external ADCs.
ADCIN1 **ADCIN2**	58 57	**External ADC Serial Input** (*Input*) - The CS42516 provides for up to two external stereo analog to digital converter inputs to provide a maximum of six channels on one serial data output line when the CS42516 is placed in One Line mode.
OMCK	59	**External Reference Clock** (*Input*) - External clock reference that must be 12.288MHz, 18.432MHz, or 24.576MHz.
SAI_LRCK	60	**Serial Audio Interface Left/Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SAI_SCLK	61	**Serial Audio Interface Serial Clock** *(Input/Output)* - Serial clock for the Serial Audio Interface.
TEST	62	**Test Pin** (*Input*) - This pin must be connected to DGND.

2 TYPICAL CONNECTION DIAGRAM

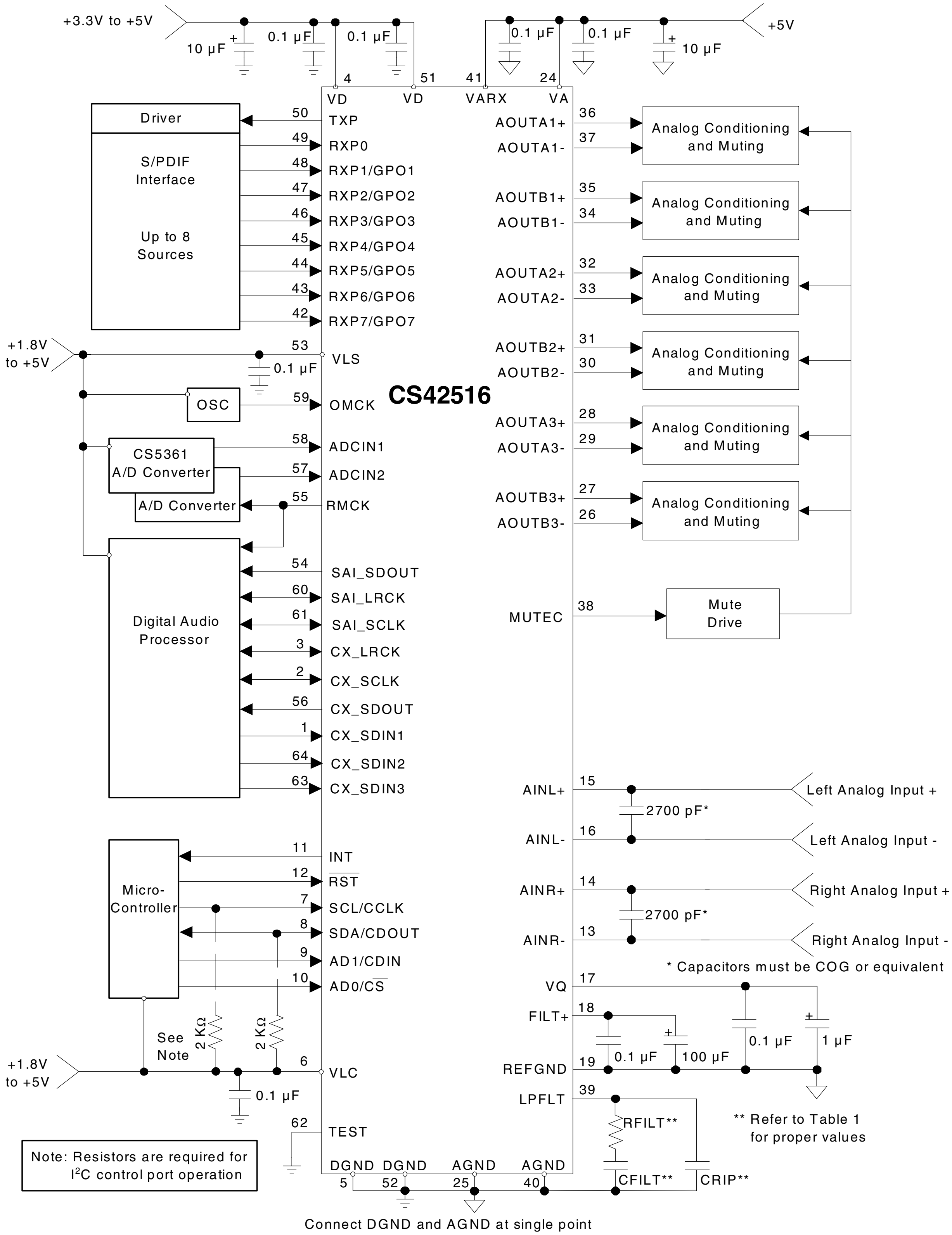


Figure 1. Typical Connection Diagram

3 APPLICATIONS

3.1 Overview

The CS42516 is a highly integrated mixed signal 24-bit audio codec comprised of 2 analog-to-digital converters (ADC), implemented using multi-bit delta-sigma techniques, 8 digital-to-analog converters (DAC) and a 192kHz digital audio S/PDIF receiver. Other functions integrated within the codec include independent digital volume controls for each DAC, digital e-emphasis filters for DAC and S/PDIF, digital gain control for ADC channels, ADC high-pass filters, an on-chip voltage reference, and an 8:2 mux for S/PDIF sources. All serial data is transmitted through two configurable serial audio interfaces with standard serial interface support as well as enhanced one line modes of operation allowing up to 6 channels of serial audio data on one data line. All functions are configured through a serial control port operable in SPI mode or in I^2C mode. Figure 1 shows the recommended connections for the CS42516.

The CS42516 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the FM bits in register "Functional Mode (address 03h)" on page 38. Single-Speed mode (SSM) supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed mode (DSM) supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed mode (QSM) supports input sample rates up to 192 kHz and uses an oversampling ratio of 32x.

Using the receiver clock recovery PLL, a low jitter clock is recovered from the incoming S/PDIF data stream. The recovered clock or an externally supplied clock attached to the OMCK pin can be used as the System Clock.

3.2 Analog Inputs

3.2.1 Line Level Inputs

AINR+, AINR-, AINL+, and AINL- are the line level differential analog inputs. These pins are internally biased to the DC quiescent reference voltage, VQ, of approximately 2.5V. The level of the signal can be adjusted for the left and right ADC independently through the ADC Left and Right Channel Gain Control Registers on page 49. The ADC output data is in 2's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively and cause the ADC Overflow bit in the register "Interrupt Status (address 20h) (Read Only)" on page 52 to be set to a '1'.

The analog modulator samples the input at 6.144 MHz (internal MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are ($n \times 6.144$ MHz) the digital passband frequency, where n=0,1,2,...Refer to the Typical Connection Diagram which shows the suggested filter that will attenuate any noise energy at 6.144 MHz. See the CDB42518 evaluation board for additional input filter applications. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. If active circuitry precedes the ADC inputs, it is recommended that a low source impedance RC filter be placed between the active circuitry and the AINR+/- and AINL+/- pins.

3.2.2 High Pass Filter and DC Offset Calibration

The CS42516 includes a digital high pass filter after the decimator to remove the indeterminate DC offsets introduced by the analog buffer stage and the analog modulator. The high pass filter helps prevent audible “clicks” when switching between audio sources downstream from the ADCs. The high pass filter response, given in “A/D Digital Filter Characteristics” on page 62, scales linearly with sample rate. When enabled, any DC present at the analog inputs will be represented in the ADC outputs and the high pass filter will continuously subtract a measure of the DC offset from the output of the decimation filter. The high pass filters are controlled using the HPF_FREEZE bit in the register “Misc Control (address 05h)” on page 41.

3.3 Analog Outputs

3.3.1 Line Level Outputs and Filtering

The CS42516 contains on-chip buffer amplifiers capable of producing line level differential outputs. These amplifiers are biased to a quiescent DC level of approximately VQ.

The delta-sigma conversion process produces high frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low pass filter. The application note “Design Notes for a 2-Pole Filter with Differential Input” discusses the second-order Butterworth filter and differential to single-ended converter which was implemented on the CS42516 evaluation board, the CDB42518. The CS42516 does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

3.3.2 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS42516 incorporates selectable interpolation filters for each mode of operation. A “fast” and a “slow” roll-off filter is available in each of Single, Double, and Quad Speed modes. These filters have been designed to accommodate a variety of musical tastes and styles. The FILT_SEL bit found in the register “Misc Control (address 05h)” on page 41 is used to select which filter is used. Filter response plots can be found in Figures 38 to 61.

3.3.3 Digital Volume and Mute Control

Each DAC’s output level is controlled via the Volume Control registers operating over the range of 0 to -127 dB attenuation with 0.5 dB resolution. See “Volume Control (addresses 0Fh, 10h, 11h, 12h, 13h, 14h)” on page 47. Volume control changes are programmable to ramp in increments of 0.125 dB at a variable rate controlled by the SZCX1:0 bits in the Digital Volume Control register. See “Volume Control (address 0Dh)” on page 45.

Each output can be independently muted via mute control bits in the register “Channel Mute (address 0Eh)” on page 47. When enabled, each XX_MUTE bit attenuates the corresponding DAC to its maximum value (-127 dB). When the XX_MUTE bit is disabled, the corresponding DAC returns to the attenuation level set in the Volume Control register. The attenuation is ramped up and down at the rate specified by the SZCX1:0 bits.

The Mute Control pin, MUTEC, is typically connected to an external mute control circuit. The Mute Control pin is tri-stated during power up or in power down mode by setting the PDN bit in the register “Power

Control (address 02h)" on page 38 to a '1'. Once out of power-down mode the pin can be controlled by the user via the control port, or automatically asserted high when zero data is present on all eight DAC inputs, or when serial port clock errors are present. To prevent large transients on the output, it is desirable to mute the DAC outputs before the Mute Control pin is asserted. Please see the MUTEC pin in the Pin Descriptions section for more information.

Each of the RXP1/GPO1-RXP7/GPO7 can be programed to provide a hardware MUTE signal to individual circuits. When not used as an S/PDIF input, each pin can be programed as an output, with specific muting capabilities as defined by the function bits in the register "RXP/General Purpose Pin Control (addresses 29h to 2Fh)" on page 57.

The CS42516 implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 14 on page 49 and Figure 2 for additional information.

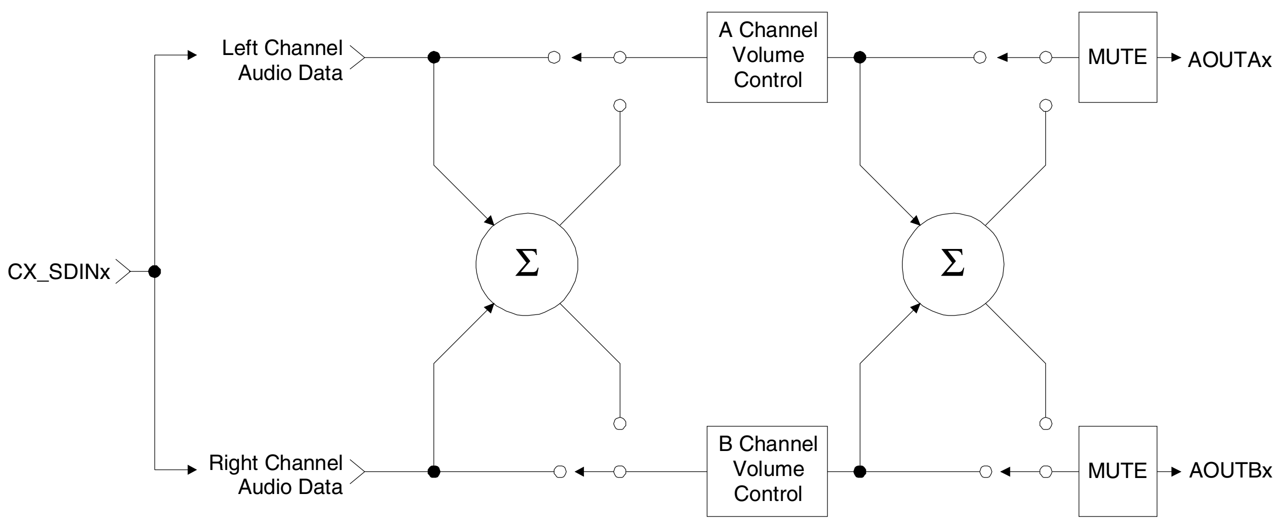


Figure 2. ATAPI Block Diagram (x = channel pair 1, 2, or 3)

3.4 S/PDIF Receiver

The CS42516 includes an S/PDIF digital audio receiver. The S/PDIF receiver accepts and decodes digital audio data according to the IEC60958 (S/PDIF), and EIAJ CP-1201 interface standards. The receiver consists of an 8:2 multiplexer input stage, driven through pins RXP0 and RXP1/GPO1 - RXP7/GPO7, a PLL based clock recovery circuit, and a decoder which separates the audio data from the channel status and user data. A comprehensive buffering scheme provides read access to the channel status and user data.

External components are used to terminate and isolate the incoming data cables from the CS42516. These components and required circuitry are detailed in the reference design for the CS42516, the CDB42518.

3.4.1 8:2 S/PDIF Input Multiplexer

The CS42516 contains an 8:2 S/PDIF Input Multiplexer to accommodate up to eight channels of input digital audio data. Digital audio data is single-ended and input through the RXP0 and RXP1/GPO1-RXP7/GPO7 pins. Any one of these inputs can be multiplexed to the input of the S/PDIF receiver and to the S/PDIF output pin TXP.

When any portion of the multiplexer is implemented, unused RXP0 and RXPx/GPOx pins should be tied to a 0.01uF capacitor to ground. The receiver multiplexer select line control is accessed through bits RMUX2:0 in the Receiver Mode Control 2 register on page 51. The TXP multiplexer select line control is accessed through bits TMUX2:0 in the same register. The multiplexer defaults to RXP0 for both functions.

3.4.2 Error Reporting and Hold Function

While decoding the incoming S/PDIF data stream, the CS42516 can identify several kinds of error, indicated in the register “Receiver Errors (address 26h) (Read Only)” on page 55. The UNLOCK bit indicates whether the PLL is locked to the incoming S/PDIF data. The V bit reflects the current validity bit status. The CONF (confidence) bit indicates the amplitude of the eye pattern opening, indicating a link that is close to generating errors. The BIP (bi-phase) error bit indicates an error in incoming bi-phase coding. The PAR (parity) bit indicates a received parity error.

The error bits are "sticky": they are set on the first occurrence of the associated error and will remain set until the user reads the register through the control port. This enables the register to log all unmasked errors that occurred since the last time the register was read.

The Receiver Errors Mask register (see “Receiver Errors Mask (address 27h)” on page 56) allows masking of individual errors. The bits in this register serve as masks for the corresponding bits of the Receiver Error Register. If a mask bit is set to 1, the error is unmasked, which implies the following: its occurrence will be reported in the receiver error register, invoke the occurrence of a RERR interrupt, and affect the current audio sample according to the status of the HOLD bits. The HOLD bits allow a choice of holding the previous sample, replacing the current sample with zero (mute), or not changing the current audio sample. If a mask bit is set to 0, the error is masked, which implies the following: its occurrence will not be reported in the receiver error register, the RERR interrupt will not be generated, and the current audio sample will not be affected. The QCRC and CCRC errors do not affect the current audio sample, even if unmasked.

3.4.3 Channel Status Data Handling

The first 2 bytes of the Channel Status block (C data) are decoded into the Receiver Channel Status register (see “Receiver Channel Status (address 25h) (Read Only)” on page 54). The setting of the CHS bit in the register “Channel Status Data Buffer Control (address 24h)” on page 53 determines whether the channel status decodes are from the A channel (CHS = 0) or B channel (CHS = 1).

The PRO (professional) bit is extracted directly. For consumer data, the COPY (copyright) bit is extracted, and the category code and L bits are decoded to determine SCMS status, indicated by the ORIG (original) bit. If the category code is set to General on the incoming S/PDIF stream, copyright will always be indicated even when the stream indicates no copyright. Finally, the $\overline{\text{AUDIO}}$ bit is extracted and used to set an $\overline{\text{AUDIO}}$ indicator, as described in the Non-Audio Auto-Detection section below.

If 50/15 µs pre-emphasis is detected, and the Receiver Auto De-emphasis control is enabled, then de-emphasis will automatically be applied to the incoming digital PCM data. See “Functional Mode (address 03h)” on page 38 for more details.

The encoded channel status bits which indicate sample word length are decoded according to IEC 60958. Audio data routed to the Serial Audio Interface port is unaffected by the word length settings; all 24 bits are passed on as received.

The CS42516 also contains sufficient RAM to store a full block of C data for both A and B channels (192 x 2 = 384 bits), and also 384 bits of User (U data) information. The user may read from these buffer RAMs through the control port.

The buffering scheme involves 2 block-sized buffers, named D and E, as shown in Figure 3. The MSB of each byte represents the first bit in the serial C data stream. For example, the MSB of byte 0 (which is at control port address 4Ah) is the consumer/professional bit for channel status block A.

The first buffer (D) accepts incoming C data from the S/PDIF receiver. The 2nd buffer (E) accepts entire blocks of data from the D buffer. The E buffer is also accessible from the control port, allowing reading of the C data.

3.4.3.1 Channel Status Data E Buffer Access

The user can monitor the incoming Channel Status data by reading the E buffer, which is mapped into the register space of the CS42516, through the control port Data Buffer. The Data Buffer must first be configured to point to the address space of the C data. This is accomplished be setting the BSEL bit to ‘0’ in the register “Channel Status Data Buffer Control (address 24h)” on page 53.

The user can configure the Interrupt Mask Register to cause an interrupt whenever any data bit changes are detected when D to E Channel Status buffer transfers occur. If no data bits have changed within the current transfer of data from D to E, then no interrupt will be generated. This allows determination of the acceptable time periods to interact with the E buffer. See “Interrupt Mask (address 21h)” on page 53 for more details.

The E buffer is organized as 24 x 16-bit words. For each word the MS Byte is the A channel data, and the LS Byte is the B channel data (see Figure 3). There are two methods of accessing this memory, known as

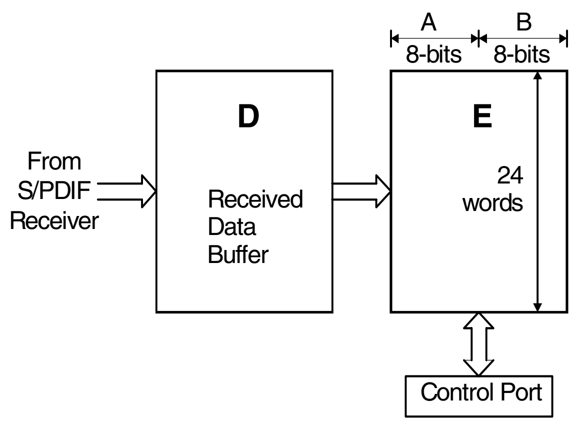


Figure 3. Channel Status Data Buffer Structure

one byte mode and two byte mode. The desired mode is selected by setting the CAM bit in the Channel Status Data Buffer Control Register.

One Byte mode

In many applications, the channel status blocks for the A and B channels will be identical. In this situation, if the user reads a byte from one of the channel's blocks, the corresponding byte for the other channel will be the same. One byte mode takes advantage of the often identical nature of A and B channel status data. When reading data in one byte mode, a single byte is returned, which can be from channel A or B data, depending on a register control bit.

One byte mode saves the user substantial control port access time, as it effectively accesses 2 bytes worth of information in 1 byte's worth of access time. If the control port's autoincrement addressing is used in combination with this mode, multi-byte accesses such as full-block reads can be done especially efficiently.

Two Byte mode

There are those applications in which the A and B channel status blocks will not be the same, and the user is interested in accessing both blocks. In these situations, two byte mode should be used to access the E buffer.

In this mode, a read will cause the CS42516 to output two bytes from its control port. The first byte out will represent the A channel status data, and the 2nd byte will represent the B channel status data.

3.4.3.2 Serial Copy Management System (SCMS)

The CS42516 allows read access to all the channel status bits. For consumer mode SCMS compliance, the host microcontroller needs to read and interpret the Category Code, Copy bit and L bit appropriately.

3.4.4 User Data Handling

The incoming User (U) data is buffered in a user accessible buffer. If the U data bits have been encoded as Q-channel subcode, the data is decoded and presented in 10 consecutive register locations, address 30h to 39h. The user can configure the Interrupt Mask Register to cause interrupts to indicate the decoding of a new Q-channel block, which may be read through the control port.

3.4.4.1 User (U) Data E Buffer Access

Entire blocks of U data are buffered using a cascade of 2 block-sized RAMs to perform the buffering as describe in the Channel Status section. The user has access to the E buffer through the control port Data Buffer which is mapped into the register space of the CS42516. The Data Buffer must first be configured to point to the address space of the U data. This is accomplished be setting the BSEL bit to ‘1’ in the register “Channel Status Data Buffer Control (address 24h)” on page 53.

The user can configure the Interrupt Mask Register to cause an interrupt whenever any data bit changes are detected when D to E Channel Status buffer transfers occur. If no data bits have changed within the current transfer of data from D to E, then no interrupt will be generated. This allows determination of the acceptable time periods to interact with the E buffer. See “Interrupt Mask (address 21h)” on page 53 for more details.

The U buffer access only operates in two byte mode, since there is no concept of A and B blocks for user data. The arrangement of the data is as followings: Bit15[A7]Bit14[B7]Bit13[A6]Bit12[B6]......Bit1[A0]Bit0[B0]. The arrangement of the data in each byte is MSB is the first received bit and is the first transmitted bit. The first byte read is the first byte received, and the first byte sent is the first byte transmitted. When two bytes are read from the E buffer, the bits are presented in the following arrangement: A[7]B[7]A[6]B[6]....A[0]B[0].

3.4.5 Non-Audio Auto-Detection

An S/PDIF data stream may be used to convey non-audio data, thus it is important to know whether the incoming data stream is digital PCM audio samples or not. This information is typically conveyed in channel status bit 1 ($\overline{\text{AUDIO}}$), which is extracted automatically by the CS42516. However, certain non-audio sources, such as AC-3® or MPEG encoders, may not adhere to this convention, and the bit may not be properly set.

The CS42516 S/PDIF receiver can detect such non-audio data. This is accomplished by looking for a 96-bit sync code, consisting of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872, and 0x4E1F. When the sync code is detected, an internal AUTODETECT signal will be asserted. If no additional sync codes are detected within the next 4096 frames, AUTODETECT will be de-asserted until another sync code is detected. The $\overline{\text{AUDIO}}$ bit in the Receiver Channel Status register is the logical OR of AUTODETECT and the received channel status bit 1. If non-audio data is detected, the data will be processed exactly as if it were normal audio. It is up to the user to mute the outputs as required.

3.5 Clock Generation

The clock generation for the CS42516 is shown in the figure below. The internal MCLK is derived from the output of the PLL or a master clock source attached to OMCK. The mux selection is controlled by the SW_CTRLx bits and can be configured to manual switch mode only, or automatically switch on lost of PLL lock to the other source input.

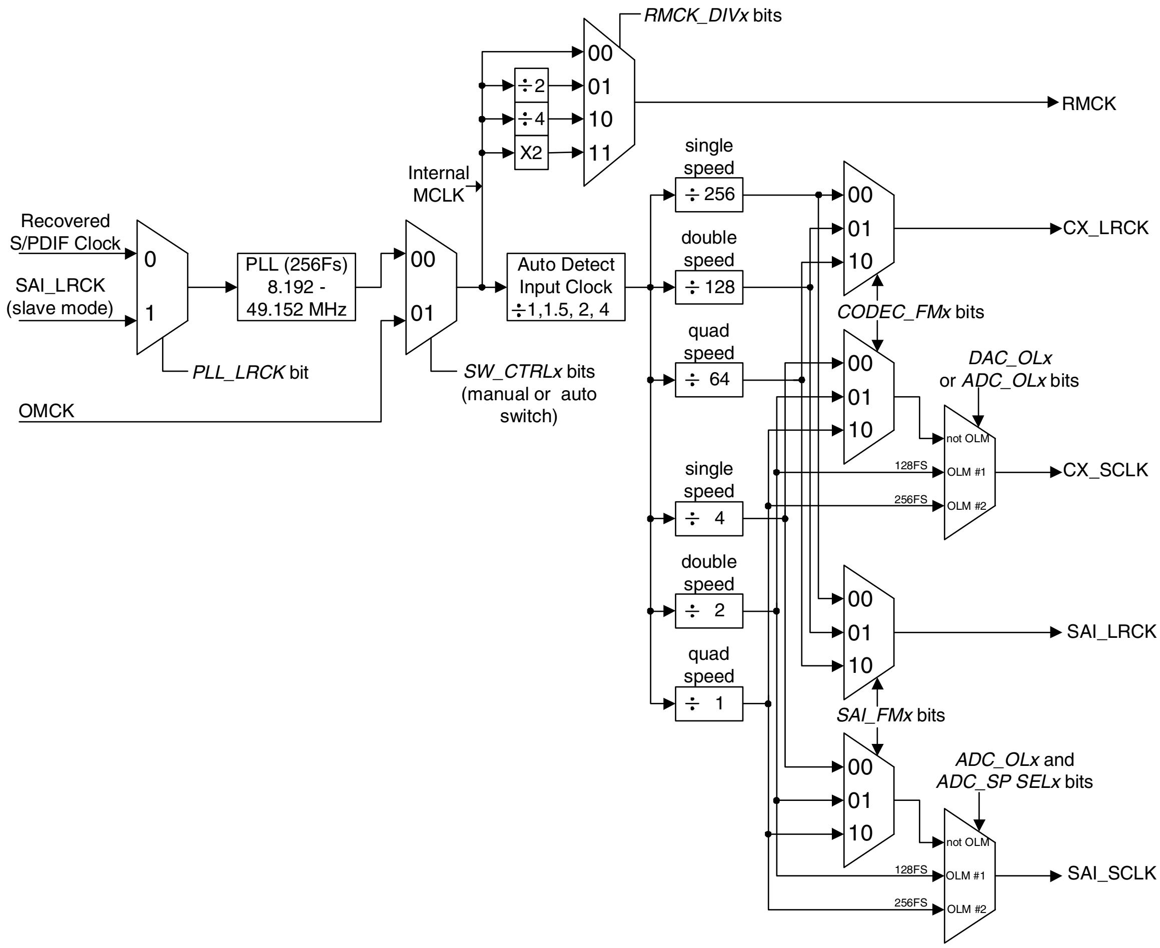


Figure 4. CS42516 Clock Generation

3.5.1 PLL and Jitter Attenuation

An on-chip Phase Locked Loop (PLL) is used to recover the clock from the incoming S/PDIF data stream. There are some applications where low jitter in the recovered clock, presented on the RMCK pin, is important. For this reason, the PLL has been designed to have good jitter attenuation characteristics as shown in Figures 5. In addition, the PLL has been designed to only use the preambles of the S/PDIF stream to provide lock update information to the PLL. This results in the PLL being immune to data dependent jitter affects because the S/PDIF preambles do not vary with the data.

The PLL has the ability to lock onto a wide range of input sample rates with no external component changes. The nominal center sample rate is the sample rate that the PLL first locks onto upon application of an S/PDIF data stream.

The PLL can be configured to lock onto the incoming SAI_LRCK signal from the Serial Audio Interface Port and generate the required internal master clock frequency. By setting the PLL_LRCK bit to a ‘1’ in the register “Clock Control (address 06h)” on page 43, the PLL will lock to the incoming SAI_LRCK and generate an output clock of 256Fs. Table 2 below shows the output of the PLL with typical input Fs values for SAI_LRCK.

The PLL behavior is affected by the external filter component values. The “Typical Connection Diagram” on page 9 shows the recommended configuration of the two capacitors and one resistor required. The set of component values recommended for 32kHz to 192kHz sample rate applications are shown in Table 1. The lock time is the worst case for an Fs transition from un-locked state to locking to 192kHz.

Fs Range (kHz)	RFILT (kΩ)	CFILT (pF)	CRIP (pF)	Settling time
32 to 192	1.6	8200	220	11ms

Table 1. PLL External Component Values

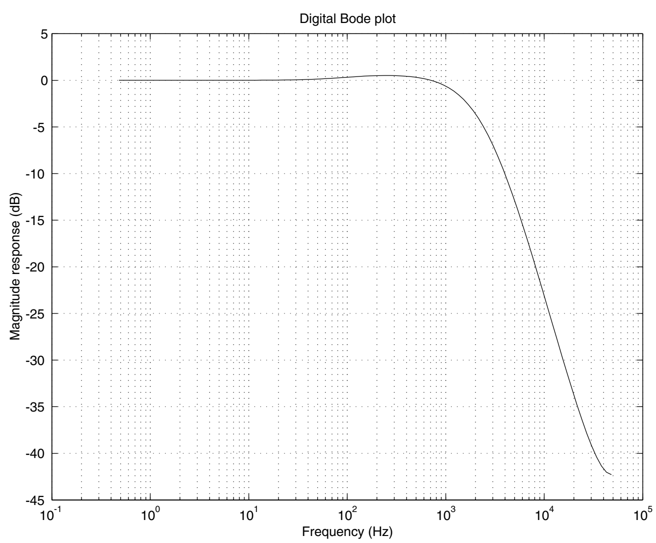


Figure 5. Jitter Attenuation Characteristics of PLL

It is important to treat the LPFLT pin as a low level analog input. It is suggested that the ground end of the PLL filter be returned directly to the AGND pin independently of the digital ground plane.

3.5.2 OMCK System Clock Mode

A special clock switching mode is available that allows the clock that is input through the OMCK pin to be used as the internal master clock. This feature is controlled by the SW_CTRLx bits in register “Clock Control (address 06h)” on page 43. An advanced auto switching mode is also implemented to maintain master clock functionality. The clock auto switching mode allows the clock input through OMCK to be used as a clock in the system without any disruption when the PLL loses lock, for example, when the input is removed from the receiver. This clock switching is done glitch free.

3.5.3 Master Mode

In master mode, the serial interface timings are derived from an external clock attached to OMCK or the output of the PLL with an input reference to either the S/PDIF Receiver recovered clock or the SAI_LRCK input from the Serial Audio Interface Port. Master clock selection and operation is configured with the SW_CTRL1:0 and CLK_SEL bits in the Clock Control Register (See "Clock Control (address 06h)" on page 43).

The supported PLL output frequencies are shown in Table 2 below. The sample rate to OMCK ratios and OMCK frequency requirements for Master mode operation are shown in Table 3.

Sample Rate (kHz)	PLL Output (MHz)		
	Single Speed (4 to 50kHz)	Double Speed (50 to 100kHz)	Quad Speed (100 to 192kHz)
	256x	256x	256x
32	8.1920	-	-
44.1	11.2896	-	-
48	12.2880	-	-
64	-	16.3840	-
88.2	-	22.5792	-
96	-	24.5760	-
176.4	-	-	45.1584
192	-	-	49.1520

Table 2. Common PLL Output Clock Frequencies

Sample Rate (kHz)	OMCK (MHz)								
	Single Speed (4 to 50kHz)			Double Speed (50 to 100kHz)			Quad Speed (100 to 192kHz)		
	256x	384x	512x	128x	192x	256x	64x	96x	128x
48	12.2880	18.4320	24.5760	-	-	-	-	-	-
96	-	-	-	12.2880	18.4320	24.5760	-	-	-
192	-	-	-	-	-	-	12.2880	18.4320	24.5760

Table 3. Common OMCK Clock Frequencies

3.5.4 Slave Mode

In Slave mode, CX_LRCK, CX_SCLK and/or SAI_LRCK, SAI_SCLK operate as inputs. The signal Left/Right clock must be equal to the sample rate, Fs and must be synchronously derived from the supplied master clock, OMCK or the output of the PLL. The serial bit clock, CX_SCLK and/or SAI_SCLK, must be synchronously derived from the master clock and be equal to 128x, 64x, 48x or 32x Fs depending on the interface format selected and desired speed mode. One Line Mode #1 is supported in Slave Mode. One Line Mode #2 is not supported. Refer to Table 4 for required clock ratios.

	Single Speed	Double Speed	Quad Speed	One Line Mode #1
OMCK/LRCK Ratio	256x, 512x	128x, 256x	128x	256x
SCLK/LRCK Ratio	32x, 48x, 64x, 128x	32x, 64x	32x, 64x	128x

Table 4. Slave Mode Clock Ratios

3.6 Digital Interfaces

3.6.1 Serial Audio Interface Signals

The CS42516 interfaces to an external Digital Audio Processor via two independent serial ports, the CODEC serial port, CODEC_SP and the Serial Audio Interface serial port, SAI_SP. The digital output of the internal ADCs can be configured to use either the CX_SDOUT pin or the SAI_SDOUT pin and the corresponding serial port clocking signals. These configuration bits and the selection of Single, Double or Quad -Speed mode for CODEC_SP and SAI_SP are found in register "Functional Mode (address 03h)" on page 38.

The serial interface clocks, SAI_SCLK for SAI_SP and CX_SCLK for CODEC_SP, are used for both transmitting and receiving audio data. Either SAI_SCLK or CX_SCLK can be generated by the CS42516 (master mode) or it can be input from an external source (slave mode). Master or Slave mode selection is made using bits CODEC_SP $M/\overline{S}$ and SAI_SP $M/\overline{S}$ in register "Misc Control (address 05h)" on page 41.

The Left/Right clock (SAI_LRCK or CX_LRCK) is used to indicate left and right data frames and the start of a new sample period. It may be an output of the CS42516 (master mode), or it may be generated by an external source (slave mode). As described in later sections, particular modes of operation do allow the sample rate, Fs, of the SAI_SP and the CODEC_SP to be different, but must be multiples of each other.

The serial data interface format selection (left/right justified, I^2S or one line mode) for the Serial Audio Interface serial port data out pin, SAI_SDOUT, the CODEC serial port data out pin, CX_SDOUT, and the CODEC input pins, CX_SDIN1:3, is configured using the appropriate bits in the register "Interface Formats (address 04h)" on page 40. The serial audio data is presented in 2's complement binary form with the MSB first in all formats.

CX_SDIN1, CX_SDIN2, and CX_SDIN3 are the serial data input pins supplying the associated internal DAC. CX_SDOUT, the ADC data output pin, carries data from the two internal 24-bit ADCs and, when configured for one-line mode, up to four additional ADC channels attached externally to the signals ADCIN1 and ADCIN2 (typically two CS5361 stereo ADCs). When operated in One Line Data Mode, 6 channels of DAC data are input on CX_SDIN1 and 6 channels of ADC data are output on CX_SDOUT. Table 5 outlines the serial port channel allocations

.

Serial Inputs / Outputs		
CX_SDIN1	left channel	DAC #1
	right channel	DAC #2
	one line mode	DAC channels 1,2,3,4,5,6
CX_SDIN2	left channel	DAC #3
	right channel	DAC #4
	one line mode	not used
CX_SDIN3	left channel	DAC #5
	right channel	DAC #6
	one line mode	not used

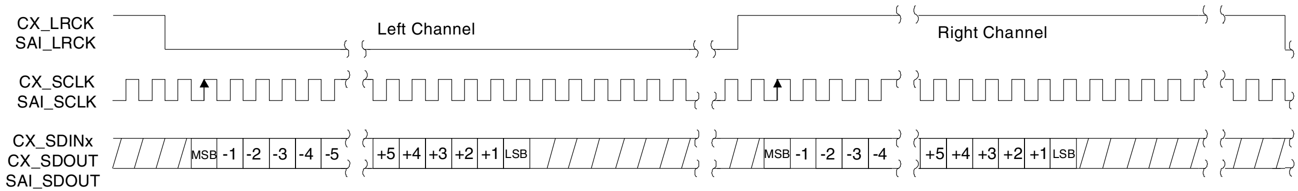
Table 5. Serial Audio Port Channel Allocations

Serial Inputs / Outputs		
CX_SDOUT	left channel right channel one line mode	ADC #1 ADC #2 ADC channels 1,2,3,4,5,6
SAI_SDOUT	left channel right channel one line mode	S/PDIF Left or ADC #1 S/PDIF Right or ADC #2 ADC channels 1,2,3,4,5,6
ADCIN1	left channel right channel	External ADC #3 External ADC #4
ADCIN2	left channel right channel	External ADC #5 External ADC #6

Table 5. Serial Audio Port Channel Allocations

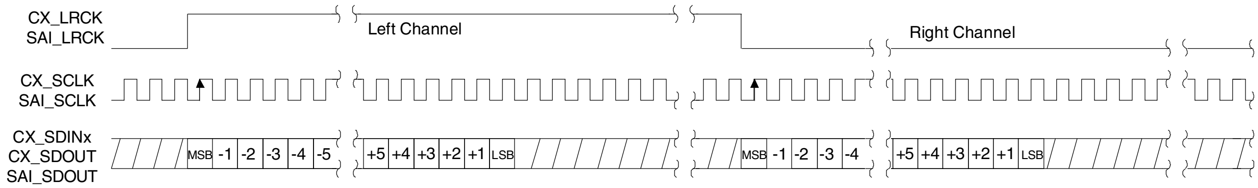
3.6.2 Serial Audio Interface Formats

The CODEC_SP and SAI_SP digital audio serial ports support 5 formats with varying bit depths from 16 to 24 as shown in Figure 6, Figure 7, Figure 8, Figure 9 and Figure 10. These formats are selected using the configuration bits in these registers, “Functional Mode (address 03h)” on page 38 and “Interface Formats (address 04h)” on page 40. For the diagrams below, single-speed mode is equivalent to Fs = 32, 44.1, 48kHz; double-speed mode is for Fs = 64, 88.2, 96kHz; and quad-speed mode is for Fs = 176.4, 196kHz.



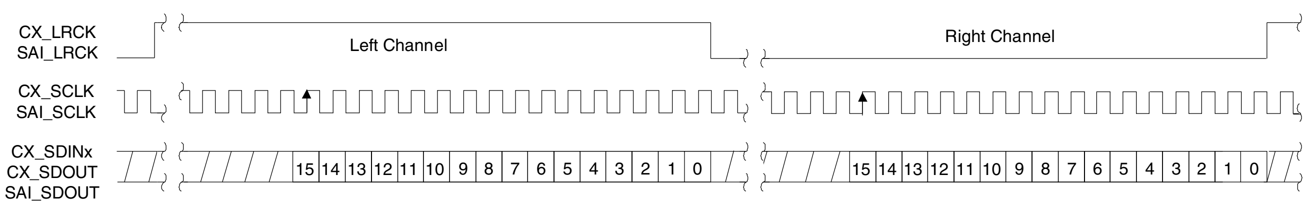
I2S Mode, Data Valid on Rising Edge of SCLK			
Bits/Sample	SCLK Rate(s)		Notes
	Master	Slave	
16	64, 128 Fs	48, 64, 128 Fs	single-speed mode
	64 Fs	64 Fs	double-speed mode
	64 Fs	64 Fs	quad-speed mode
18 to 24	64, 128, 256 Fs	48, 64, 128 Fs	single-speed mode
	64 Fs	64 Fs	double-speed mode
	64 Fs	64 Fs	quad-speed mode

Figure 6. I²S Serial Audio Formats



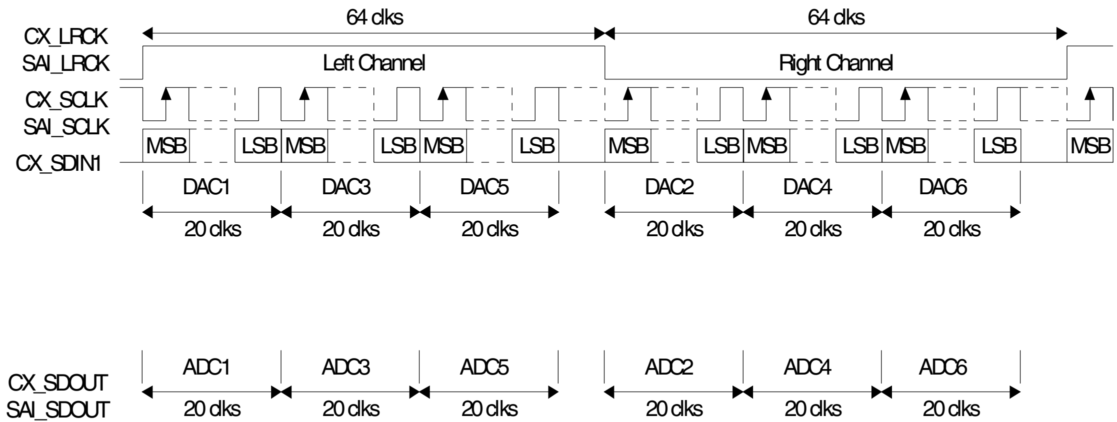
Left Justified Mode, Data Valid on Rising Edge of SCLK			
Bits/Sample	SCLK Rate(s)		Notes
	Master	Slave	
16	64, 128 Fs	32, 48, 64, 128 Fs	single-speed mode
	64 Fs	32, 64 Fs	double-speed mode
	64 Fs	32, 64 Fs	quad-speed mode
18 to 24	64, 128, 256 Fs	48, 64, 128 Fs	single-speed mode
	64 Fs	64 Fs	double-speed mode
	64 Fs	64 Fs	quad-speed mode

Figure 7. Left Justified Serial Audio Formats



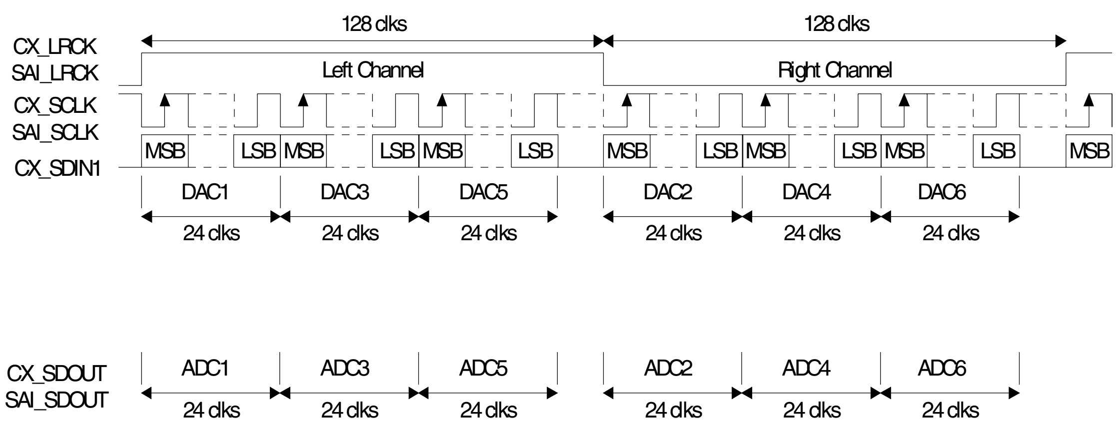
Right Justified Mode, Data Valid on Rising Edge of SCLK			
Bits/Sample	SCLK Rate(s)		Notes
	Master	Slave	
16	64, 128 Fs	32, 48, 64, 128 Fs	single-speed mode
	64 Fs	32, 64 Fs	double-speed mode
	64 Fs	32, 64 Fs	quad-speed mode
24	64, 128, 256 Fs	48, 64, 128 Fs	single-speed mode
	64 Fs	64 Fs	double-speed mode
	64 Fs	64 Fs	quad-speed mode

Figure 8. Right Justified Serial Audio Formats



One Line Data Mode #1, Data Valid on Rising Edge of SCLK			
Bits/Sample	SCLK Rate(s)		Notes
	Master	Slave	
20	128 Fs	128 Fs	single-speed mode
	128 Fs	128Fs	double-speed mode

Figure 9. One Line Mode #1 Serial Audio Format

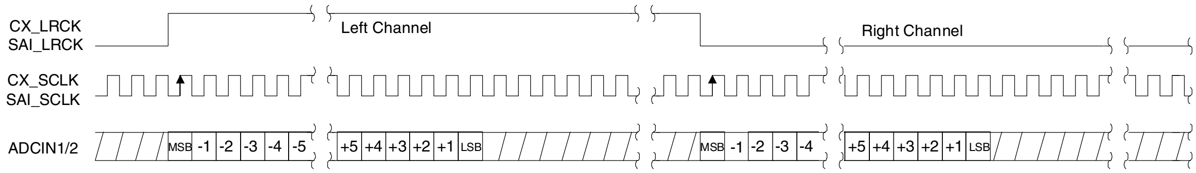


One Line Data Mode #2, Data Valid on Rising Edge of SCLK			
Bits/Sample	SCLK Rate(s)		Notes
	Master	Slave	
24	256 Fs	not supported	single-speed mode

Figure 10. One Line Mode #2 Serial Audio Format

3.6.3 ADCIN1/ADCIN2 Serial Data Format

The two serial data lines which interface to the optional external ADCs, ADCIN1 and ADCIN2, support only left-justified, 24-bit samples at 64Fs or 128Fs. This interface is not effected by any of the serial port configuration register bit settings. These serial data lines are used when supporting One Line Mode of operation with external ADCs attached. If these signals are not being used, they should be wired to GND via a pull-down resistor.



Left Justified Mode, Data Valid on Rising Edge of SCLK		
Bits/Sample	SCLK Rate(s)	Notes
24	64, 128 Fs	single-speed mode, Fs= 32, 44.1, 48 KHz
	64 Fs	double-speed mode, Fs= 64, 88.2, 96 KHz
	not supported	quad-speed mode, Fs= 176.4, 192 KHz

Figure 11. ADCIN1/ADCIN2 Serial Audio Format

For proper operation, the CS42516 must be configured to select which SCLK/LRCK is being used to clock the external ADCs. The EXT ADC SCLK bit in register “Misc Control (address 05h)” on page 41, must be set accordingly. Set this bit to ‘1’ if the external ADCs are wired using the CODEC_SP clocks. If the ADCs are wired to use the SAI_SP clocks, set this bit to ‘0’.

3.6.4 One Line Mode(OLM) Configurations

3.6.4.1 OLM Config #1

One Line Mode Configuration #1 can support up to 6 channels of DAC data, 6 channels of ADC data and 2 channels of S/PDIF received data. This is the only configuration which will support up to 24-bit samples at a sampling frequency of 48kHz on all channels for both the DAC and ADC.

Register / Bit Settings	Description
Functional Mode Register (addr = 03h)	
Set CODEC_FMx = SAI_FMx = 00,01,10	CX_LRCK must equal SAI_LRCK; sample rate conversion not supported
Set ADC_SP SELx = 00	Configure ADC data on CX_SDOUT, S/PDIF data on SAI_SDOUT
Interface Format Register (addr = 04h)	
Set DIFx bits to proper serial format	Select the digital interface format when not in one line mode
Set ADC_OLx bits = 00,01,10	Select ADC operating mode, see table below for valid combinations
Set DAC_OLx bits = 00,01,10	Select DAC operating mode, see table below for valid combinations
Misc. Control Register (addr = 05h)	
Set CODEC_SP M/S = 1	Configure CODEC Serial Port to master mode.
Set SAI_SP M/S = 1	Configure Serial Audio Interface Port to master mode.
Set EXT ADC SCLK = 0	Identify external ADC clock source as Serial Audio Interface Port.

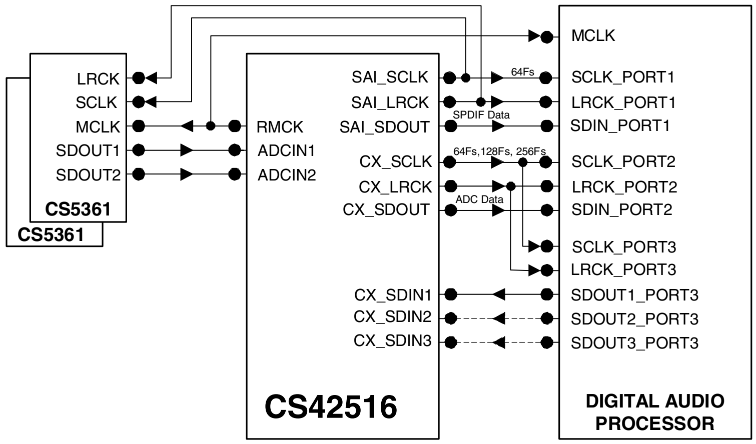


Figure 12. OLM Configuration #1

CX_SDOUT=ADC Data SAI_SDOUT=S/PDIF Data		**DAC Mode**		
		Not One Line Mode	**One Line Mode #1**	**One Line Mode #2**
ADC Mode	**Not One Line Mode**	CX_SCLK=64Fs CX_LRCK=SSM/DSM/QSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	CX_SCLK=128Fs CX_LRCK=SSM/DSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	not valid
	One Line Mode #1	CX_SCLK=128Fs CX_LRCK=SSM/DSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	CX_SCLK=128Fs CX_LRCK=SSM/DSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	not valid
	One Line Mode #2	CX_SCLK=256Fs CX_LRCK=SSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	not valid	CX_SCLK=256Fs CX_LRCK=SSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK

3.6.4.2 OLM Config #2

This configuration will support up to 6 channels of DAC data, 6 channels of ADC data and no channels of S/PDIF received data and will handle up to 20-bit samples at a sampling frequency of 96kHz on all channels for both the DAC and ADC. The output data stream of the internal and external ADCs is configured to use the SAI_SDOUT output and run at the SAI_SP clock speeds.

Register / Bit Settings	Description
Functional Mode Register (addr = 03h)	
Set CODEC_FMx = SAI_FMx = 00,01,10	CX_LRCK must equal SAI_LRCK; sample rate conversion not supported
Set ADC_SP SELx = 10	Configure ADC data to use SAI_SDOUT and SAI_SP Clocks. S/PDIF data is not supported in this configuration
Interface Format Register (addr = 04h)	
Set DIFx bits to proper serial format	Select the digital interface format when not in one line mode
Set ADC_OLx bits = 00,01,10	Select ADC operating mode, see table below for valid combinations
Set DAC_OLx bits = 00,01	Select DAC operating mode, see table below for valid combinations
Misc. Control Register (addr = 05h)	
Set CODEC_SP M/S = 1	Set CODEC Serial Port to master mode.
Set SAI_SP M/S = 1	Set Serial Audio Interface Port to master mode.
Set EXT ADC SCLK = 1	Identify external ADC clock source as CODEC Serial Port.

CX_SDOUT= not used SAI_SDOUT=ADC Data		**DAC Mode**		
		Not One Line Mode	**One Line Mode #1**	**One Line Mode #2**
ADC Mode	**Not One Line Mode**	CX_SCLK=64Fs CX_LRCK=SSM/DSM/QSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	CX_SCLK=128Fs CX_LRCK=SSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	not valid
	One Line Mode #1	CX_SCLK=64Fs CX_LRCK=SSM/DSM SAI_SCLK=128Fs SAI_LRCK=CX_LRCK	CX_SCLK=128Fs CX_LRCK=SSM SAI_SCLK=128Fs SAI_LRCK=CX_LRCK	not valid
	One Line Mode #2	CX_SCLK=64Fs CX_LRCK=SSM SAI_SCLK=256Fs SAI_LRCK=CX_LRCK	not valid	not valid

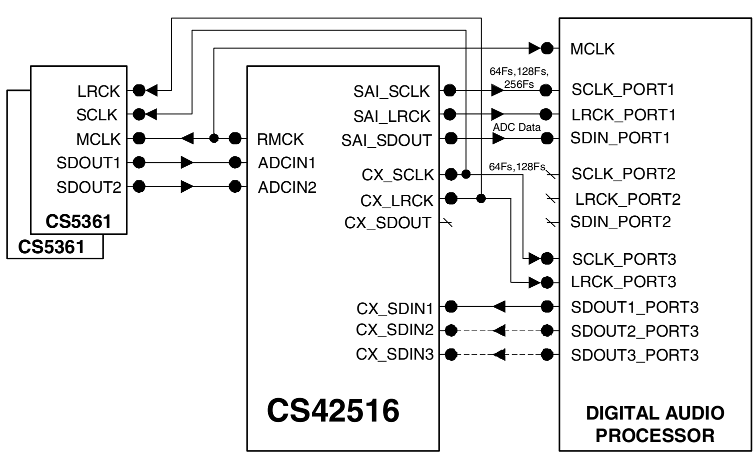


Figure 13. OLM Configuration #2

3.6.4.3 OLM Config #3

This One Line Mode configuration #3 will support up to 6 channels of DAC data, 6 channels of ADC data and 2 channels of S/PDIF received data and will handle up to 20-bit samples at a sampling frequency of 48kHz on all channels for both the DAC and ADC. The output data stream of the internal and external ADCs is configured to use the CX_SDOUT output and run at the CODEC_SP clock speeds. One Line Mode #2, which supports 24-bit samples, is not supported by this configuration.

Register / Bit Settings	Description
Functional Mode Register (addr = 03h)	
Set CODEC_FMx = SAI_FMx = 00,01,10	CX_LRCK must equal SAI_LRCK; sample rate conversion not supported
Set ADC_SP SELx = 00	Configure ADC data to use CX_SDOUT and CODEC_SP Clocks. S/PDIF data is supported on SAI_SDOUT
Interface Format Register (addr = 04h)	
Set DIFx bits to proper serial format	Select the digital interface format when not in one line mode
Set ADC_OLx bits = 00,01	Select ADC operating mode, see table below for valid combinations
Set DAC_OLx bits = 00,01	Select DAC operating mode, see table below for valid combinations
Misc. Control Register (addr = 05h)	
Set CODEC_SP M/S = 1	Set CODEC Serial Port to master mode.
Set SAI_SP M/S = 0 or 1	Set Serial Audio Interface Port to master mode or slave mode.
Set EXT ADC SCLK = 1	Identify external ADC clock source as CODEC Serial Port.

CX_SDOUT= ADC Data SAI_SDOUT=S/PDIF Data		**DAC Mode**		
		Not One Line Mode	**One Line Mode #1**	**One Line Mode #2**
ADC Mode	**Not One Line Mode**	CX_SCLK=64Fs CX_LRCK=SSM/DSM/QSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	CX_SCLK=128Fs CX_LRCK=SSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	not valid
	One Line Mode #1	CX_SCLK=128Fs CX_LRCK=SSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	CX_SCLK=128Fs CX_LRCK=SSM SAI_SCLK=64Fs SAI_LRCK=CX_LRCK	not valid
	One Line Mode #2	not valid	not valid	not valid

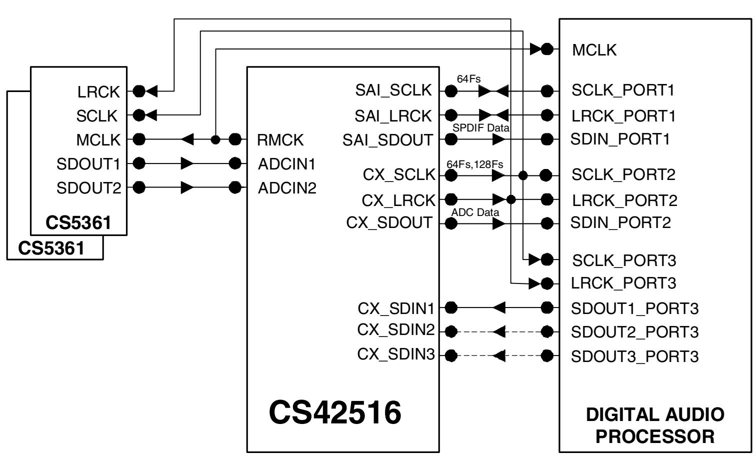


Figure 14. OLM Configuration #3

3.6.4.4 OLM Config #4

This configuration will support up to 6 channels of DAC data, 6 channels of ADC data and no channels of S/PDIF received data. OLM Config #4 will handle up to 20-bit ADC samples at an Fs of 48kHz and 24-bit DAC samples at an Fs of 48kHz. Since the ADCs data stream is configured to use the SAI_SDOUT output and the internal and external ADCs are clocked from the SAI_SP, then the sample rate for the CODEC Serial Port can be different from the sample rate of the Serial Audio Interface serial port.

Register / Bit Settings	Description
Functional Mode Register (addr = 03h)	
Set CODEC_FMx = 00,01,10	CX_LRCK can run at SSM, DSM, or QSM independent of SAI_LRCK
Set SAI_FMx = 00,01,10	SAI_LRCK can run at SSM, DSM, or QSM independent of CX_LRCK
Set ADC_SP SELx = 10	Configure ADC data to use SAI_SDOUT and SAI_SP Clocks. S/PDIF data is not supported in this configuration
Interface Format Register (addr = 04h)	
Set DIFx bits to proper serial format	Select the digital interface format when not in one line mode
Set ADC_OLx bits = 00,01	Select ADC operating mode, see table below for valid combinations
Set DAC_OLx bits = 00,01,10	Select DAC operating mode, see table below for valid combinations
Misc. Control Register (addr = 05h)	
Set CODEC_SP M/S = 1	Set CODEC Serial Port to master mode.
Set SAI_SP M/S = 0 or 1	Set Serial Audio Interface Port to master mode or slave mode.
Set EXT ADC SCLK = 0	Identify external ADC clock source as Serial Audio Interface Port.

CX_SDOUT= not used SAI_SDOUT=ADC Data		**DAC Mode**		
		Not One Line Mode	**One Line Mode #1**	**One Line Mode #2**
ADC Mode	**Not One Line Mode**	CX_SCLK=64Fs CX_LRCK=SSM/DSM/QSM SAI_SCLK=64Fs SAI_LRCK=SSM/DSM/QSM	CX_SCLK=128Fs CX_LRCK=SSM/DSM SAI_SCLK=64Fs SAI_LRCK=SSM/DSM/QSM	CX_SCLK=256Fs CX_LRCK=SSM SAI_SCLK=64Fs SAI_LRCK=SSM/DSM/QSM
	One Line Mode #1	CX_SCLK=64Fs CX_LRCK=SSM/DSM/QSM SAI_SCLK=128Fs SAI_LRCK=SSM	CX_SCLK=128Fs CX_LRCK=SSM/DSM SAI_SCLK=128Fs SAI_LRCK=SSM	CX_SCLK=256Fs CX_LRCK=SSM SAI_SCLK=128Fs SAI_LRCK=SSM
	One Line Mode #2	not valid	not valid	not valid

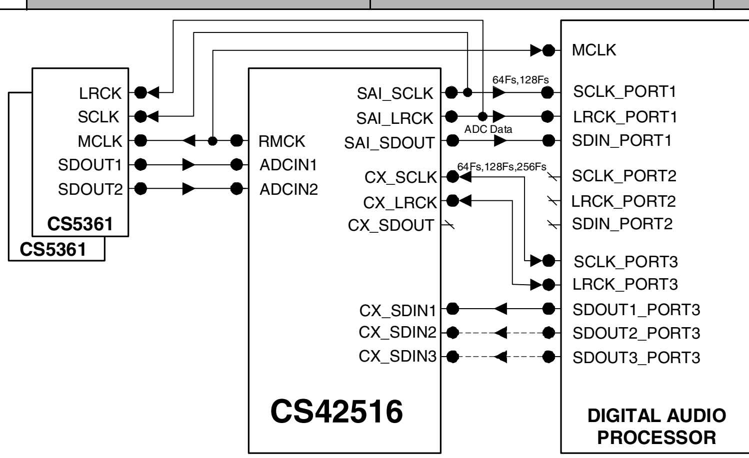


Figure 15. OLM Configuration #4

3.6.4.5 OLM Config #5

This configuration can support up to 6 channels of DAC data, 2 channels of ADC data and 2 channels of S/PDIF received data and will handle up to 24-bit samples at a sampling frequency of 48KHz on all channels for both the DAC and ADC. The output data stream of the internal ADCs can be configured to use the CX_SDOUT output and run at the CODEC_SP clock speeds or to use the SAI_SDOUT data output and run at the SAI_SP rate. The Codec_SP and SAI_SP can operate at different Fs rates.

Register / Bit Settings	Description
Functional Mode Register (addr = 03h)	
Set CODEC_FMx = 00,01,10	CX_LRCK can run at SSM, DSM, or QSM independent of SAI_LRCK
Set SAI_FMx = 00,01,10	SAI_LRCK can run at SSM, DSM, or QSM independent of CX_LRCK
Set ADC_SP SELx = 00,01,10	Configure ADC data to use CX_SDOUT and CODEC_SP clocks, or SAI_SDOUT and SAI_SP cocks.
Interface Format Register (addr = 04h)	
Set DIFx bits to proper serial format	Select the digital interface format when not in one line mode
Set ADC_OLx bits = 00	Set ADC operating mode to Not One Line Mode since only 2 channels of ADC are supported
Set DAC_OLx bits = 00,01	Select DAC operating mode, see table below for valid combinations
Misc. Control Register (addr = 05h)	
Set CODEC_SP M/S = 0 or 1	Set CODEC Serial Port to master mode or slave mode.
Set SAI_SP M/S = 0 or 1	Set Serial Audio Interface Port to master mode or slave mode.
Set EXT ADC SCLK = 0	External ADCs are not used. Leave bit in default state.

CX_SDOUT= ADC Data SAI_SDOUT=ADC or S/PDIF Data		**DAC Mode**		
		Not One Line Mode	**One Line Mode #1**	**One Line Mode #2**
ADC Mode	**Not One Line Mode**	CX_SCLK=64Fs CX_LRCK=SSM/DSM/QSM SAI_SCLK=64Fs SAI_LRCK=SSM/DSM/QSM	CX_SCLK=128Fs CX_LRCK=SSM/DSM SAI_SCLK=64Fs SAI_LRCK=SSM/DSM/QSM	not valid
	One Line Mode #1	not valid	not valid	not valid
	One Line Mode #2	not valid	not valid	not valid

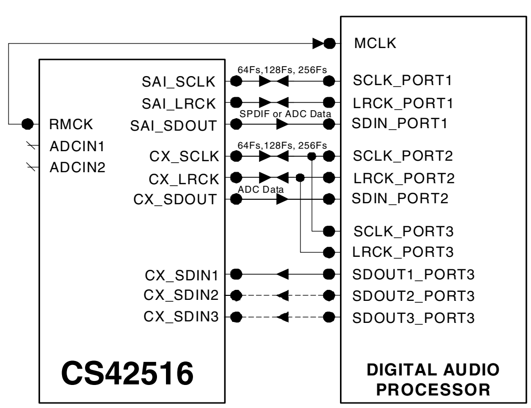


Figure 16. OLM Configuration #5

3.7 Control Port Description and Timing

The control port is used to access the registers, allowing the CS42516 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and I^{2}C, with the CS42516 acting as a slave device. SPI mode is selected if there is a high to low transition on the AD0/$\overline{\text{CS}}$ pin, after the $\overline{\text{RST}}$ pin has been brought high. I^{2}C mode is selected by connecting the AD0/$\overline{\text{CS}}$ pin through a resistor to VLC or DGND, thereby permanently selecting the desired AD0 bit address state.

3.7.1 SPI Mode

In SPI mode, $\overline{\text{CS}}$ is the CS42516 chip select signal, CCLK is the control port bit clock (input into the CS42516 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 17 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{\text{CS}}$ low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator (R/$\overline{\text{W}}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 KΩ resistor, if desired.

There is a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will autoincrement after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{\text{CS}}$ high) immediately after the MAP byte. The MAP auto increment bit (INCR) may be set or

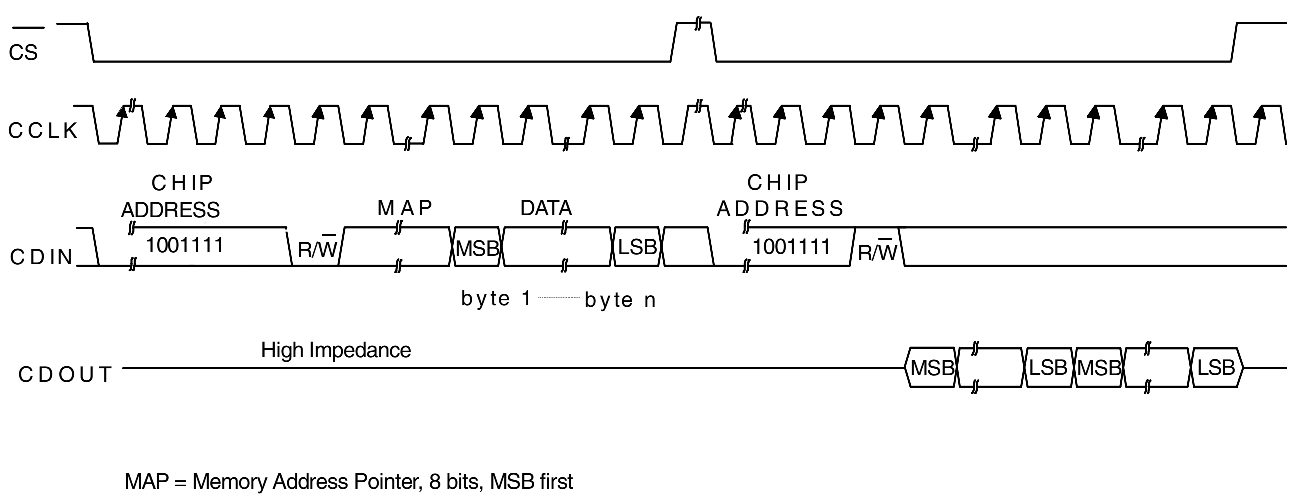


Figure 17. Control Port Timing in SPI Mode

not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.

3.7.2 I²C Mode

In I²C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{CS}$ pin. Pins AD0 and AD1 form the two least significant bits of the chip address and should be connected through a resistor to VLC or DGND as desired. The state of the pins is sensed while the CS42516 is being reset.

The signal timings for a read and write cycle are shown in Figure 18 and Figure 19. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS42516 after a Start condition consists of a 7 bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 5 bits of the 7-bit address field are fixed at 10011. To communicate with a CS42516, the chip address field, which is the first byte sent to the CS42516, should match 10011 followed by the settings of the AD1 and AD0. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42516 after each input byte is read, and is input to the CS42516 from the microcontroller after each transmitted byte.

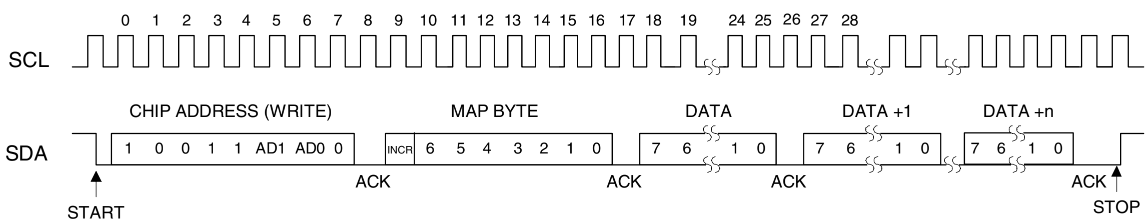


Figure 18. Control Port Timing, I²C Slave Mode Write

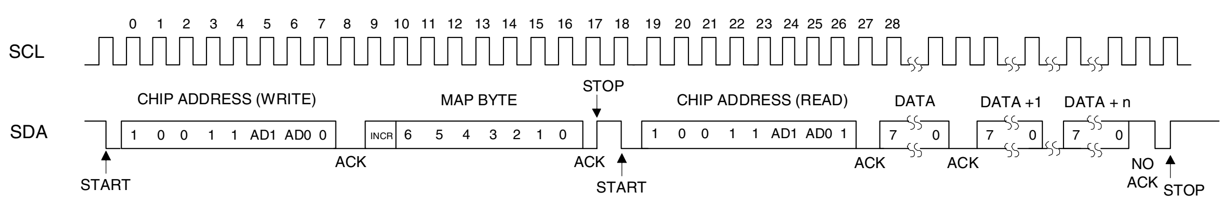


Figure 19. Control Port Timing, I²C Slave Mode Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 19, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 10011xx0 (chip address & write operation).

Receive acknowledge bit.

Send MAP byte, auto increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 10011xx1(chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

3.8 Interrupts

The CS42516 has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may be set to be active low, active high or active low with no active pull-up transistor. This last mode is used for active low, wired-OR hook-ups, with multiple peripherals connected to the microcontroller interrupt input pin.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. See “Interrupt Status (address 20h) (Read Only)” on page 52. Each source may be masked off through mask register bits. In addition, each source may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer.

3.9 Reset and Power-up

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be activated if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

When $\overline{\text{RST}}$ is low, the CS42516 enters a low power mode and all internal states are reset, including the control port and registers, and the outputs are muted. When $\overline{\text{RST}}$ is high, the control port becomes operational and the desired settings should be loaded into the control registers. Writing a 0 to the PDN bit in the Power Control Register will then cause the part to leave the low power state and begin operation. If the internal PLL is selected as the clock source, the serial audio outputs will be enabled after the PLL has settled. See “Power Control (address 02h)” on page 38 for more details.

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by setting the $\overline{\text{RST}}$ pin high. However, the voltage reference will take much longer to reach a final value due to the presence of external capacitance on the VREFP pin. A time delay of approximately 80ms is required after applying power to the device or after exiting a reset state. During this voltage reference ramp delay, all serial ports and DAC outputs will be automatically muted.

3.10 Power Supply, Grounding, and PCB layout

As with any high resolution converter, the CS42516 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA and VARX connected to clean supplies. VD, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VD may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VD.

For applications where the recovered input clock, output on the RMCK pin, is required to be low jitter, use a separate, low noise analog +5 V supply for VA, decoupled to AGND. In addition, a separate region of analog ground plane around the FILT+, VQ, LPFLT, REFGND, AGND, VA, VARX, RXP/GPO1-7 and RXP0 pins is recommended.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as near to the pins of the CS42516 as possible, with the low value ceramic capacitor being the nearest and should be mounted on the same side of the board as the CS42516 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+, VQ and LPFLT pins in order to avoid unwanted coupling into the modulators and PLL. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and REFGND. The CDB42518 evaluation board demonstrates the optimum layout and power supply arrangements.

4 REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
01h	ID	Chip_ID3	Chip_ID2	Chip_ID1	CHIP_ID0	Rev_ID3	Rev_ID2	Rev_ID1	Rev_ID0
	default	1	1	1	0	0	0	0	1
02h	Power Control	Reserved	PDN_RCVR	PDN_ADC	PDN_RSVD	PDN_DAC3	PDN_DAC2	PDN_DAC1	PDN
	default	0	0	0	0	0	0	0	1
03h	Functional Mode	CODEC_FM 1	CODEC_FM 0	SAI_FM1	SAI_FM0	ADC_SP SEL1	ADC_SP SEL0	DAC_DEM	RCVR_DEM
	default	0	0	0	0	0	0	0	0
04h	Interface Formats	DIF1	DIF0	ADC_OL1	ADC_OL0	DAC_OL1	DAC_OL0	RX_RJ16	DAC_RJ16
	default	0	1	0	0	0	0	0	0
05h	Misc Control	Ext ADC SCLK	Reserved	Reserved	FREEZE	FILTSEL	HPF_ FREEZE	CODEC_SP M/$\overline{S}$	SAI_SP M/$\overline{S}$
	default	0	0	0	0	0	0	1	1
06h	Clock Control	RMCK_DIV1	RMCK_DIV0	OMCK Freq1	OMCK Freq0	PLL_LRCK	SW_CTRL1	SW_CTRL0	Reserved
	default	0	0	0	0	0	0	1	0
07h	OMCK/PLL_CLK Ratio	RATIO7	RATIO6	RATIO5	RATIO4	RATIO3	RATIO2	RATIO1	RATIO0
	default	X	X	X	X	X	X	X	X
08h	RVCR Status	Digital Silence	Reserved	Reserved	Reserved	Active_CLK	RVCR_CLK 2	RVCR_CLK 1	RVCR_CLK 0
	default	X	X	X	X	X	X	X	X
09h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	X	X	X	X	X	X	X	X
0Ah	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	X	X	X	X	X	X	X	X
0Bh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	X	X	X	X	X	X	X	X
0Ch	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	X	X	X	X	X	X	X	X
0Dh	Volume Control	Reserved	SNGVOL	SZC1	SZC0	AMUTE	MUTE SAI_SP	RAMP_UP	RAMP_DN
	default	0	0	0	0	1	0	0	0
0Eh	Channel Mute	Reserved	Reserved	B3_MUTE	A3_MUTE	B2_MUTE	A2_MUTE	B1_MUTE	A1_MUTE
	default	0	0	0	0	0	0	0	0
0Fh	Vol. Control A1	A1_VOL7	A1_VOL6	A1_VOL5	A1_VOL4	A1_VOL3	A1_VOL2	A1_VOL1	A1_VOL0
	default	0	0	0	0	0	0	0	0
10h	Vol. Control B1	B1_VOL7	B1_VOL6	B1_VOL5	B1_VOL4	B1_VOL3	B1_VOL2	B1_VOL1	B1_VOL0
	default	0	0	0	0	0	0	0	0
11h	Vol. Control A2	A2_VOL7	A2_VOL6	A2_VOL5	A2_VOL4	A2_VOL3	A2_VOL2	A2_VOL1	A2_VOL0
	default	0	0	0	0	0	0	0	0
12h	Vol. Control B2	B2_VOL7	B2_VOL6	B2_VOL5	B2_VOL4	B2_VOL3	B2_VOL2	B2_VOL1	B2_VOL0
	default	0	0	0	0	0	0	0	0
13h	Vol. Control A3	A3_VOL7	A3_VOL6	A3_VOL5	A3_VOL4	A3_VOL3	A3_VOL2	A3_VOL1	A3_VOL0
	default	0	0	0	0	0	0	0	0
14h	Vol. Control B3	B3_VOL7	B3_VOL6	B3_VOL5	B3_VOL4	B3_VOL3	B3_VOL2	B3_VOL1	B3_VOL0
	default	0	0	0	0	0	0	0	0
15h	Reserved	A4_VOL7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
16h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
17h	Channel Invert	Reserved	Reserved	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
	default	0	0	0	0	0	0	0	0
18h	Mixing Ctrl Pair 1	P1_A=B	Reserved	Reserved	P1_ATAPI4	P1_ATAPI3	P1_ATAPI2	P1_ATAPI1	P1_ATAPI0
	default	0	0	0	0	1	0	0	1
19h	Mixing Ctrl Pair 2	P2_A=B	Reserved	Reserved	P2_ATAPI4	P2_ATAPI3	P2_ATAPI2	P2_ATAPI1	P2_ATAPI0
	default	0	0	0	0	1	0	0	1
1Ah	Mixing Ctrl Pair 3	P3_A=B	Reserved	Reserved	P3_ATAPI4	P3_ATAPI3	P3_ATAPI2	P3_ATAPI1	P3_ATAPI0
	default	0	0	0	0	1	0	0	1
1Bh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	1	0	0	1
1Ch	ADC Left Ch. Gain	Reserved	Reserved	LGAIN5	LGAIN4	LGAIN3	LGAIN2	LGAIN1	LGAIN0
	default	0	0	0	0	0	0	0	0
1Dh	ADC Right Ch. Gain	Reserved	Reserved	RGAIN5	RGAIN4	RGAIN3	RGAIN2	RGAIN1	RGAIN0
	default	0	0	0	0	0	0	0	0
1Eh	RCVR Mode Ctrl	Reserved	Reserved	Reserved	Reserved	INT1	INT0	HOLD1	HOLD0
	default	0	0	0	0	0	0	0	0
1Fh	RCVR Mode Ctrl 2	Reserved	TMUX2	TMUX1	TMUX0	Reserved	RMUX2	RMUX1	RMUX0
	default	0	0	0	0	0	0	0	0
20h	Interrupt Status	UNLOCK	Reserved	QCH	DETC	DETU	Reserved	OverFlow	RERR
	default	X	X	X	X	X	X	X	X
21h	Interrupt Mask	UNLOCKM	Reserved	QCHM	DETCM	DETUM	Reserved	OverFlowM	RERRM
	default	0	0	0	0	0	0	0	0
22h	Interrupt Mode MSB	UNLOCK1	Reserved	QCH1	DETC1	DETU1	Reserved	OF1	RERR1
	default	0	0	0	0	0	0	0	0
23h	Interrupt Mode LSB	UNLOCK0	Reserved	QCH0	DETC0	DETU0	Reserved	OF0	RERR0
	default	0	0	0	0	0	0	0	0
24h	Buffer Ctrl	Reserved	Reserved	Reserved	Reserved	Reserved	BSEL	CAM	CHS
	default	0	0	0	0	0	0	0	0
25h	RCVR CS Data	AUX3	AUX2	AUX1	AUX0	PRO	$\overline{\text{AUDIO}}$	COPY	ORIG
	default	X	X	X	X	X	X	X	X
26h	RCVR Errors	Reserved	QCRC	CCRC	UNLOCK	V	CONF	BIP	PAR
		X	X	X	X	X	X	X	X
27h	RCVR Errors Mask	Reserved	QCRCM	CCRCM	UNLOCKM	VM	CONFM	BIPM	PARM
	default	0	0	0	0	0	0	0	0
28h	MUTEC	Reserved	Reserved	Polarity	M_AOUTA1	M_AOUTB1	M_AOUTA2 M_AOUTB2	M_AOUTA3 M_AOUTB3	Reserved
	default	0	0	0	1	1	1	1	1
29h	RXP7/GPO7	Mode1	Mode0	Polarity	Function4	Function3	Function2	Function1	Function0
	default	0	0	0	0	0	0	0	0
2Ah	RXP6/GPO6	Mode1	Mode0	Polarity	Function4	Function3	Function2	Function1	Function0
	default	0	0	0	0	0	0	0	0
2Bh	RXP5/GPO5	Mode1	Mode0	Polarity	Function4	Function3	Function2	Function1	Function0
	default	0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
2Ch	RXP4/GPO4	Mode1	Mode0	Polarity	Function4	Function3	Function2	Function1	Function0
	default	0	0	0	0	0	0	0	0
2Dh	RXP3/GPO3	Mode1	Mode0	Polarity	Function4	Function3	Function2	Function1	Function0
	default	0	0	0	0	0	0	0	0
2Eh	RXP2/GPO2	Mode1	Mode0	Polarity	Function4	Function3	Function2	Function1	Function0
	default	0	0	0	0	0	0	0	0
2Fh	RXP1/GPO1	Mode1	Mode0	Polarity	Function4	Function3	Function2	Function1	Function0
	default	0	0	0	0	0	0	0	0
30h	Q Subcode	Address3	Address2	Address1	Address0	Control3	Control2	Control1	Control0
	default	X	X	X	X	X	X	X	X
31h	Q Subcode	Track7	Track6	Track5	Track4	Track3	Track2	Track1	Track0
	default	X	X	X	X	X	X	X	X
32h	Q Subcode	Index7	Index6	Index5	Index4	Index3	Index2	Index1	Index0
	default	X	X	X	X	X	X	X	X
33h	Q Subcode	Minute7	Minute6	Minute5	Minute4	Minute3	Minute2	Minute1	Minute0
	default	X	X	X	X	X	X	X	X
34h	Q Subcode	Second7	Second6	Second5	Second4	Second3	Second2	Second1	Second0
	default	X	X	X	X	X	X	X	X
35h	Q Subcode	Frame7	Frame6	Frame5	Frame4	Frame3	Frame2	Frame1	Frame0
	default	X	X	X	X	X	X	X	X
36h	Q Subcode	Zero7	Zero6	Zero5	Zero4	Zero3	Zero2	Zero1	Zero0
	default	X	X	X	X	X	X	X	X
37h	Q Subcode	A.Minute7	A.Minute6	A.Minute5	A.Minute4	A.Minute3	A.Minute2	A.Minute1	A.Minute0
	default	X	X	X	X	X	X	X	X
38h	Q Subcode	A.Second7	A.Second6	A.Second5	A.Second4	A.Second3	A.Second2	A.Second1	A.Second0
	default	X	X	X	X	X	X	X	X
39h	Q Subcode	A.Frame7	A.Frame6	A.Frame5	A.Frame4	A.Frame3	A.Frame2	A.Frame1	A.Frame0
	default	X	X	X	X	X	X	X	X
3Ah -	C or U Data Buffer	CU Buffer7	CU Buffer6	CU Buffer5	CU Buffer4	CU Buffer3	CU Buffer2	CU Buffer1	CU Buffer0
51h	default	X	X	X	X	X	X	X	X

5 REGISTER DESCRIPTION

All registers are read/write except for I.D. and Revision Register, OMCK/PLL_CLK Ratio Register, Interrupt Status Register, Q-Channel Subcode Bytes and C-bit or U-bit Data Buffer, which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.

5.1 *Memory Address Pointer (MAP)*

Not a register

7	6	5	4	3	2	1	0
INCR	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0

5.1.1 INCREMENT(INCR)

Default = 1
Function:

memory address pointer auto increment control
0 -MAP is not incremented automatically.
1 -internal MAP is automatically incremented after each read or write.

5.1.2 MEMORY ADDRESS POINTER (MAPX)

Default = 0000001
Function:

Memory address pointer (MAP). Sets the register address that will be read or written by the control port.

5.2 CS42516 *I.D. and Revision Register (address 01h) (Read Only)*

7	6	5	4	3	2	1	0
Chip_ID3	Chip_ID2	Chip_ID1	CHIP_ID0	Rev_ID3	Rev_ID2	Rev_ID1	Rev_ID0

5.2.1 CHIP I.D. (CHIP_IDX)

Default = 1110
Function:

I.D. code for the CS42516. Permanently set to 1110.

5.2.2 CHIP REVISION (REV_IDX)

Default = 0001
Function:

CS42516 revision level. Revision B is coded as 0001.

5.3 Power Control (address 02h)

7	6	5	4	3	2	1	0
Reserved	PDN_RCVR	PDN_ADC	PDN_RSVD	PDN_DAC3	PDN_DAC2	PDN_DAC1	PDN

5.3.1 POWER DOWN RECEIVER (PDN_RCVR)

Default = 0
Function:

When enabled the S/PDIF receiver and PLL will remain in a reset state. It is advised that any change of this bit be made while the DACs are muted or the power down bit (PDN) is enabled to eliminate the possibility of audible artifacts.

5.3.2 POWER DOWN ADC (PDN_ADC)

Default = 0
Function:

When enabled the stereo analog to digital converter will remain in a reset state. It is advised that any change of this bit be made while the DACs are muted or the power down bit (PDN) is enabled to eliminate the possibility of audible artifacts.

5.3.3 POWER DOWN RESERVE TEST (PDN_RSVD)

Default = 0
Function:

This bit is a reserved power down bit used for test purposes only. For proper operation, this bit must be set to ‘1’.

5.3.4 POWER DOWN DAC PAIRS (PDN_DACX)

Default = 0
Function:

When enabled the respective DAC channel pair x (AOUTAx and AOUTBx) will remain in a reset state.

5.3.5 POWER DOWN (PDN)

Default = 1
Function:

The entire device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power down bit defaults to ‘enabled’ on power-up and must be disabled before normal operation can occur.

5.4 Functional Mode (address 03h)

7	6	5	4	3	2	1	0
CODEC_FM1	CODEC_FM0	SAI_FM1	SAI_FM0	ADC_SP SEL1	ADC_SP SEL0	DAC_DEM	RCVR_DEM

5.4.1 CODEC FUNCTIONAL MODE (CODEC_FMX)

Default = 00
00 - Single-Speed Mode (4 to 50 kHz sample rates)

01 - Double-Speed Mode (50 to 100 kHz sample rates)
10 - Quad-Speed Mode (100 to 192 kHz sample rates)
11 - Reserved
Function:

Selects the required range of sample rates for all converters clocked from the CODEC serial port (CODEC_SP). These bits must be set to the corresponding sample rate range when the CODEC_SP is in Master or Slave mode.

5.4.2 SERIAL AUDIO INTERFACE FUNCTIONAL MODE (SAI_FMX)

Default = 00
00 - Single-Speed Mode (4 to 50 kHz sample rates)
01 - Double-Speed Mode (50 to 100 kHz sample rates)
10 - Quad-Speed Mode (100 to 192 kHz sample rates)
11 - Reserved
Function:

Selects the required range of sample rates for the Serial Audio Interface port(SAI_SP). These bits must be set to the corresponding sample rate range when the SAI_SP is in Master or Slave mode.

5.4.3 ADC SERIAL PORT SELECT (ADC_SP SELX)

Default = 00
00 - Serial data on CX_SDOUT pin, clocked from the CODEC_SP. S/PDIF data on SAI_SDOUT pin.
01 - Serial data on CX_SDOUT pin, clocked from the SAI_SP. S/PDIF data on SAI_SDOUT pin.
10 - Serial data on SAI_SDOUT pin, clocked from the SAI_SP. No S/PDIF data available.
11 - Reserved
Function:

Selects the desired clocks and routing for the ADC serial output.

5.4.4 DAC DE-EMPHASIS CONTROL (DAC_DEM)

Default = 0
Function:

Enables the digital filter to maintain the standard 15µs/50µs digital de-emphasis filter response at the auto-detected sample rate of either 32, 44.1, or 48 kHz. De-emphasis will not be enabled, regardless of this register setting, at any other sample rate.

5.4.5 RECEIVER AUTO DE-EMPHASIS CONTROL (RCVR_DEM)

Default = 0
Function:

When enabled, de-emphasis will be automatically applied when emphasis is detected based on the channel status bits. The appropriate digital filter will be selected to maintain the standard 15µs/50µs digital de-emphasis filter response at the auto-detected sample rate of either 32, 44.1, or 48 kHz.

5.5 Interface Formats (address 04h)

7	6	5	4	3	2	1	0
DIF1	DIF0	ADC_OL1	ADC_OL0	DAC_OL1	DAC_OL0	SAI_RJ16	CODEC_RJ16

5.5.1 DIGITAL INTERFACE FORMAT (DIFX)

Default = 01
Function:

These bits select the digital interface format used for the CODEC Serial Port and Serial Audio Interface Port when not in one_line mode. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 6 - 8.

DIF1	DIF0	Description	Format	Figure
0	0	Left Justified, up to 24-bit data	0	7
0	1	I^2S, up to 24-bit data	1	6
1	0	Right Justified, 16-bit or 24-bit data	2	8
1	1	reserved	-	-

Table 6. Receiver Digital Interface Formats

5.5.2 ADC ONE_LINE MODE (ADC_OLX)

Default = 00
Function:

These bits select which mode the ADC will use. By default one-line mode is disabled but can be selected using these bits. Please see Figures 9 and 10 to see the format of one-line mode 1 and one-line mode 2.

ADC_OL1	ADC_OL2	Description	Format	Figure
0	0	DIF: take the DIF setting from reg04h[7:6]	-	-
0	1	One-Line #1	3	9
1	0	One-Line #2	4	10
1	1	reserved	-	-

Table 7. ADC One_Line Mode

5.5.3 DAC ONE_LINE MODE (DAC_OLX)

Default = 00
Function:

These bits select which mode the DAC will use. By default one-line mode is disabled but can be selected using these bits. Please see Figures 9 and 10 to see the format of one-line mode 1 and one-line mode 2.

DAC_OL1	DAC_OL2	Description	Format	Figure
0	0	DIF: take the DIF setting from reg04h[7:6]	-	-
0	1	One-Line #1	3	9
1	0	One-Line #2	4	10
1	1	reserved	-	-

Table 8. DAC One_Line Mode

5.5.4 SAI RIGHT JUSTIFIED BITS (SAI_RJ16)

Default = 0
Function:

This bit determines how many bits to use during right_justified mode for the Serial Audio Interface Port. By default the receiver will be in RJ24 bits but can be set to RJ16 bits.

0 - 24 bit mode.
1 - 16 bit mode.

5.5.5 CODEC RIGHT JUSTIFIED BITS (CODEC_RJ16)

Default = 0
Function:

This bit determines how many bits to use during right_justified mode for the DAC and ADC within the CODEC Serial Port. By default the DAC and ADC will be in RJ24 bits but can be set to RJ16 bits.

0 - 24 bit mode.
1 - 16 bit mode.

5.6 Misc Control (address 05h)

7	6	5	4	3	2	1	0
Ext ADC SCLK	Reserved	Reserved	FREEZE	FILT_SEL	HPF_FREEZE	CODEC_SP M/$\overline{S}$	SAI_SP M/$\overline{S}$

5.6.1 EXTERNAL ADC SCLK SELECT (EXT ADC SCLK)

Default = 0
Function:

This bit identifies the SCLK source for the external ADCs attached to the ADCIN1/2 ports when using one line mode of operation.

0 - SAI_SCLK is used as external ADC SCLK.
1 - CX_SCLK is used as external ADC SCLK.

5.6.2 FREEZE CONTROLS (FREEZE)

Default = 0
Function:

This function will freeze the previous output of, and allow modifications to be made, to the Chnl Volume Control (address 0Fh-16h), Channel Invert (address 17h) and Mixing Control Pair (address 18h-1Bh) registers without the changes taking effect until the FREEZE is disabled. To make multiple changes in these control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

5.6.3 INTERPOLATION FILTER SELECT (FILT_SEL)

Default = 0
Function:

This feature allows the user to select whether the DAC interpolation filter has a fast or slow roll off. For filter characteristics please see “D/A Digital Filter Characteristics” on page 66.

0 - Fast roll off.
1 - Slow roll off.

5.6.4 HIGH PASS FILTER FREEZE (HPF_FREEZE)

Default = 0
Function:

The CS42516 includes a high pass filter after the decimator to remove the indeterminate DC offsets introduced by the analog input buffer stage and the analog modulator. The first-order high pass filter response characteristics are detailed in “A/D Digital Filter Characteristics” on page 62. The filter scales linearly with the sample rate of the ADC.

5.6.5 CODEC SERIAL PORT MASTER/SLAVE SELECT (CODEC_SP M/$\overline{S}$)

Default = 1
Function:

In Master mode, CX_SCLK and CX_LRCK are outputs. Internal dividers will divide the master clock to generate the serial clock and left/right clock. In Slave mode, CX_SCLK and CX_LRCK become inputs. If the internal MCLK is using the output of the PLL and the SAI serial port is in Master Mode, then one of these conditions must be met for proper operation:

1). The codec serial port, CX_SP, must also be in Master Mode,

2). If the CX_SP is in slave mode, then CX_LRCK and CX_SCLK must be present.

5.6.6 SERIAL AUDIO INTERFACE SERIAL PORT MASTER/SLAVE SELECT (SAI_SP M/$\overline{S}$)

Default = 1
Function:

In Master mode, SAI_SCLK and SAI_LRCK are outputs. Internal dividers will divide the master clock to generate the serial clock and left/right clock. In Slave mode, SAI_SCLK and SAI_LRCK become inputs.If the internal MCLK is using the output of the PLL and the SAI serial port is in Master Mode, then one of these conditions must be met for proper operation:

1). The codec serial port, CX_SP, must also be in Master Mode,

2). If the CX_SP is in slave mode, then CX_LRCK and CX_SCLK must be present.

5.7 Clock Control (address 06h)

7	6	5	4	3	2	1	0
RMCK_DIV1	RMCK_DIV0	OMCK Freq1	OMCK Freq0	PLL_LRCK	SW_CTRL1	SW_CTRL0	Reserved

5.7.1 RMCK DIVIDE (RMCK_DIVX)

Default = 00
Function:

Divides/multiplies the internal MCLK, either from the PLL or OMCK, by the selected factor.

RMCK_DIV1	RMCK_DIV0	Description
0	0	Divide by 1
0	1	Divide by 2
1	0	Divide by 4
1	1	Multiply by 2

Table 9. RMCK Divider Settings

5.7.2 OMCK FREQUENCY (OMCK FREQX)

Default = 00
Function:

Sets the appropriate frequency for the supplied OMCK.

OMCK Freq1	OMCK Freq0	Description
0	0	11.2896 MHz or 12.2880 MHz
0	1	16.9344 MHz or 18.4320 MHz
1	0	22.5792 MHz or 24.5760 MHz
1	1	Reserved

Table 10. OMCK Frequency Settings

5.7.3 PLL LOCK TO LRCK (PLL_LRCK)

Default = 0
0 - Disabled
1 - Enabled
Function:

When enabled, the internal PLL of the CS42516 will lock to the LRCK of the receiver serial port.

5.7.4 MASTER CLOCK SOURCE SELECT (SW_CTRLX)

Default = 01
Function:

These two bits, along with the UNLOCK bit in register "Interrupt Status (address 20h) (Read Only)" on page 52, determine the master clock source for the CS42516. When SW_CTRL1 and SW_CTRL0 are set to '00'b, selecting the output of the PLL as the internal clock source, and the PLL becomes unlocked, then RMCK will equal OMCK, but all internal and serial port timings are not valid.

SW_CTRL1	SW_CTRL0	UNLOCK	Description
0	0	X	Manual setting, MCLK sourced from PLL.
0	1	X	Manual setting, MCLK sourced from OMCK.
1	0	0 1	Hold, keep same MCLK source. Auto switch, MCLK sourced from OMCK.
1	1	0 1	Auto switch, MCLK sourced from PLL. Auto switch, MCLK sourced from OMCK.

Table 11. Master Clock Source Select

5.8 OMCK/PLL_CLK Ratio (address 07h) (Read Only)

7	6	5	4	3	2	1	0
RATIO7(2^{1})	RATIO6(2^{0})	RATIO5(2^{-1})	RATIO4(2^{-2})	RATIO3(2^{-3})	RATIO2(2^{-4})	RATIO1(2^{-5})	RATIO0(2^{-6})

5.8.1 OMCK/PLL_CLK RATIO (RATIOX)

Default = sixth
Function:

This register allows the user to find the exact absolute frequency of the recovered MCLK coming from the PLL. This value is represented as an integer (RATIO7:6) and a fractional (RATIO5:0) part. For example, an OMCK/PLL_CLK ratio of 1.5 would be displayed as 60h.

5.9 RVCR Status (address 08h) (Read Only)

7	6	5	4	3	2	1	0
Digital Silence	Reserved	Reserved	Reserved	Active_CLK	RVCR_CLK2	RVCR_CLK1	RVCR_CLK0

5.9.1 DIGITAL SILENCE DETECTION (DIGITAL SILENCE)

Default = x
0 - Digital Silence not detected
1 - Digital Silence detected
Function:

The CS42516 will auto-detect a digital silence condition when 1548 consecutive zeros have been detected.

5.9.2 SYSTEM CLOCK SELECTION (ACTIVE_CLK)

Default = x
0 - Output of PLL
1 - OMCK
Function:

This bit identifies the source of the internal system clock (MCLK).

5.9.3 RECEIVER CLOCK FREQUENCY (RCVR_CLKX)

Default = xxxh
Function:

The CS42516 will auto-detect the ratio between the OMCK and the recovered clock from the PLL, which is displayed in register 07h. Based on this ratio, the absolute frequency of the PLL clock can be determined, and this information is displayed according to the following table. If the absolute frequency of the PLL clock does not match one of the given frequencies, this register will display the closest available value.

RCVR_CLK2	RCVR_CLK1	RCVR_CLK0	Description
0	0	0	8.1920 MHz
0	0	1	11.2896 MHz
0	1	0	12.288 MHz
0	1	1	16.3840 MHz
1	0	0	22.5792 MHz
1	0	1	24.5760 MHz
1	1	0	45.1584 MHz
1	1	1	49.1520 MHz

Table 12. Receiver Clock Frequency Detection

5.10 Volume Control (address 0Dh)

7	6	5	4	3	2	1	0
Reserved	SNGVOL	SZC1	SZC0	AMUTE	MUTE SAI_SP	RAMP_UP	RAMP_DN

5.10.1 SINGLE VOLUME CONTROL (SNGVOL)

Default = 0
Function:

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on all channels is determined by the A1 Channel Volume Control register and the other Volume Control registers are ignored.

5.10.2 SOFT RAMP AND ZERO CROSS CONTROL (SZCX)

Default = 00
00 - Immediate Change
01 - Zero Cross
10 - Soft Ramp
11 - Soft Ramp on Zero Crossings
Function:

Immediate Change

When Immediate Change is selected all level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp on Zero Crossing

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

5.10.3 AUTO-MUTE (AMUTE)

Default = 1
0 - Disabled
1 - Enabled
Function:

The Digital-to-Analog converters of the CS42516 will mute the output following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the MUTEC pin will go active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits (SZC1:0).

5.10.4 SERIAL AUDIO INTERFACE SERIAL PORT MUTE (MUTE SAI_SP)

Default = 0
0 - Disabled
1 - Enabled
Function:

When enabled, the Serial Audio Interface serial port (SAI_SP) will be muted.

5.10.5 SOFT VOLUME RAMP-UP AFTER ERROR (RMP_UP)

Default = 0
0 - Disabled
1 - Enabled
Function:

An un-mute will be performed after executing a filter mode change, after a MCLK/LRCK ratio change or error, and after changing the Functional Mode. When this feature is enabled, this un-mute is effected, similar to attenuation changes, by the Soft and Zero Cross bits (SZC1:0). When disabled, an immediate un-mute is performed in these instances.

Note: For best results, it is recommended that this bit be used in conjunction with the RMP_DN bit.

5.10.6 SOFT RAMP-DOWN BEFORE FILTER MODE CHANGE (RMP_DN)

Default = 0
0 - Disabled
1 - Enabled
Function:

A mute will be performed prior to executing a filter mode or de-emphasis mode change. When this feature is enabled, this mute is effected, similar to attenuation changes, by the Soft and Zero Cross bits (SZC1:0). When disabled, an immediate mute is performed prior to executing a filter mode or de-emphasis mode change.

Note: For best results, it is recommended that this bit be used in conjunction with the RMP_UP bit.

5.11 Channel Mute (address 0Eh)

7	6	5	4	3	2	1	0
Reserved	Reserved	B3_MUTE	A3_MUTE	B2_MUTE	A2_MUTE	B1_MUTE	A1_MUTE

5.11.1 INDEPENDENT CHANNEL MUTE (XX_MUTE)

Default = 0
0 - Disabled
1 - Enabled
Function:

The Digital-to-Analog converter outputs of the CS42516 will mute when enabled. The quiescent voltage on the outputs will be retained. The muting function is effected, similar to attenuation changes, by the Soft and Zero Cross bits (SZC1:0).

5.12 Volume Control (addresses 0Fh, 10h, 11h, 12h, 13h, 14h)

7	6	5	4	3	2	1	0
xx_VOL7	xx_VOL6	xx_VOL5	xx_VOL4	xx_VOL3	xx_VOL2	xx_VOL1	xx_VOL0

5.12.1 VOLUME CONTROL (XX_VOL)

Default = 0
Function:

The Digital Volume Control registers allow independent control of the signal levels in 0.5 dB increments from 0 to -127 dB. Volume settings are decoded as shown in Table 13. The volume changes are implemented as dictated by the Soft and Zero Cross bits (SZC1:0). All volume settings less than -127 dB are equivalent to enabling the MUTE bit for the given channel.

Binary Code	Decimal Value	Volume Setting
00000000	0	0 dB
00101000	40	-20 dB
01010000	80	-40 dB
01111000	120	-60 dB
10110100	180	-90 dB

Table 13. Example Digital Volume Settings

5.13 Channel Invert (address 17h)

7	6	5	4	3	2	1	0
Reserved	Reserved	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1

5.13.1 INVERT SIGNAL POLARITY (INV_XX)

Default = 0
0 - Disabled
1 - Enabled
Function:

When enabled, these bits will invert the signal polarity of their respective channels.

5.14 Mixing Control Pair 1 (Channels A1 & B1)(address 18h) Mixing Control Pair 2 (Channels A2 & B2)(address 19h) Mixing Control Pair 3 (Channels A3 & B3)(address 1Ah)

7	6	5	4	3	2	1	0
Px_A=B	Reserved	Reserved	Px_ATAPI4	Px_ATAPI3	Px_ATAPI2	Px_ATAPI1	Px_ATAPI0

5.14.1 CHANNEL A VOLUME = CHANNEL B VOLUME (PX_A=B)

Default = 0
0 - Disabled
1 - Enabled
Function:

The AOUTAx and AOUTBx volume levels are independently controlled by the A and the B Channel Volume Control registers when this function is disabled. The volume on both AOUTAx and AOUTBx are determined by the A Channel Volume Control registers (per A-B pair), and the B Channel Volume Control registers are ignored when this function is enabled.

5.14.2 ATAPI CHANNEL MIXING AND MUTING (PX_ATAPIX)

Default = 01001

Function:

The CS42516 implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 14 and Figure 2 for additional information.

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTAx	AOUTBx
0	0	0	0	0	MUTE	MUTE
0	0	0	0	1	MUTE	bR
0	0	0	1	0	MUTE	bL
0	0	0	1	1	MUTE	b[(L+R)/2]
0	0	1	0	0	aR	MUTE
0	0	1	0	1	aR	bR
0	0	1	1	0	aR	bL
0	0	1	1	1	aR	b[(L+R)/2]
0	1	0	0	0	aL	MUTE
0	1	0	0	1	aL	bR
0	1	0	1	0	aL	bL
0	1	0	1	1	aL	b[(L+R)/2]
0	1	1	0	0	a[(L+R)/2]	MUTE
0	1	1	0	1	a[(L+R)/2]	bR
0	1	1	1	0	a[(L+R)/2]	bL
0	1	1	1	1	a[(L+R)/2]	b[(L+R)/2]
1	0	0	0	0	MUTE	MUTE
1	0	0	0	1	MUTE	bR
1	0	0	1	0	MUTE	bL
1	0	0	1	1	MUTE	[(aL+bR)/2]
1	0	1	0	0	aR	MUTE
1	0	1	0	1	aR	bR
1	0	1	1	0	aR	bL
1	0	1	1	1	aR	[(bL+aR)/2]
1	1	0	0	0	aL	MUTE
1	1	0	0	1	aL	bR
1	1	0	1	0	aL	bL
1	1	0	1	1	aL	[(aL+bR)/2]
1	1	1	0	0	[(aL+bR)/2]	MUTE
1	1	1	0	1	[(aL+bR)/2]	bR
1	1	1	1	0	[(bL+aR)/2]	bL
1	1	1	1	1	[(aL+bR)/2]	[(aL+bR)/2]

Table 14. ATAPI Decode

5.15 ADC Left Channel Gain (address 1Ch)

7	6	5	4	3	2	1	0
Reserved	Reserved	LGAIN5	LGAIN4	LGAIN3	LGAIN2	LGAIN1	LGAIN0

5.15.1 ADC LEFT CHANNEL GAIN (LGAINX)

Default = 00h
Function:

The level of the left analog channel can be adjusted in 1dB increments as dictated by the Soft and Zero Cross bits (SZC1:0) from +15 to -15dB. Levels are decoded in two's complement, as shown in Table 15.

5.16 ADC Right Channel Gain (address 1Dh)

7	6	5	4	3	2	1	0
Reserved	Reserved	RGAIN5	RGAIN4	RGAIN3	RGAIN2	RGAIN1	RGAIN0

5.16.1 ADC RIGHT CHANNEL GAIN (RGAINX)

Default = 00h
Function:

The level of the right analog channel can be adjusted in 1dB increments as dictated by the Soft and Zero Cross bits (SZC1:0) from +15 to -15dB. Levels are decoded in two's complement, as shown in Table 15.

Binary Code	Decimal Value	Volume Setting
001111	+15	+15 dB
001010	+10	+10 dB
000101	+5	+5 dB
000000	0	0 dB
111011	-5	-5 dB
110110	-10	-10 dB
110001	-15	-15 dB

Table 15. Example ADC Input Gain Settings

5.17 Receiver Mode Control (address 1Eh)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	INT1	INT0	HOLD1	HOLD0

5.17.1 INTERRUPT PIN CONTROL (INTX)

Default = 00
00 - Active high; high output indicates interrupt condition has occurred
01 - Active low, low output indicates an interrupt condition has occurred
10 - Open drain, active low. Requires an external pull-up resistor on the INT pin.
11 - Reserved
Function:

Determines how the interrupt pin (INT) will indicate an interrupt condition.

5.17.2 AUDIO SAMPLE HOLD (HOLDX)

Default = 00
00 - Hold the last valid audio sample
01 - Replace the current audio sample with 00 (mute)
10 - Do not change the received audio sample
11 - Reserved
Function:

Determines how received audio samples are affected when a receiver error occurs.

5.18 Receiver Mode Control 2 (address 1Fh)

7	6	5	4	3	2	1	0
Reserved	TMUX2	TMUX1	TMUX0	Reserved	RMUX2	RMUX1	RMUX0

5.18.1 TXP MULTIPLEXER (TMUXX)

Default = 000
Function:

Selects which of the eight receiver inputs will be mapped directly to the TXP output pin.

TMUX2	TMUX1	TMUX0	Description
0	0	0	Output from pin RXP0
0	0	1	Output from pin RXP1
0	1	0	Output from pin RXP2
0	1	1	Output from pin RXP3
1	0	0	Output from pin RXP4
1	0	1	Output from pin RXP5
1	1	0	Output from pin RXP6
1	1	1	Output from pin RXP7

Table 16. TXP Output Selection

5.18.2 RECEIVER MULTIPLEXER (RMUXX)

Default = 000
Function:

Selects which of the eight receiver inputs will be mapped to the internal receiver.

RMUX2	RMUX1	RMUX0	Description
0	0	0	Input from pin RXP0
0	0	1	Input from pin RXP1
0	1	0	Input from pin RXP2
0	1	1	Input from pin RXP3
1	0	0	Input from pin RXP4
1	0	1	Input from pin RXP5
1	1	0	Input from pin RXP6
1	1	1	Input from pin RXP7

Table 17. Receiver Input Selection

5.19 Interrupt Status (address 20h) (Read Only)

7	6	5	4	3	2	1	0
UNLOCK	Reserved	QCH	DETC	DETU	Reserved	OverFlow	RERR

For all bits in this register, a “1” means the associated interrupt condition has occurred at least once since the register was last read. A ”0” means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0. Status bits that are masked off in the associated mask register will always be “0” in this register.

5.19.1 PLL UNLOCK (UNLOCK)

Default = 0
Function:

PLL unlock status bit. This bit will go high if the PLL becomes unlocked.

5.19.2 NEW Q-SUBCODE BLOCK (QCH)

Default = 0
Function:

Indicates when the Q-Subcode block has changed.

5.19.3 D TO E C-BUFFER TRANSFER (DETC)

Default = 0
Function:

Indicates when the channel status buffer has changed.

5.19.4 D TO E U-BUFFER TRANSFER (DETU)

Default = 0
Function:

Indicates when the user status buffer has changed.

5.19.5 ADC OVERFLOW (OVERFLOW)

Default = 0
Function:

Indicates that there is an over-range condition anywhere in the CS42516 ADC signal path.

5.19.6 RECEIVER ERROR (RERR)

Default = 0
Function:

Indicates that a receiver error has occurred. The register “Receiver Errors (address 26h) (Read Only)” on page 55 may be read to determine the nature of the error which caused the interrupt.

5.20 Interrupt Mask (address 21h)

7	6	5	4	3	2	1	0
UNLOCKM	Reserved	QCHM	DETCM	DETUM	Reserved	OverFlowM	RERRM

Default = 00000000
Function:

The bits of this register serve as a mask for the interrupt sources found in the register “Interrupt Status (address 20h) (Read Only)” on page 52. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in the Interrupt Status register.

5.21 Interrupt Mode MSB (address 22h) Interrupt Mode LSB (address 23h)

7	6	5	4	3	2	1	0
UNLOCK1	Reserved	QCH1	DETC1	DETU1	Reserved	OF1	RERR1
UNLOCK0	Reserved	QCH0	DETC0	DETU0	Reserved	OF0	RERR0

Default = 00000000
Function:

The two Interrupt Mode registers form a 2-bit code for each Interrupt Status register function. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT interrupt pin becomes active during the interrupt condition. Be aware that the active level(Active High or Low) only depends on the INT(1:0) bits located in the register “Receiver Mode Control (address 1Eh)” on page 50.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

5.22 Channel Status Data Buffer Control (address 24h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	BSEL	CAM	CHS

5.22.1 DATA SELECT (BSEL)

Default = 0
0 - Data buffer address space contains Channel Status data
1 - Data buffer address space contains User data
Function:

Selects the data buffer register addresses to contain either User data or Channel Status data.

5.22.2 C-DATA BUFFER CONTROL (CAM)

Default = 0
0 - One byte mode
1 - Two byte mode
Function:

Sets the C-data buffer control port access mode.

5.22.3 CHANNEL SELECT (CHS)

Default = 0
Function:

When set to ‘0’, channel A information is displayed in the receiver channel status register. Channel A information is output during control port reads when CAM is set to ‘0’ (one byte mode).

When set to ‘1’, channel B information is displayed in the receiver channel status register. Channel B information is output during control port reads when CAM is set to ‘0’ (one byte mode).

5.23 Receiver Channel Status (address 25h) (Read Only)

7	6	5	4	3	2	1	0
AUX3	AUX2	AUX1	AUX0	PRO	$\overline{\text{AUDIO}}$	COPY	ORIG

The bits in this register can be associated with either channel A or B of the received data. The desired channel is selected with the CHS bit of the Channel Status Data Buffer Control register.

5.23.1 AUXILIARY DATA WIDTH (AUXX)

Default = xxxx
Function:

Selects the incoming auxiliary data field width, as indicated by the incoming channel status bits, decoded according to IEC60958.

AUX3	AUX2	AUX1	AUX0	Description
0	0	0	0	Auxiliary data is not present
0	0	0	1	Auxiliary data is 1 bit long
0	0	1	0	Auxiliary data is 2 bit long
0	0	1	1	Auxiliary data is 3 bit long
0	1	0	0	Auxiliary data is 4 bit long
0	1	0	1	Auxiliary data is 5 bit long
0	1	1	0	Auxiliary data is 6 bit long
0	1	1	1	Auxiliary data is 7 bit long
1	0	0	0	Auxiliary data is 8 bit long
1	0	0	1	1001 - 1111 is Reserved

Table 18. Auxiliary Data Width Selection

5.23.2 CHANNEL STATUS BLOCK FORMAT (PRO)

Default = x
Function:

Indicates the channel status block format.

5.23.3 AUDIO INDICATOR ($\overline{\text{AUDIO}}$)

Default = x
Function:

A ‘0’ indicates that the received data is linearly coded PCM audio. A ‘1’ indicates that the received data is not linearly coded PCM audio.

5.23.4 SCMS COPYRIGHT (COPY)

Default = x
Function:

A ‘0’ indicates that copyright is not asserted, while a ‘1’ indicates that copyright is asserted. If the category code is set to General in the incoming S/PDIF digital stream, copyright will always be indicated by COPY, even when the stream indicates no copyright.

5.23.5 SCMS GENERATION (ORIG)

Default = x
Function:

A ‘0’ indicates that the received data is 1st generation or higher. A ‘1’ indicates that the received data is original. COPY and ORIG will both be set to ‘1’ if the incoming data is flagged as professional, or if the receiver is not in use.

5.24 Receiver Errors (address 26h) (Read Only)

7	6	5	4	3	2	1	0
Reserved	QCRC	CCRC	UNLOCK	V	CONF	BIP	PAR

5.24.1 CRC ERROR (QCRC)

Default = x
0 - No error
1 - Error
Function:

Indicates a Q-subcode data CRC error. This bit is updated on Q-subcode block boundaries.

5.24.2 REDUNDANCY CHECK (CCRC)

Default = x
0 - No error
1 - Error
Function:

Indicates a channel status block cyclic redundancy. This bit is updated on CS block boundaries, valid in Professional mode.

5.24.3 PLL LOCK STATUS (UNLOCK)

Default = x
0 - PLL locked
1 - PLL out of lock
Function:

Indicates the lock status of the PLL.

5.24.4 RECEIVED VALIDITY (V)

Default = x
0 - Data is valid and is normally linear coded PCM audio
1 - Data is invalid, or may be valid compressed audio
Function:

Indicates the received validity status. This bit is updated on sub-frame boundaries.

5.24.5 RECEIVED CONFIDENCE (CONF)

Default = x
0 - No error
1 - Confidence error. This indicates that the received data eye opening is less than half a bit period, indicating a poor link that is not meeting specifications.
Function:

Indicates the received confidence status. This bit is updated on sub-frame boundaries.

5.24.6 BI-PHASE ERROR (BIP)

Default = x
0 - No error
1 - Bi-phase error. This indicates an error in the received bi-phase coding.
Function:

Indicates a bi-phase coding error. This bit is updated on sub-frame boundaries.

5.24.7 PARITY STATUS (PAR)

Default = x
0 - No error
1 - Parity Error
Function:

Indicates the Parity status. This bit is updated on sub-frame boundaries.

5.25 Receiver Errors Mask (address 27h)

7	6	5	4	3	2	1	0
Reserved	QCRCM	CCRCM	UNLOCKM	VM	CONFM	BIPM	PARM

Default = 00000000
Function:

The bits in this register serve as masks for the corresponding bits of the Receiver Errors register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will appear in the receiver errors register, will affect the RERR interrupt, and will affect the current audio sample according to the status of the HOLD bit. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not appear in the receiver error register, will not affect the RERR interrupt, and will not affect the current audio sample. The CCRC and QCRC bits behave differently from the other bits: they do not affect the current audio sample even when unmasked.

5.26 MuteC Pin Control (address 28h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Polarity	M_AOUTA1	M_AOUTB1	M_AOUTA2 M_AOUTB2	M_AOUTA3 M_AOUTB3	Reserved

5.26.1 POLARITY SELECT (POLARITY)

Default = 0
0 - Active low
1 - Active high
Function:

Determines the polarity of the MUTEC pin.

5.26.2 CHANNEL MUTES SELECT (M_AOUTXX)

Default = 1111
0 - Channel mute is not mapped to the MUTEC pin
1 - Channel mute is mapped to the MUTEC pin
Function:

Determines which channel mutes will be mapped to the MUTEC pin. If no channel mute bits are mapped, then the MUTEC pin is driven to the "active" state as defined by the POLARITY bit. These Channel Mute Select bits are "ANDed" together in order for the MUTEC pin to go active. This means that if multiple Channel Mutes are selected to be mapped to the MUTEC pin, then all corresponding channels must be muted before the MUTEC will go active.

5.27 RXP/General Purpose Pin Control (addresses 29h to 2Fh)

7	6	5	4	3	2	1	0
Mode1	Mode0	Polarity	Function4	Function3	Function2	Function1	Function0

5.27.1 MODE CONTROL (MODEX)

Default = 00
00 - RXP Input
01 - Mute Output Mode
1X - GPO Output Mode
Function:

<u>RXP Input</u> - The pin is configured as a receiver input which can then be muxed to either the TXP pin or to the internal receiver.

<u>Mute Output Mode</u> - The pin is configured as a dedicated mute pin. The muting function is controlled by the Function bits.

<u>GPO Output Mode</u> - The pin is configured as a general purpose output. In this mode, bit 6 will determine whether the pin is driven high or low.

5.27.2 POLARITY SELECT (POLARITY)

Default = 0
Function:

RXP Input - If the pin is configured for an RXP input, the polarity bit is ignored. It is recommended that in this mode this bit be set to 0.

Mute Output Mode - If the pin is configured as a dedicated mute output pin, then the polarity bit determines the polarity of the mapped pin according to the following

0 - Active low
1 - Active high

GPO Output Mode - If the pin is configured as a general purpose output, the polarity bit is ignored. It is recommended that in this mode this bit be set to 0.

5.27.3 FUNCTIONAL CONTROL (FUNCTIONX)

Default = 00000
Function:

RXP Input - If the pin is configured for an RXP input, the functional bits are ignored. It is recommended that in this mode all the functional bits be set to 0.

Mute Output Mode - If the pin is configured as a dedicated mute pin, then the functional bits determine which channel mutes will be mapped to this pin according to the following

0 - Channel mute is not mapped to the RXPx/GPOx pin
1 - Channel mute is mapped to the RXPx/GPOx pin
:

RXPx/GPOx	Reg Address	Function4	Function3	Function2	Function1	Function0
RXP7/GPO7 pin 42	29h	M_AOUTA1	M_AOUTB1	M_AOUTA2 M_AOUTB2	M_AOUTA3 M_AOUTB3	Reserved
RXP6/GPO6 pin 43	2Ah	M_AOUTA1 M_AOUTB1	M_AOUTA2	M_AOUTB2	M_AOUTA3 M_AOUTB3	Reserved
RXP5/GPO5 pin 44	2Bh	M_AOUTA1 M_AOUTB1	M_AOUTA2	M_AOUTB2	M_AOUTA3 M_AOUTB3	Reserved
RXP4/GPO4 pin 45	2Ch	M_AOUTA1 M_AOUTB1	M_AOUTA2 M_AOUTB2	M_AOUTA3	M_AOUTB3	Reserved
RXP3/GPO3 pin 46	2Dh	M_AOUTA1 M_AOUTB1	M_AOUTA2 M_AOUTB2	M_AOUTA3	M_AOUTB3	Reserved
RXP2/GPO2 pin 47	2Eh	M_AOUTA1 M_AOUTB1	M_AOUTA2 M_AOUTB2	M_AOUTA3 M_AOUTB3	Reserved	Reserved
RXP1/GPO1 pin 48	2Fh	M_AOUTA1 M_AOUTB1	M_AOUTA2 M_AOUTB2	M_AOUTA3 M_AOUTB3	Reserved	Reserved

GPO Output Mode - If the pin is configured as a general purpose output, then the functional bits are ignored, while bit 6 determines whether the pin is driven high or low. It is recommended that in this mode all the functional bits be set to 0.

5.28 Q-Channel Subcode Bytes 0 to 9 (addresses 30h to 39h) (Read Only)

7	6	5	4	3	2	1	0
Address3	Address2	Address1	Address0	Control3	Control2	Control1	Control0
Track7	Track6	Track5	Track4	Track3	Track2	Track1	Track0
Index7	Index6	Index5	Index4	Index3	Index2	Index1	Index0
Minute7	Minute6	Minute5	Minute4	Minute3	Minute2	Minute1	Minute0
Second7	Second6	Second5	Second4	Second3	Second2	Second1	Second0
Frame7	Frame6	Frame5	Frame4	Frame3	Frame2	Frame1	Frame0
Zero7	Zero6	Zero5	Zero4	Zero3	Zero2	Zero1	Zero0
A.Minute7	A.Minute6	A.Minute5	A.Minute4	A.Minute3	A.Minute2	A.Minute1	A.Minute0
A.Second7	A.Second6	A.Second5	A.Second4	A.Second3	A.Second2	A.Second1	A.Second0
A.Frame7	A.Frame6	A.Frame5	A.Frame4	A.Frame3	A.Frame2	A.Frame1	A.Frame0

These ten registers contain the decoded Q-channel subcode data.

5.29 C-bit or U-bit Data Buffer (addresses 3Ah to 51h) (Read Only)

7	6	5	4	3	2	1	0
CU Buffer7	CU Buffer6	CU Buffer5	CU Buffer4	CU Buffer3	CU Buffer2	CU Buffer1	CU Buffer0

Either channel status data buffer E or user data buffer E is accessible through these register addresses.

6 CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25 °C.)

SPECIFIED OPERATING CONDITIONS (T_A = 25 °C; AGND=DGND=0, all voltages with respect to ground; OMCK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supply	Analog power	VA / VARX	4.75	5.0	5.25	V
	Digital internal power	VD	3.13	3.3	5.25	V
	Serial data port interface power	VLS	1.8	5.0	5.25	V
	Control port interface power	VLC	1.8	5.0	5.25	V
Ambient Operating Temperature (power applied)	CS42516-CQ	T_A	-10	-	+70	°C
	CS42516-IQ		-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS (AGND = DGND = 0V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog power	VA / VARX	-0.3	6.0	V
	Digital internal power	VD	-0.3	6.0	V
	Serial data port interface power	VLS	-0.3	6.0	V
	Control port interface power	VLC	-0.3	6.0	V
Input Current	(Note 1)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 2)	V_{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage	Serial data port interface	V_{IND-S}	-0.3	VLS+ 0.4	V
(Note 2)	Control port interface	V_{IND-C}	-0.3	VLC+ 0.4	V
	S/PDIF interface	V_{IND-SP}	-0.3	VARX+0.4	V
Ambient Operating Temperature(power applied)					
	CS42516-CQ	T_A	-20	+85	°C
	CS42516-IQ	T_A	-50	+95	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

2. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (T_A = 25° C; VA =VARX= 5 V, VD = 3.3 V, Logic "0" = DGND =AGND = 0 V; Logic "1" = VLS = VLC = 5V; Measurement Bandwidth 10 Hz to 20 kHz unless otherwise specified. Full scale input sine wave, 997Hz.; OMCK = 12.288 MHz; Single speed Mode CX_SCLK = 3.072 MHz; Double Speed Mode CX_SCLK = 6.144 MHz; Quad Speed Mode CX_SCLK = 12.288.)

Parameter (Note 3)		Symbol	CS42516-CQ Min	CS42516-CQ Typ	CS42516-CQ Max	CS42516-IQ Min	CS42516-IQ Typ	CS42516-IQ Max	Unit
Single Speed Mode (Fs=48kHz)									
Dynamic Range	A-weighted		108	114	-	106	114	-	dB
	unweighted		105	111	-	103	111	-	dB
Total Harmonic Distortion + Noise		THD+N							
(Note 4)	-1 dB		-	-105	-99	-	-105	-97	dB
	-20 dB		-	-91	-	-	-91	-	dB
	-60 dB		-	-51	-	-	-51	-	dB
Double Speed Mode (Fs=96kHz)									
Dynamic Range	A-weighted		108	114	-	106	114	-	dB
	unweighted		105	111	-	103	111	-	dB
	40kHz bandwidth unweighted		-	108	-	-	108	-	dB
Total Harmonic Distortion + Noise		THD+N							
(Note 4)	-1 dB		-	-105	-99	-	-105	-97	dB
	-20 dB		-	-91	-	-	-91	-	dB
	-60 dB		-	-51	-	-	-51	-	dB
40kHz bandwidth	-1 dB		-	-97	-	-	-97	-	dB
Quad Speed Mode (Fs=192kHz)									
Dynamic Range	A-weighted		108	114	-	106	114	-	dB
	unweighted		105	111	-	103	111	-	dB
	40kHz bandwidth unweighted		-	108	-	-	108	-	dB
Total Harmonic Distortion + Noise		THD+N							
(Note 4)	-1 dB		-	-105	-99	-	-105	-97	dB
	-20 dB		-	-91	-	-	-91	-	dB
	-60 dB		-	-51	-	-	-51	-	dB
40kHz bandwidth	-1 dB		-	-97	-	-	-97	-	dB
Dynamic Performance for All Modes									
Interchannel Isolation			-	110	-	-	110	-	dB
Interchannel Phase Deviation			-	0.0001	-	-	0.0001	-	Degree
DC Accuracy									
Interchannel Gain Mismatch			-	0.1	-	-	0.1	-	dB
Gain Drift			-	+/-100	-	-	+/-100	-	ppm/°C
Offset Error	HPF_FREEZE enabled		-	0	-	-	0	-	LSB
	HPF_FREEZE disabled		-	100	-	-	100	-	LSB
Analog Input									
Full-scale Differential Input Voltage			1.9	2.0	2.1	1.8	2.0	2.2	Vrms
Input Impedance(differential) (Note 5)			37	-	-	37	-	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	-	82	-	dB
VQ Nominal Voltage			-	2.5	-	-	2.5	-	V
Output Impedance			-	50	-	-	50	-	kΩ
Maximum allowable DC current			-	0.01	-	-	0.01	-	mA

FILT+ Nominal Voltage		-	5.0	-	-	5.0	-	V
Output Impedance		-	35	-	-	35	-	kΩ
Maximum allowable DC current		-	0.01	-	-	0.01	-	mA

Notes: 3. Typical performance numbers are taken at 25 °C. Min/Max performance numbers are guaranteed across the specified temperature range, T_A.

4. Referred to the typical full-scale voltage.

5. Measured between AIN+ and AIN-

A/D DIGITAL FILTER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Single Speed Mode (2 to 50 kHz sample rates)					
Passband (-0.1 dB) (Note 6)		0	-	0.47	Fs
Passband Ripple		-	-	±0.035	dB
Stopband (Note 6)		0.58	-	-	Fs
Stopband Attenuation		-95	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	µs
Double Speed Mode (50 to 100 kHz sample rates)					
Passband (-0.1 dB) (Note 6)		0	-	0.45	Fs
Passband Ripple		-	-	±0.035	dB
Stopband (Note 6)		0.68	-	-	Fs
Stopband Attenuation		-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	µs
Quad Speed Mode (100 to 192 kHz sample rates)					
Passband (-0.1 dB) (Note 6)		0	-	0.24	Fs
Passband Ripple		-	-	±0.035	dB
Stopband (Note 6)		0.78	-	-	Fs
Stopband Attenuation		-97	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	µs
High Pass Filter Characteristics					
Frequency Response -3.0 dB		-	1	-	Hz
-0.13 dB (Note 7)			20	-	Hz
Phase Deviation @ 20Hz (Note 7)		-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Setting Time		-	10^5/Fs	-	s

Notes: 6. The filter frequency response scales precisely with Fs.

7. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

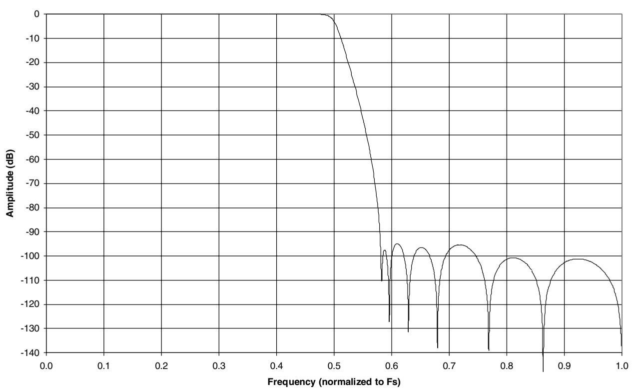


Figure 20. Single Speed Mode Stopband Rejection

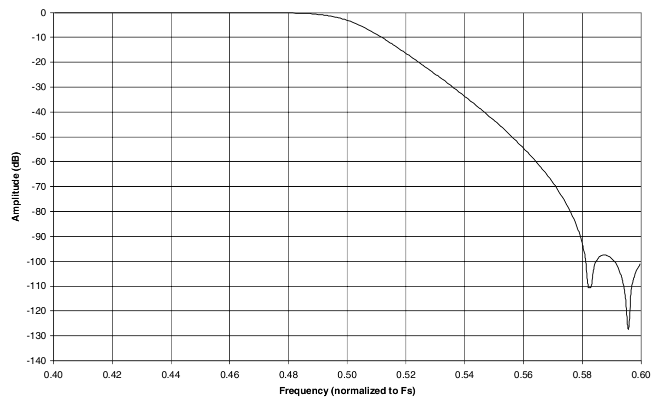


Figure 21. Single Speed Mode Transition Band

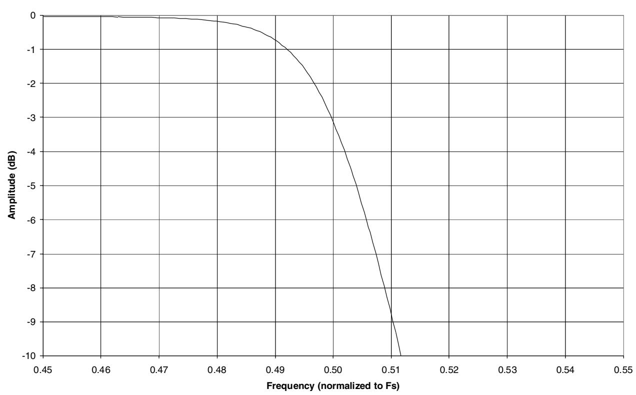


Figure 22. Single Speed Mode Transition Band (Detail)

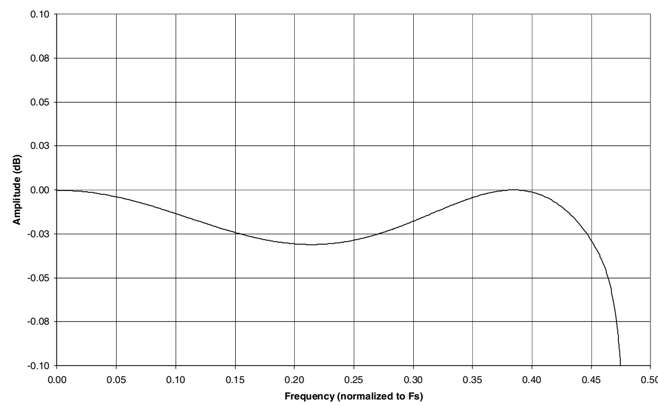


Figure 23. Single Speed Mode Passband Ripple

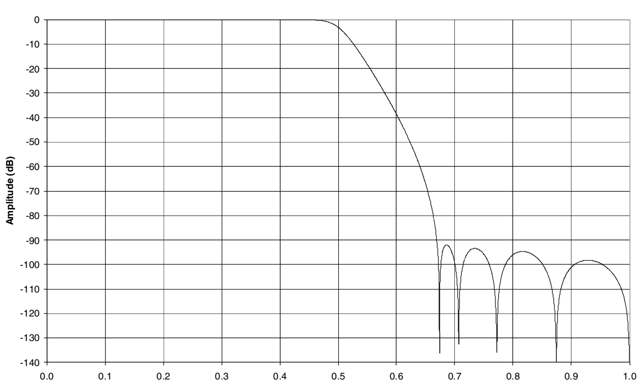


Figure 24. Double Speed Mode Stopband Rejection

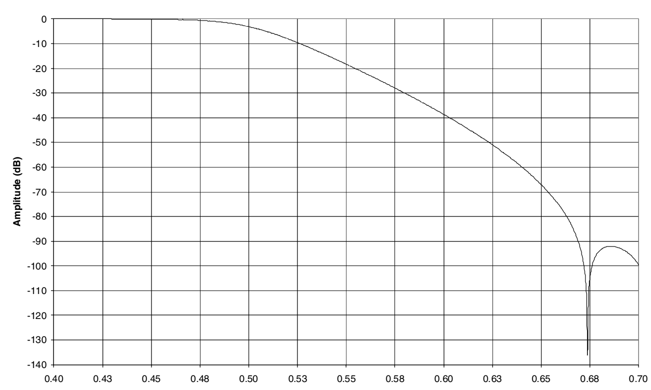


Figure 25. Double Speed Mode Transition Band

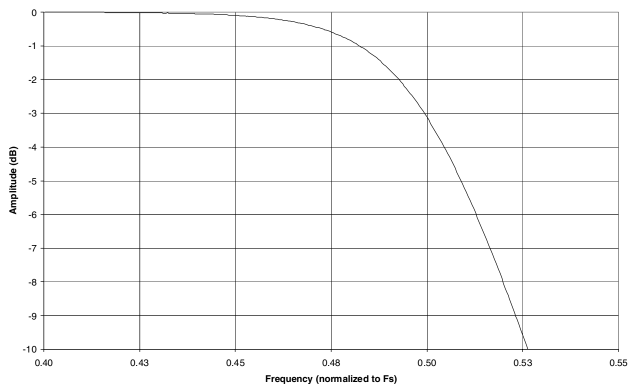


Figure 32. Double Speed Mode Transition Band (Detail)

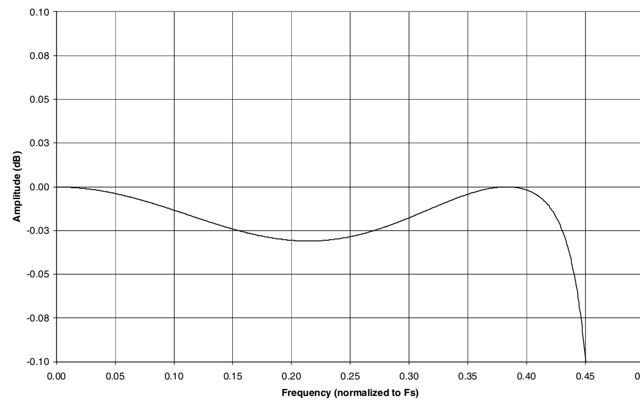


Figure 33. Double Speed Mode Passband Ripple

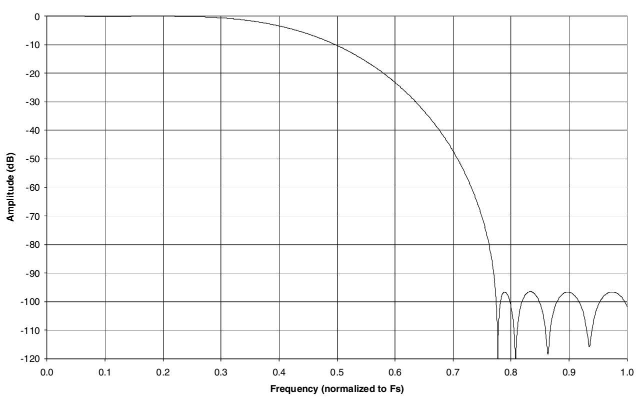


Figure 34. Quad Speed Mode Stopband Rejection

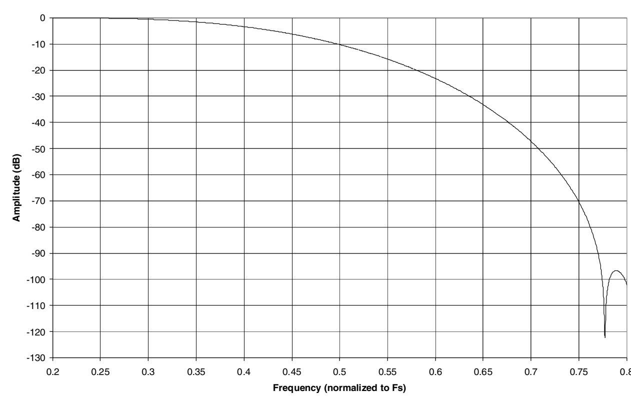


Figure 35. Quad Speed Mode Transition Band

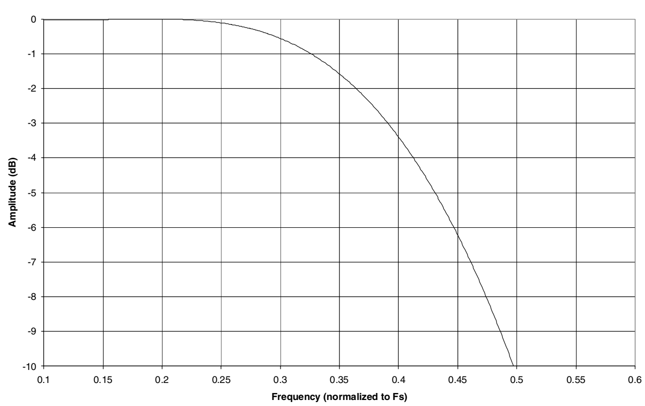


Figure 36. Quad Speed Mode Transition Band (Detail)

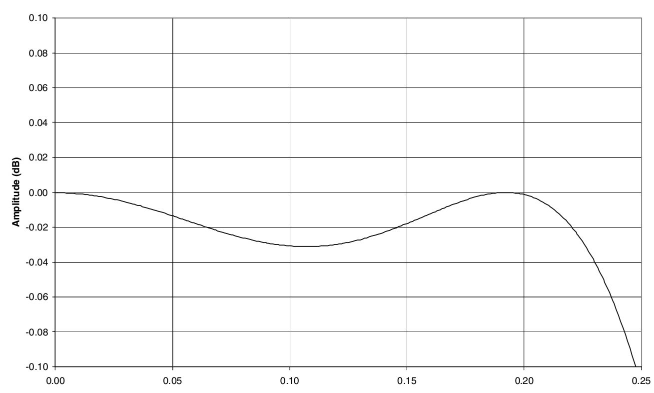


Figure 37. Quad Speed Mode Passband Ripple

ANALOG OUTPUT CHARACTERISTICS (T_A = 25° C; VA =VARX= 5 V, VD = 3.3 V, Logic "0" = DGND =AGND = 0 V; Logic "1" = VLS = VLC = 5V; Measurement Bandwidth 10 Hz to 20 kHz unless otherwise specified.; Full scale output 997 Hz sine wave, Test load R_L = 3 kΩ, C_L = 30 pF; OMCK = 12.288 MHz; Single speed Mode, CX_SCLK = 3.072 MHz; Double Speed Mode, CX_SCLK = 6.144 MHz; Quad Speed Mode, CX_SCLK = 12.288 MHz.)

Parameter	Symbol	CS42516-CQ Min	CS42516-CQ Typ	CS42516-CQ Max	CS42516-IQ Min	CS42516-IQ Typ	CS42516-IQ Max	Unit
Dynamic performance for all modes								
Dynamic Range(Note 8)								
24-bit A-weighted		104	110	-	104	110	-	dB
unweighted		101	107	-	101	107	-	dB
16-bit A-Weighted		-	97	-	-	97	-	dB
(Note 9) unweighted		-	94	-	-	94	-	dB
Total Harmonic Distortion + Noise	THD+N							
24-bit 0 dB		-	-100	-94	-	-100	-94	dB
-20 dB		-	-91	-	-	-91	-	dB
-60 dB		-	-51	-	-	-51	-	dB
16-bit 0 dB		-	-94	-	-	-94	-	dB
(Note 9) -20 dB		-	-74	-	-	-74	-	dB
-60 dB		-	-34		-	-34	-	dB
Idle Channel Noise/Signal-to-noise ratio		-	110	-	-	110	-	dB
Interchannel Isolation (1kHz)		-	90	-	-	90	-	dB
Analog Output Characteristics for all modes								
Full Scale Differential Output		.88VA	.92VA	.94VA	.88VA	.92VA	.94VA	Vpp
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	100	-	-	100	-	ppm/°C
Output Impedance	Z_{OUT}	-	100	-	-	100	-	Ω
AC-Load Resistance	R_L	3	-	-	3	-	-	kΩ
Load Capacitance	C_L	-	-	30	-	-	30	pF

Notes: 8. One-half LSB of triangular PDF dither is added to data.

9. Performance limited by 16-bit quantization noise.

D/A DIGITAL FILTER CHARACTERISTICS

Parameter		Fast Roll-Off			Slow Roll-Off		Unit
		Min	Typ	Max	Min	Typ	Max	
Combined Digital and On-chip Analog Filter Response - Single Speed Mode - 48kHz (Note 10)								
Passband (Note 11)	to -0.01 dB corner	0	-	.4535	0	-	0.4166	Fs
	to -3 dB corner	0	-	.4998	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	-0.01	-	+0.01	dB
StopBand		.5465	-	-	.5834	-	-	Fs
StopBand Attenuation	(Note 12)	90	-	-	64	-	-	dB
Group Delay		-	12/Fs	-	-	6.5/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.41/Fs		-	±0.14/Fs	s
De-emphasis Error (Note 13)	Fs = 32 kHz	-	-	±0.23	-	-	±0.23	dB
(Relative to 1kHz)	Fs = 44.1 kHz	-	-	±0.14	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	-	-	±0.09	dB
Combined Digital and On-chip Analog Filter Response - Double Speed Mode - 96kHz (Note 10)								
Passband (Note 11)	to -0.01 dB corner	0	-	.4166	0	-	.2083	Fs
	to -3 dB corner	0	-	.4998	0	-	.4998	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	-0.01	-	0.01	dB
StopBand		.5834	-	-	.7917	-	-	Fs
StopBand Attenuation	(Note 12)	80	-	-	70	-	-	dB
Group Delay		-	4.6/Fs	-	-	3.9/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.03/Fs		-	±0.01/Fs	s
Combined Digital and On-chip Analog Filter Response - Quad Speed Mode - 192kHz (Note 10)								
Passband (Note 11)	to -0.01 dB corner	0	-	.1046	0	-	.1042	Fs
	to -3 dB corner	0	-	.4897	0	-	.4813	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	-0.01	-	0.01	dB
StopBand		.6355	-	-	.8683	-	-	Fs
StopBand Attenuation	(Note 12)	90	-	-	75	-	-	dB
Group Delay		-	4.7/Fs	-	-	4.2/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	-	±0.01/Fs		-	±0.01/Fs	s

Notes: 10. Filter response is not tested but is guaranteed by design.

11. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 38 to 61) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

12. Single and Double Speed Mode Measurement Bandwidth is from stopband to 3 Fs.
Quad Speed Mode Measurement Bandwidth is from stopband to 1.34 Fs.

13. De-emphasis is available only in Single Speed Mode.

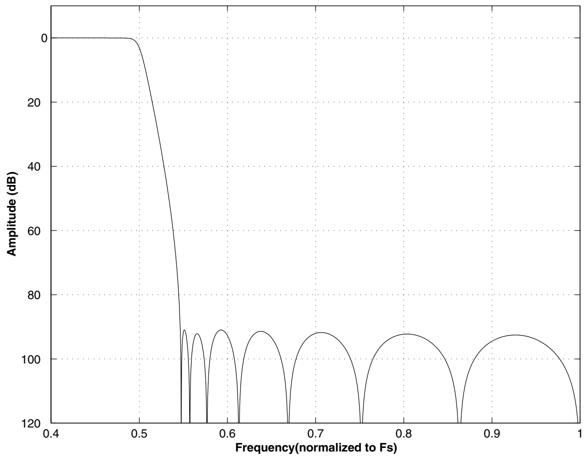


Figure 38. Single Speed (fast) Stopband Rejection

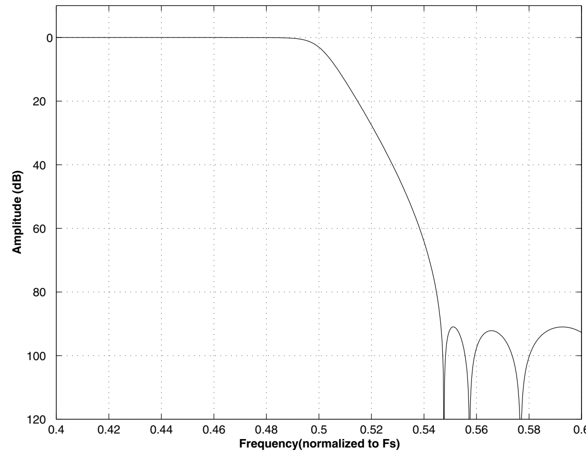


Figure 39. Single Speed (fast) Transition Band

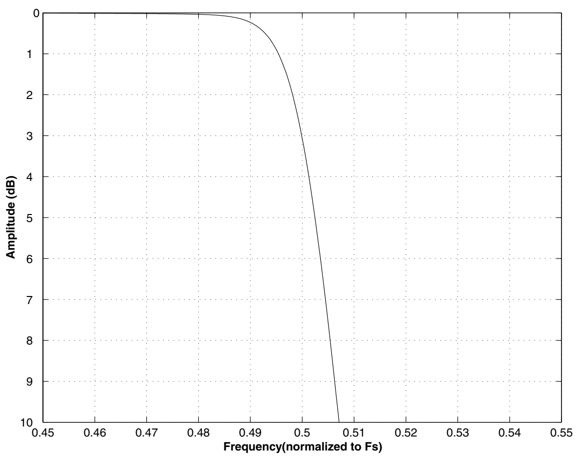


Figure 40. Single Speed (fast) Transition Band (detail)

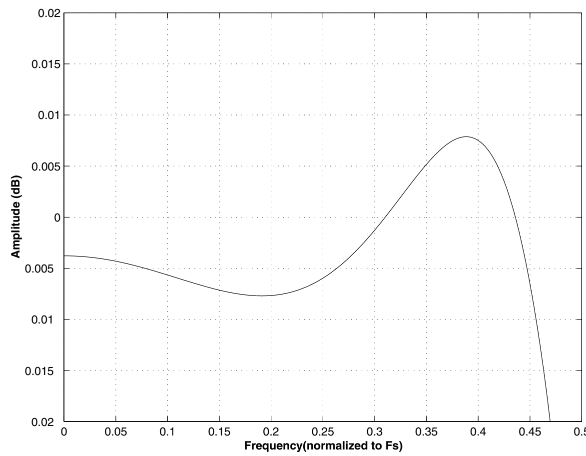


Figure 41. Single Speed (fast) Passband Ripple

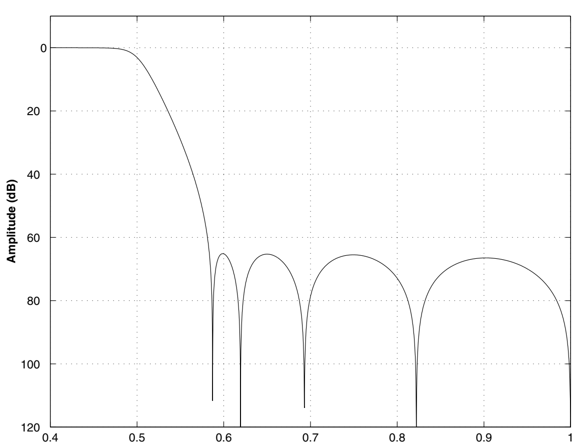


Figure 42. Single Speed (slow) Stopband Rejection

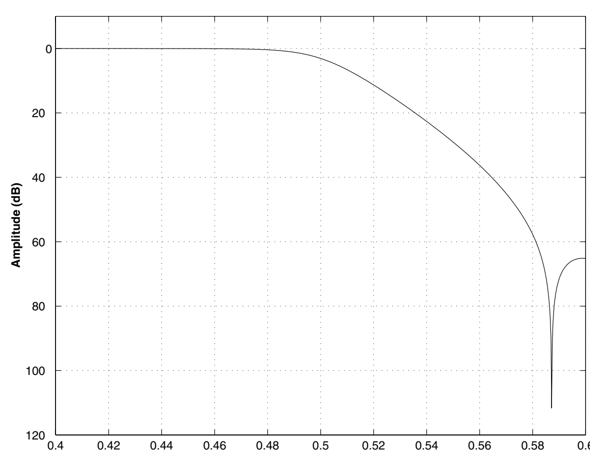


Figure 43. Single Speed (slow) Transition Band

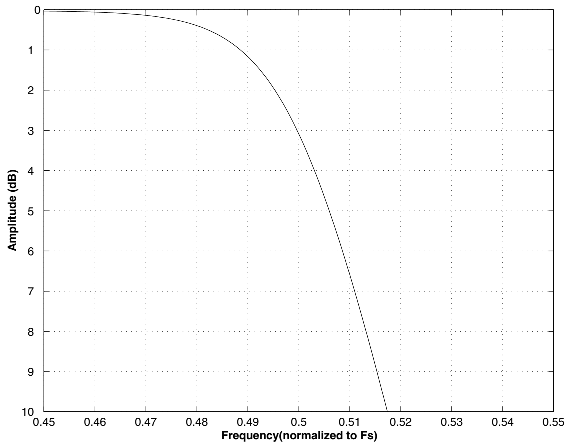


Figure 44. Single Speed (slow) Transition Band (detail)

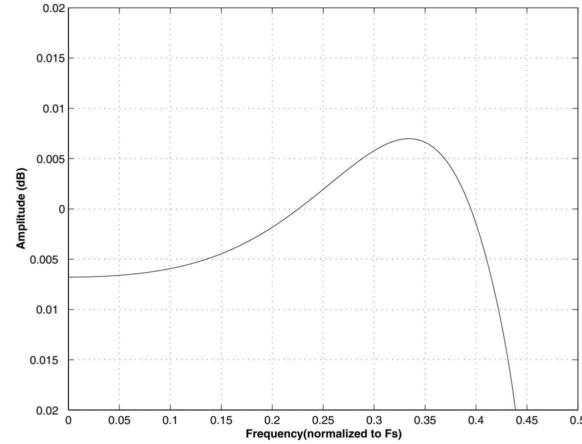


Figure 45. Single Speed (slow) Passband Ripple

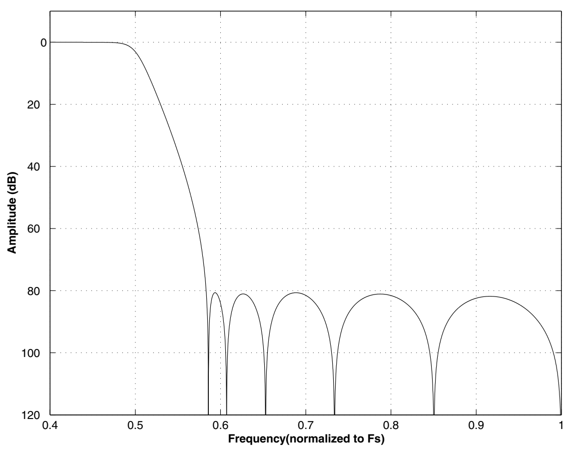


Figure 46. Double Speed (fast) Stopband Rejection

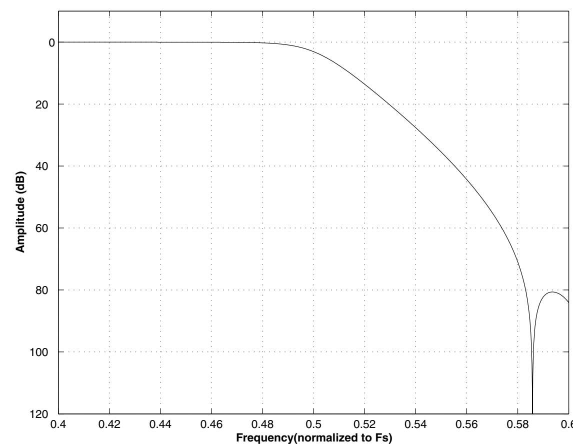


Figure 47. Double Speed (fast) Transition Band

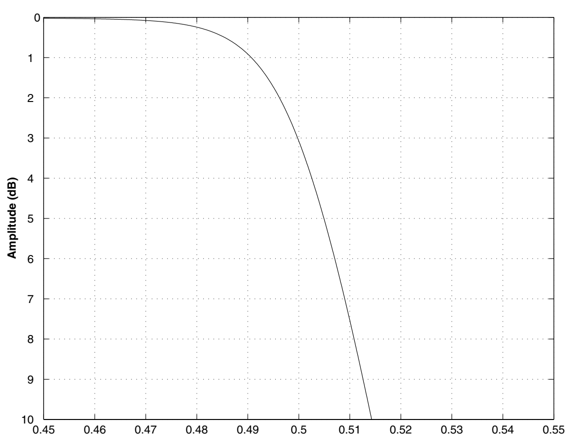


Figure 48. Double Speed (fast) Transition Band (detail)

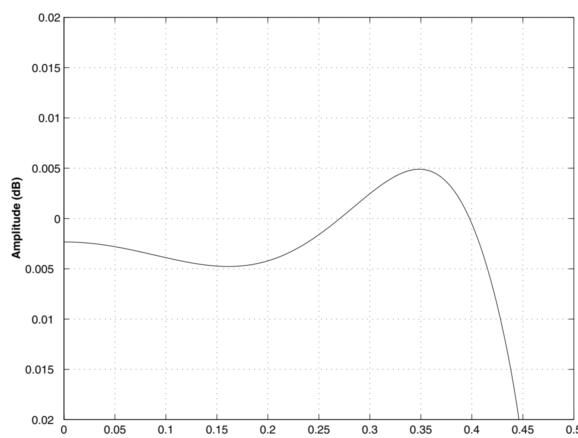


Figure 49. Double Speed (fast) Passband Ripple

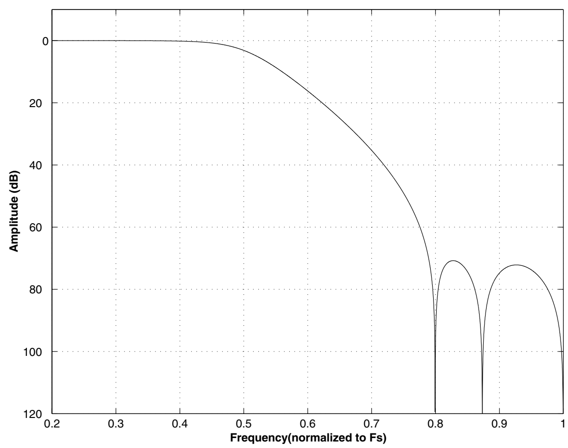


Figure 50. Double Speed (slow) Stopband Rejection

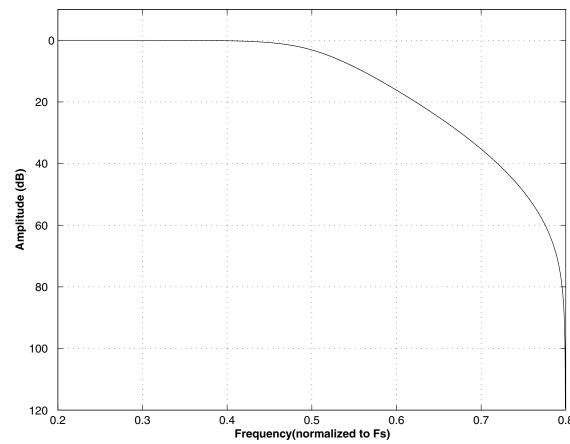


Figure 51. Double Speed (slow) Transition Band

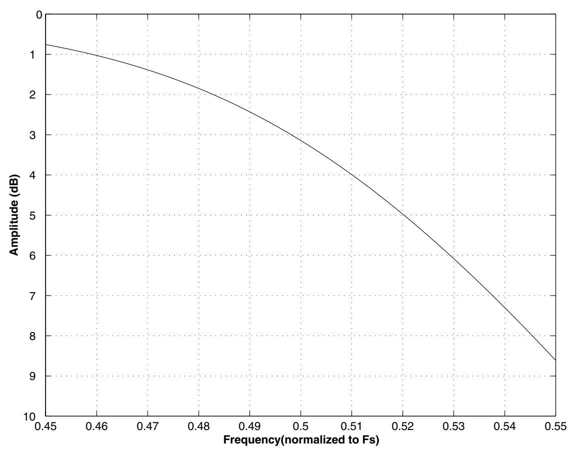


Figure 52. Double Speed (slow) Transition Band (detail)

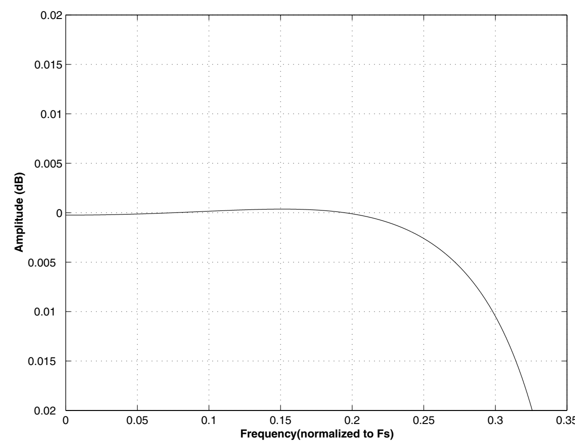


Figure 53. Double Speed (slow) Passband Ripple

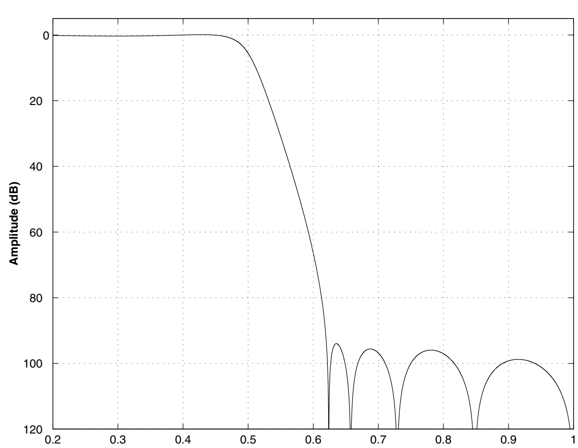


Figure 54. Quad Speed (fast) Stopband Rejection

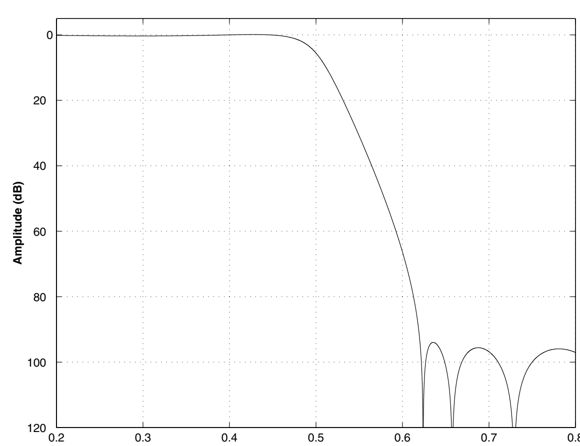


Figure 55. Quad Speed (fast) Transition Band

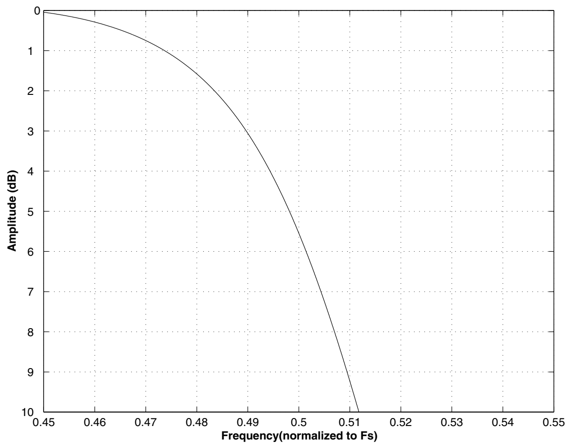


Figure 56. Quad Speed (fast) Transition Band (detail)

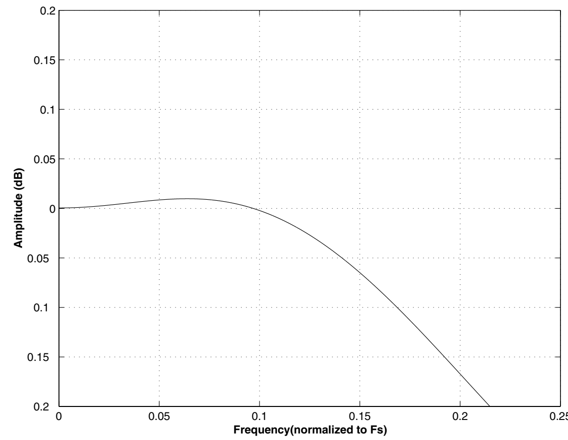


Figure 57. Quad Speed (fast) Passband Ripple

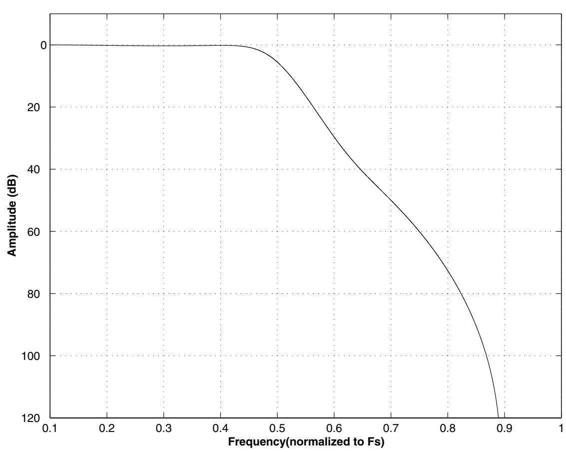


Figure 58. Quad Speed (slow) Stopband Rejection

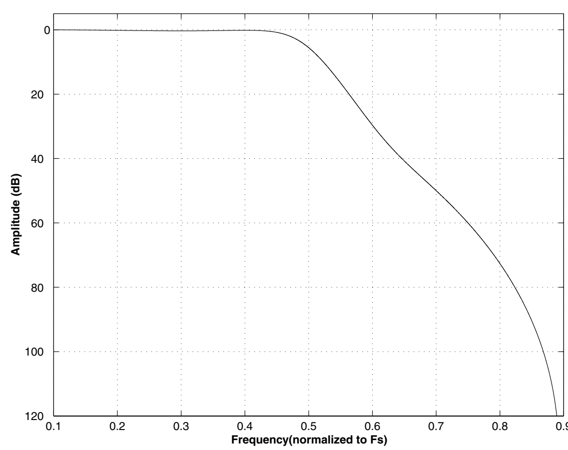


Figure 59. Quad Speed (slow) Transition Band

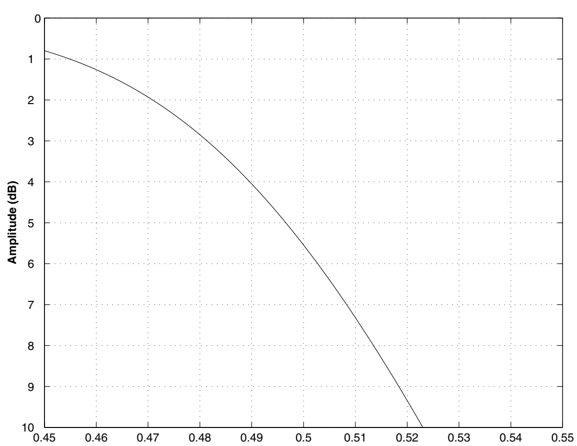


Figure 60. Quad Speed (slow) Transition Band (detail)

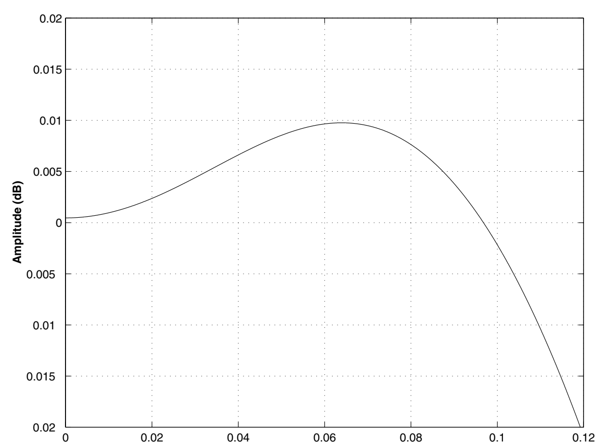


Figure 61. Quad Speed (slow) Passband Ripple

SWITCHING CHARACTERISTICS (For CQ, T_A = -10 to +70 °C; For IQ, T_A = -40 to +85 °C; VA=VARX = 5V, VD =VLC= 3.3V, VLS = 1.8 V to 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VLS, C_L = 30pF)

Parameters	Symbol	Min	Typ	Max	Units
RST pin Low Pulse Width (Note 14)		1	-	-	ms
PLL Clock Recovery Sample Rate Range		30	-	200	kHz
RMCK output jitter (Note 16)		-	200	-	ps RMS
RMCK output duty cycle		45	50	55	%
OMCK Duty Cycle (Note 15)		40	50	60	%
CX_SCLK, SAI_SCLK Duty Cycle		45	50	55	%
CX_LRCK, SAI_LRCK Duty Cycle		45	50	55	%
Master Mode					
RMCK to CX_SCLK, SAI_SCLK active edge delay	t_{smd}	0	-	10	ns
RMCK to CX_LRCK, SAI_LRCK delay	t_{lmd}	0	-	10	ns
Slave Mode					
CX_SCLK, SAI_SCLK Falling Edge to CX_SDOUT, SAI_SDOUT Output Valid	t_{dpd}		-	50	ns
CX_LRCK, SAI_LRCK Edge to MSB Valid	t_{lrpd}		-	20	ns
CX_SDIN Setup Time Before CX_SCLK Rising Edge	t_{ds}		-	10	ns
CX_SDIN Hold Time After CX_SCLK Rising Edge	t_{dh}		-	30	ns
CX_SCLK, SAI_SCLK High Time	t_{sckh}	20	-	-	ns
CX_SCLK, SAI_SCLK Low Time	t_{sckl}	20	-	-	ns
CX_SCLK, SAI_SCLK rising to CX_LRCK, SAI_LRCK Edge	t_{lrckd}	25	-	-	ns
CX_LRCK, SAI_LRCK Edge to CX_SCLK, SAI_SCLK Rising	t_{lrcks}	25	-	-	ns

Notes: 14. After powering up the CS42516, $\overline{\text{RST}}$ should be held low after the power supplies and clocks are settled.

15. See Table 3 on page 19 for suggested OMCK frequencies

16. Limit the loading on RMCK to 1 CMOS load if operating above 24.576 MHz.

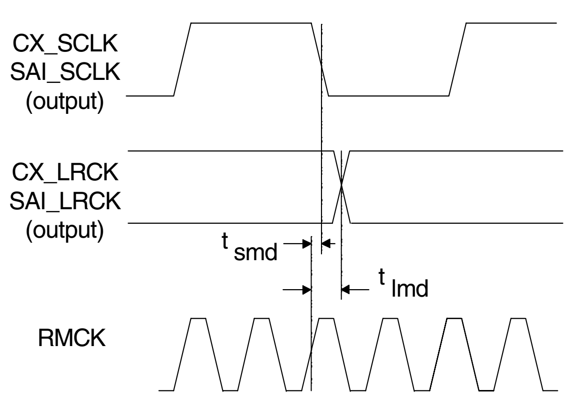


Figure 62. Serial Audio Port Master Mode Timing

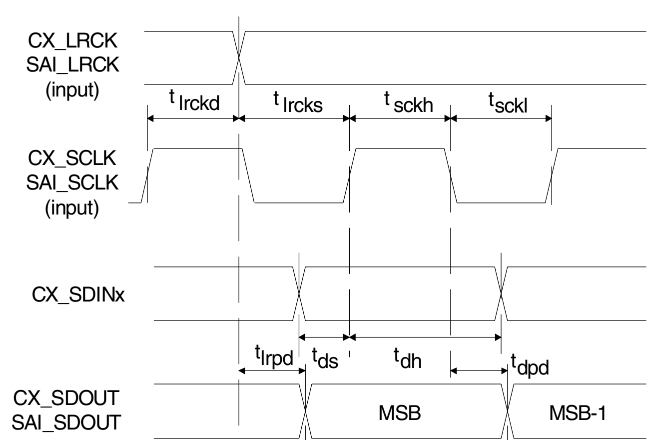


Figure 63. Serial Audio Port Slave Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I^{2}C FORMAT (For CQ, T_A = -10 to +70 °C; For IQ, T_A = -40 to +85 °C; VA=VARX = 5V, VD =VLS= 3.3V; VLC = 1.8 V to 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 17)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling (Note 18)	t_{ack}	-	(Note 19)	ns

Notes: 17. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

18. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.

19. $\frac{15}{256 \times \mathrm{Fs}}$ for Single-Speed Mode, $\frac{15}{128 \times \mathrm{Fs}}$ for Double-Speed Mode, $\frac{15}{64 \times \mathrm{Fs}}$ for Quad-Speed Mode

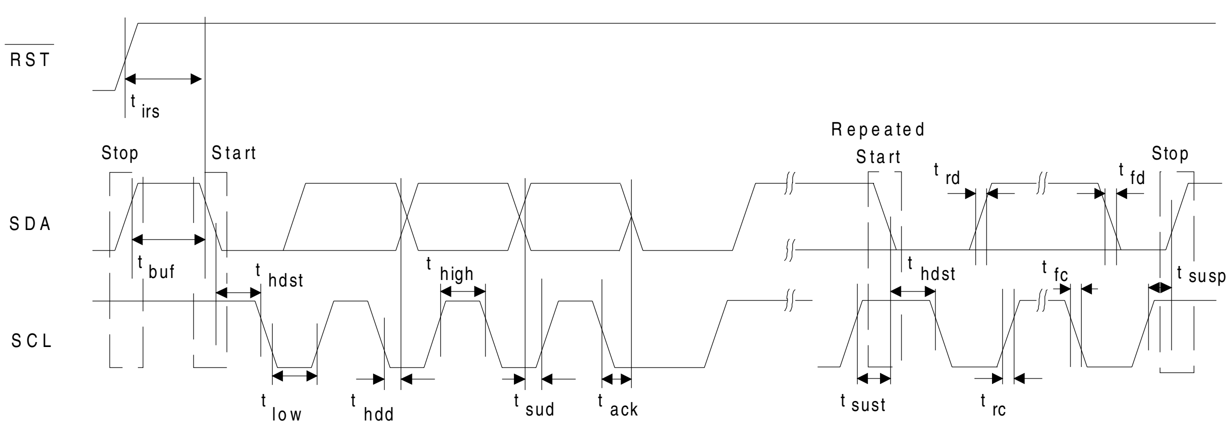


Figure 64. Control Port Timing - I^{2}C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

(For CQ, T_A = -10 to +70 °C; For IQ, T_A = -40 to +85 °C; VA=VARX = 5V, VD =VLS= 3.3V; VLC = 1.8 V to 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Typ	Max	Units
CCLK Clock Frequency	(Note 20)	f_{sck}	0	-	6.0	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	-	ns
CCLK Low Time		t_{scl}	66	-	-	ns
CCLK High Time		t_{sch}	66	-	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	-	ns
CCLK Rising to DATA Hold Time	(Note 21)	t_{dh}	15	-	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	-	50	ns
Rise Time of CDOUT		t_{r1}	-	-	25	ns
Fall Time of CDOUT		t_{f1}	-	-	25	ns
Rise Time of CCLK and CDIN	(Note 22)	t_{r2}	-	-	100	ns
Fall Time of CCLK and CDIN	(Note 22)	t_{f2}	-	-	100	ns

Notes: 20. If Fs is lower than 46.875 kHz, the maximum CCLK frequency should be less than 128 Fs. This is dictated by the timing requirements necessary to access the Channel Status and User Bit buffer memory. Access to the control register file can be carried out at the full 6 MHz rate. The minimum allowable input sample rate is 8 kHz, so choosing CCLK to be less than or equal to 1.024 MHz should be safe for all possible conditions.

21. Data must be held for sufficient time to bridge the transition time of CCLK.

22. For f_{sck} <1 MHz.

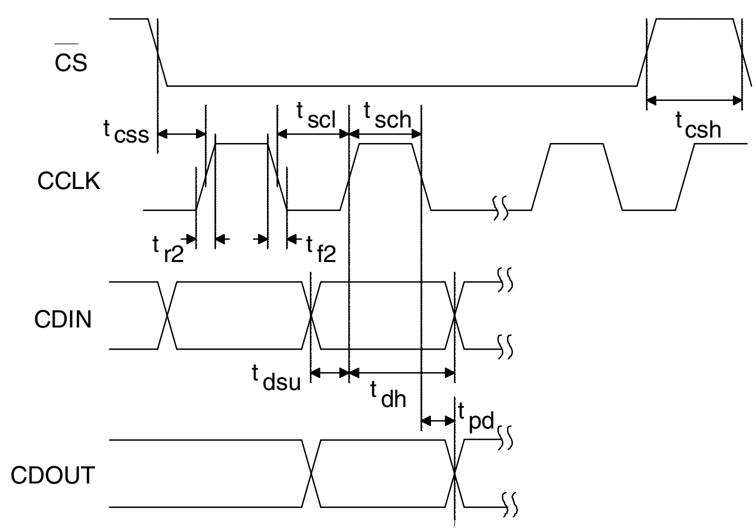


Figure 65. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS (T_A = 25 °C; AGND=DGND=0, all voltages with respect to ground; OMCK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Current	normal operation, VA=VARX=5V	I_A	-	90	-	mA
(Note 23)	VD=5V	I_D	-	150	-	mA
	VD=3.3V	I_D	-	100	-	mA
	Interface current, VLC=5V (Note 24)	I_{LC}	-	250	-	µA
	VLS=5V	I_{LS}	-	250	-	µA
	power-down state (all supplies) (Note 25)	I_{pd}	-	250	-	µA
Power Consumption	(Note 23)					
VA=VARX=5 V, VD=VLS=VLC=3.3 V	normal operation		-	780	850	mW
	power-down (Note 25)		-	1.25	-	mW
VA=VARX=5 V, VD=VLS=VLC=5 V	normal operation		-	950	1050	mW
	power-down (Note 25)		-	1.25	-	mW
Power Supply Rejection Ratio (Note 26)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB

Notes: 23. Current consumption increases with increasing FS and increasing OMCK. Max values are based on highest FS and highest OMCK. Variance between speed modes is negligible.

24. I_{LC} measured with no external loading on the SDA pin.

25. Power down mode is defined as $\overline{\text{RST}}$ pin = Low with all clock and data lines held static.

26. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 1.

DIGITAL INTERFACE CHARACTERISTICS (For CQ, T_A = +25 °C; For IQ, T_A = -40 to +85 °C)

Parameters (Note 27)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Serial Port	V_{IH}	0.7xVLS	-	-	V
	Control Port		0.7xVLC	-	-	V
	S/PDIF-GPO Interface		0.7xVARX	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.2xVLS	V
	Control Port		-	-	0.2xVLC	V
	S/PDIF-GPO Interface		-	-	0.2xVARX	V
High-Level Output Voltage at I_o=2mA	(Note 28)Serial Port	V_{OH}	VLS-1.0	-	-	V
	Control Port		VLC-1.0	-	-	V
	S/PDIF-GPO Interface		VARX-1.0	-	-	V
	MUTEC		VA-1.0	-	-	V
	TXP		VD-1.0	-	-	V
Low-Level Output Voltage at I_o=2mA	(Note 28)					
Serial Port, Control Port, S/PDIF-GPO Interface, MUTEC,TXP		V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
MUTEC Drive Current			-	3	-	mA

Notes: 27. Serial Port signals include: RMCK, OMCK, SAI_SCLK, SAI_LRCK, SAI_SDOUT, CX_SCLK, CX_LRCK, CX_SDOUT, CX_SDIN1-3, ADCIN1/2
Control Port signals include: SCL/CCLK, SDA/CDOUT, AD0/$\overline{\text{CS}}$, AD1/CDIN, INT, $\overline{\text{RST}}$
S/PDIF-GPO Interface signals include: RXP0, RXP/GPO[1:7]

28. When operating RMCK above 24.576 MHz, limit the loading on the signal to 1 CMOS load.

7 PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

8 REFERENCES

1) Cirrus Logic, Audio Quality Measurement Specification, Version 1.0, 1997. *http://www.cirrus.com/products/papers/meas/meas.html*

2) Cirrus Logic, AN18: Layout and Design Rules for Data Converters and Other Mixed Signal Devices, Version 6.0, February 1998.

3) Cirrus Logic, AN22: Overview of Digital Audio Interface Data Structures, Version 2.0, February 1998.; A useful tutorial on digital audio specifications.

4) Cirrus Logic, AN48: Design Notes for a 2-Pole Filter with Differential Input, by Steve Green

5) Cirrus Logic, AN134: AES and S/PDIF Recommended Transformers, Version 2, April 1999.

6) Cirrus Logic, AN 159: PLL Filter Optimization for the CS8415A, CS8420, and CS8427, by Patrick Muyshondt and Stuart Dudley Dimond III. A tutorial on the CS8415A Phase-Locked-Loop.

7) Cirrus Logic, An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission, by Clifton Sanchez.; an excellent tutorial on SCMS. It is available from the AES as preprint 3518.

8) Cirrus Logic, Techniques to Measure and Maximize the Performance of a 120 dB, 96 kHz A/D Converter Integrated Circuit, by Steven Harris, Steven Green and Ka Leung. Presented at the 103rd Convention of the Audio Engineering Society, September 1997.

9) Cirrus Logic, A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio, by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

10) Cirrus Logic, The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's, by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

11) Cirrus Logic, An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example, by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

12) Cirrus Logic, How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters,by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.

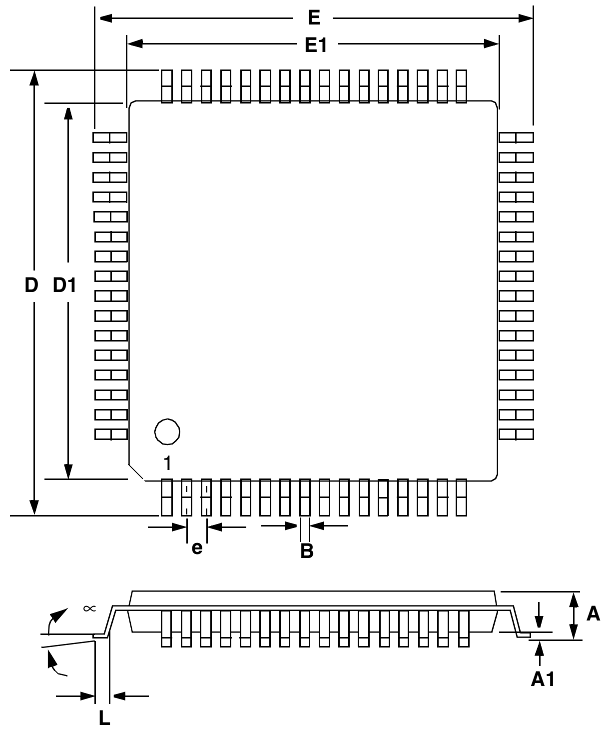
13) Cirrus Logic, A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range, by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

14) International Electrotechnical Commission, IEC60958, *http://www.ansi.org*

15) Philips Semiconductor, The I2C-Bus Specification: Version 2, Dec. 1998. *http://www.semiconductors.philips.com*

9 PACKAGE DIMENSIONS

64L LQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.55	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.008	0.011	0.17	0.20	0.27
D	0.461	0.472 BSC	0.484	11.70	12.0 BSC	12.30
D1	0.390	0.393 BSC	0.398	9.90	10.0 BSC	10.10
E	0.461	0.472 BSC	0.484	11.70	12.0 BSC	12.30
E1	0.390	0.393 BSC	0.398	9.90	10.0 BSC	10.10
e*	0.016	0.020 BSC	0.024	0.40	0.50 BSC	0.60
L	0.018	0.024	0.030	0.45	0.60	0.75
∝	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS022

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Allowable Junction Temperature		-	-	+135	°C
Junction to Ambient Thermal Impedance	θ_{JA}	-	48	-	°C/Watt

CIRRUS LOGIC®