



Dual, 10-Bit, Current-Sink Output DAC

MAX5547

General Description

The MAX5547 dual, 10-bit, dual range, digital-to-analog converter (DAC) sinks up to 3.6mA of current, making it ideal for laser-driver-control applications. Parallel the MAX5547 outputs to sink higher current (up to 7.2mA max). Operating from a single +2.7V to +5.25V supply, the MAX5547 typically consumes 1mA (internal reference).

The MAX5547 operates from a precision +2.5V internal 4ppm/°C reference or an external reference in the +2.45V to +2.55V range. The maximum full-scale current-sink range is software programmable to 3.6mA or 1.2mA for each DAC. A 10MHz SPI™-compatible serial interface configures the device.

The MAX5547 is available in a 3mm x 3mm x 0.8mm 8-pin TDFN package and is specified over the -40°C to +85°C extended temperature range.

Applications

Laser-Driver Control
Pin-Diode Bias Currents
Modulation Currents
Average Power
Extinction Ratios

Features

- ◆ Dual Current-Sink DACs
- ◆ 10-Bit Resolution
- ◆ Two Software-Programmable Full-Scale Current Ranges: 3.6mA or 1.2mA
- ◆ Parallelable Outputs for Up to 7.2mA (max)
- ◆ +2.5V Internal Reference Drifts Only 4ppm/°C
- ◆ +2.7V to +5.25V Single-Supply Operation
- ◆ INL: ±4 LSB (1.2mA Output)
- ◆ DNL: ±0.75 LSB (Guaranteed Monotonic)
- ◆ Low +0.8V Output Compliance
- ◆ Ultra-Small, 3mm x 3mm x 0.8mm, 8-Pin TDFN Package

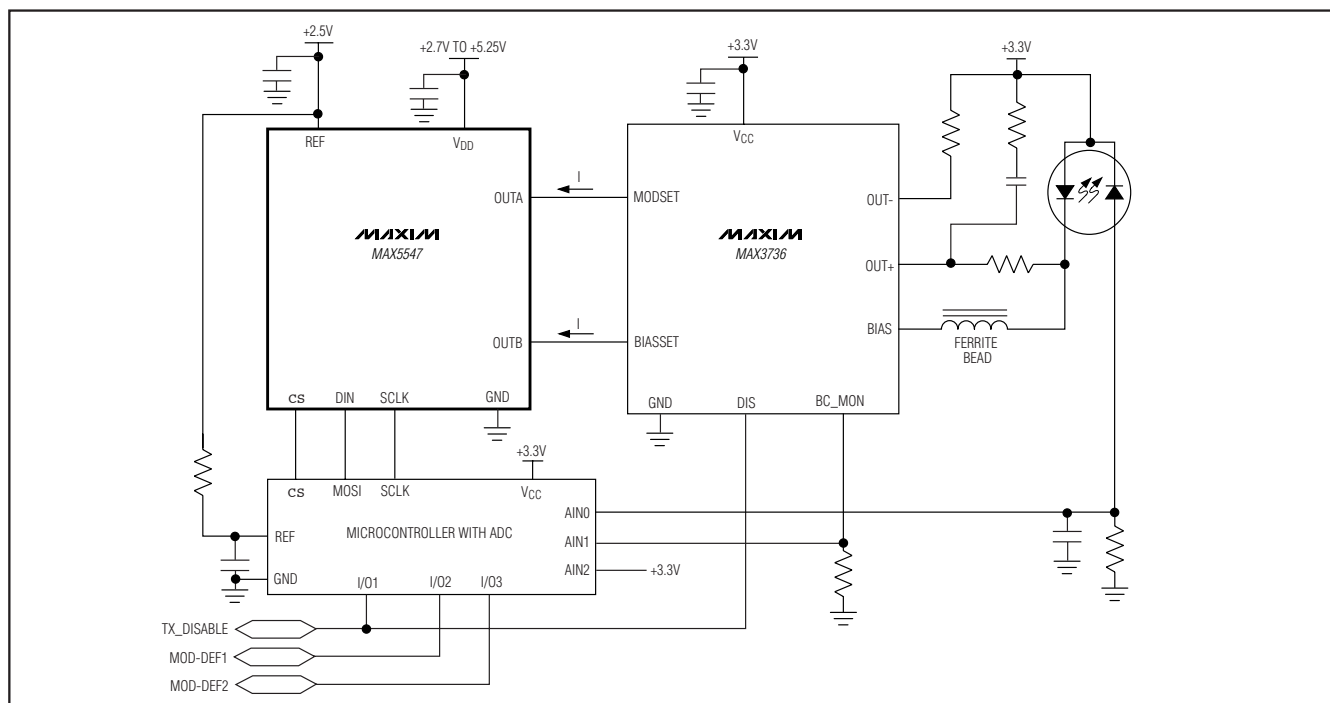
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	PKG CODE
MAX5547ETA	-40°C to +85°C	8 TDFN-EP*	APF	T833-2

*EP = Exposed pad.

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



SPI is a trademark of Motorola, Inc.



Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual, 10-Bit, Current-Sink Output DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND-0.3V to +6V
 OUTA, OUTB, REF to GND-0.3V to (V_{DD} + 0.3V)
 SCLK, DIN, \overline{CS} to GND-0.3V to +6V
 Continuous Power Dissipation (T_A = +70°C)
 8-Pin TDFN (derate 18.2mW/°C above +70°C)1454.5mW

Operating Temperature Range-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7 to +5.25V, GND = 0, external reference = +2.5V, output voltage = +2.0V, T_A = -40°C to +85°C. Typical values are at V_{DD} = +3.0V, and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution			10			Bits
Integral Nonlinearity (Note 2)	INL	I _{OUT} = 1.2mA		±4		LSB
		I _{OUT} = 3.6mA		±6		
Differential Nonlinearity	DNL	Guaranteed monotonic		±0.75		LSB
Offset Error	OE	Code = 030h		±4		LSB
Offset Temperature Coefficient				0.05		LSB/°C
Gain Error	GE	Measured from code 030h to 3FFh		±0.1	±3	%
				±0.1	±5.5	
Gain Temperature Coefficient		I _{OUT} = 1.2mA		15		ppm/°C
		I _{OUT} = 3.6mA		25		
Line Regulation		V _{DD} = +2.7V to +5.25V			0.8	LSB/V
Output Crosstalk		OUTA = midscale, OUTB switching from 030h to 3FFh		54		dB
REFERENCE						
Internal-Reference Voltage	V _{REF}	T _A = +25°C	2.48	2.5	2.52	V
Internal-Reference Temperature Coefficient		(Note 3)		4	35	ppm/°C
Internal-Reference Load Regulation		0μA < I _{REF} < +300μA		1	3.5	Ω
Internal-Reference Power-Up Time		C _{REF} = 1μF, to 0.05%		0.55		ms
Internal-Reference Sink Current					50	μA
Internal-Reference Source Current					300	μA
REF Capacitive Load		(Note 3)	0.1		10.0	μF
Reference Line Regulation		V _{DD} = +2.7V to +5.25V		25		μV/V
Internal-Reference Noise		f = 0.1Hz to 10Hz		10		μV _{RMS}
		f = 10Hz to 10kHz		27		
External-Reference Range	V _{REF}		2.45		2.55	V

Dual, 10-Bit, Current-Sink Output DAC

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.7$ to $+5.25$ V, $GND = 0$, external reference = $+2.5$ V, output voltage = $+2.0$ V, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. Typical values are at $V_{DD} = +3.0$ V, and $T_A = +25^{\circ}\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
External-Reference Input Impedance	RREF			90			kΩ
DAC OUTPUTS							
Output Current (Note 4)	IOUT_	1.2mA low-current range	Code = 030h	50			μA
			Code = 3FFh	1170	1200	1230	
		3.6mA high-current range	Code = 030h	150			
			Code = 3FFh	3400	3600	3800	
LSB Size		1.2mA full-scale current		1.17			μA
		3.6mA full-scale current		3.52			
Current-Source Compliance Voltage Range		IOUT_ = full-scale (Note 5)		0.8	VDD		V
Output Impedance at Full-Scale Current		IOUT_ = 1.2mA		800			kΩ
		IOUT_ = 3.6mA		180			
DYNAMIC PERFORMANCE							
Settling Time	ts	To 1% (Note 6)		10			μs
Output Noise	IRMS	f = 0.1Hz to 10Hz		0.05			LSBRMS
		f = 10Hz to 10kHz		0.35			
Supply Feedthrough		100mV, 1kHz signal added to VDD		0.85			LSB/V
Digital Feedthrough		RLOAD = 500Ω, CLOAD = 100pF		2			pA•s
Digital-to-Analog Glitch Impulse		RLOAD = 500Ω, CLOAD = 100pF		16			pA•s
DAC-to-DAC Full-Scale Current Matching				2			%
POWER SUPPLIES							
Supply Voltage	VDD			+2.70	+5.25		V
Supply Current	IDD	VDD = +5.25V, no load, SCLK not switching	Internal reference mode	1.1	2		mA
			External reference mode	0.75	1.5		
LOGIC AND CONTROL INPUTS							
Input High Voltage	VIH	(Note 7)		0.7 x VDD			V
Input Low Voltage	VIL	(Note 7)		0.8			V
Input Hysteresis	VHYS			0.05 x VDD			V
Input Capacitance	CIN			10			pF
Input Leakage Current	IIN			±1			μA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.7$ to $+5.25V$, $GND = 0$, external reference = $+2.5V$, output voltage = $+2.0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $V_{DD} = +3.0V$, and $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING CHARACTERISTICS (see Figure 1)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
\overline{CS} Fall to SCLK Fall Setup Time	t_{CSS}		25			ns
SCLK Fall to \overline{CS} Rise Hold Time	t_{CSH}		50			ns
DIN to SCLK Fall Setup Time	t_{DS}		40			ns
DIN to SCLK Fall Hold Time	t_{DH}		0			ns
\overline{CS} Pulse-Width High	t_{CSW}		100			ns

Note 1: Devices are 100% production tested at $T_A = +25^{\circ}C$. Limits over temperature are guaranteed by design.

Note 2: INL linearity is from code 48 to code 1023.

Note 3: Guaranteed by design. Not production tested.

Note 4: The DACs continue to operate at currents lower than $50\mu A$ on the $1.2mA$ range and $150\mu A$ on the $3.6mA$ range. However, performance is not guaranteed at these low currents. A code of all zeros has a nominal output current of $0\mu A$.

Note 5: Compliance voltage range is defined as the range where the output current is -2 LSB of its value at $V_{OUT} = +1V$.

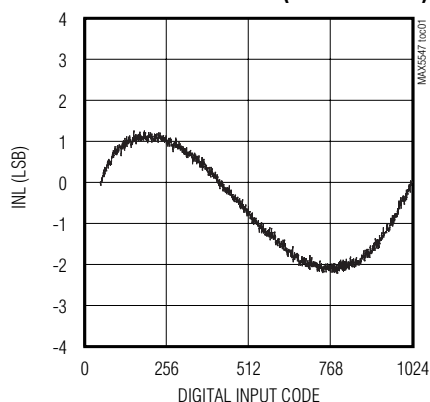
Note 6: Settling time is measured from $0.25 \times$ full scale to $0.75 \times$ full scale.

Note 7: The device draws higher supply current when the digital inputs are driven with voltages between ($V_{DD} - 0.5V$) and ($GND + 0.5V$). See Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics*.

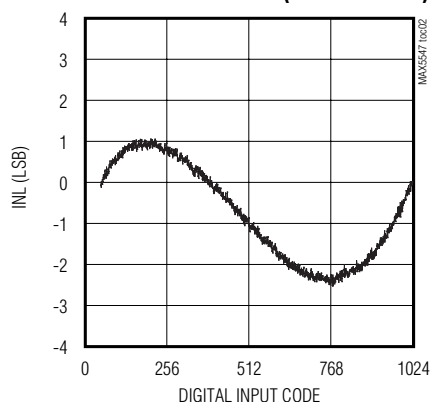
Typical Operating Characteristics

($V_{DD} = +3.0V$, $GND = 0$, external reference = $+2.5V$, $T_A = +25^{\circ}C$, unless otherwise noted.)

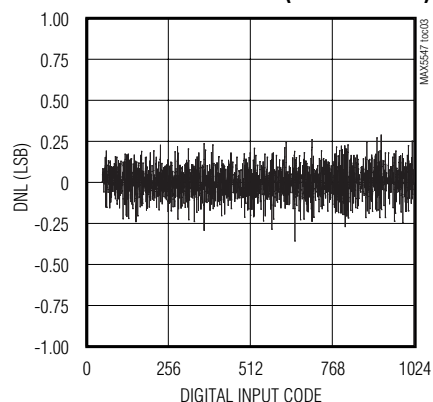
**INTEGRAL NONLINEARITY
vs. DIGITAL INPUT CODE (1.2mA SETTING)**



**INTEGRAL NONLINEARITY
vs. DIGITAL INPUT CODE (3.6mA SETTING)**



**DIFFERENTIAL NONLINEARITY
vs. DIGITAL INPUT CODE (1.2mA SETTING)**



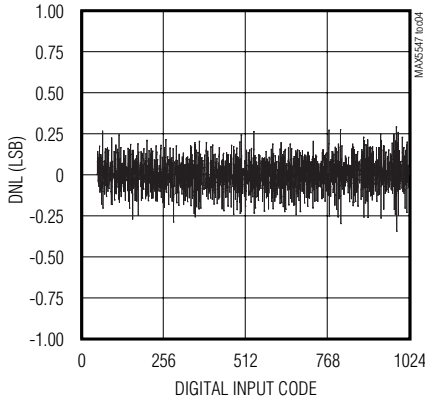
Dual, 10-Bit, Current-Sink Output DAC

MAX5547

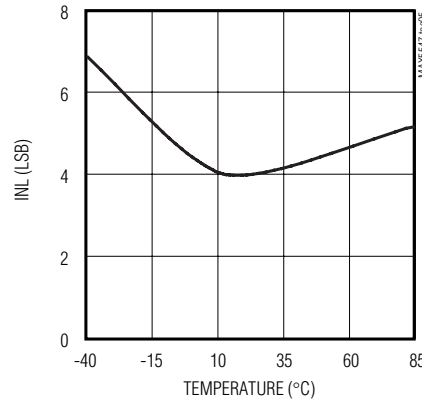
Typical Operating Characteristics (continued)

($V_{DD} = +3.0V$, $GND = 0$, external reference = $+2.5V$, $T_A = +25^\circ C$, unless otherwise noted.)

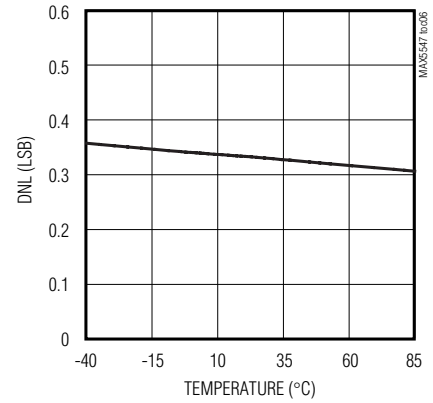
**DIFFERENTIAL NONLINEARITY
vs. DIGITAL INPUT CODE (3.6mA SETTING)**



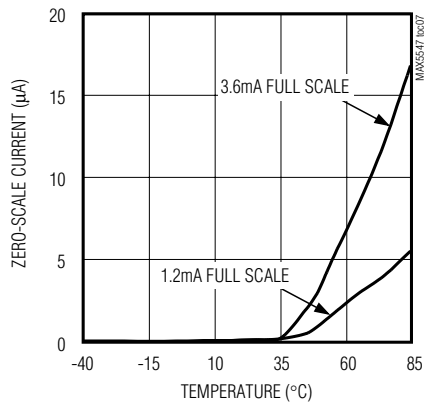
**MAXIMUM INTEGRAL NONLINEARITY
vs. TEMPERATURE (3.6mA SETTING)**



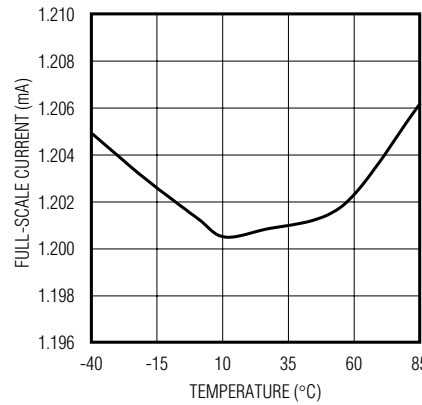
**MAXIMUM DIFFERENTIAL NONLINEARITY
vs. TEMPERATURE (3.6mA SETTING)**



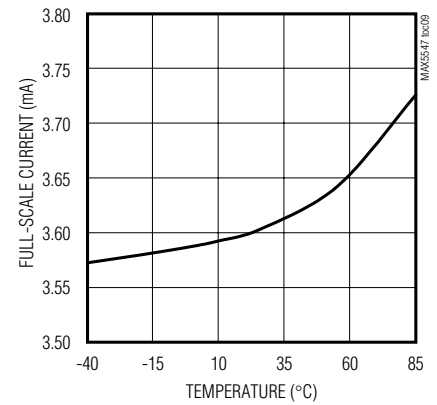
**ZERO-SCALE SINK CURRENT
vs. TEMPERATURE**



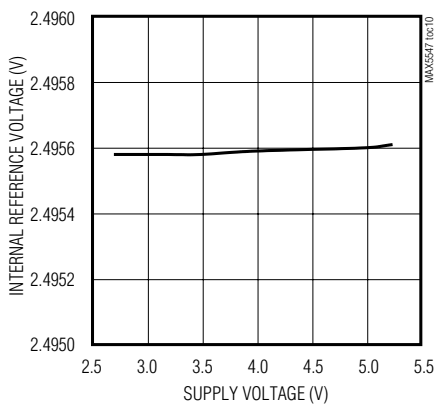
**FULL-SCALE SINK CURRENT
vs. TEMPERATURE (1.2mA SETTING)**



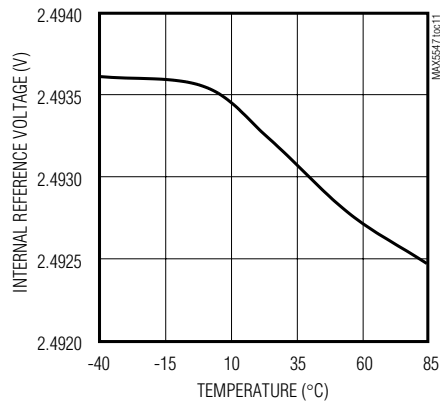
**FULL-SCALE SINK CURRENT
vs. TEMPERATURE (3.6mA SETTING)**



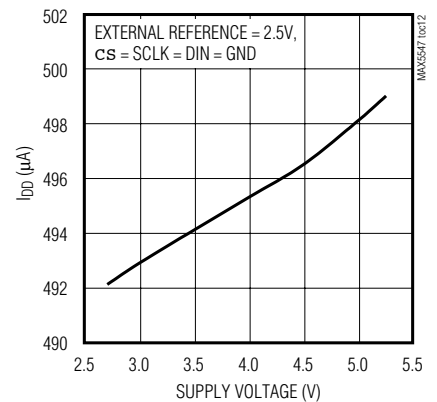
**INTERNAL REFERENCE VOLTAGE
vs. SUPPLY VOLTAGE**



**INTERNAL REFERENCE
VOLTAGE vs. TEMPERATURE**



SUPPLY CURRENT vs. SUPPLY VOLTAGE

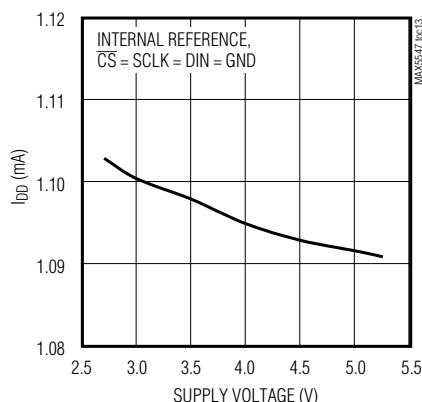


Dual, 10-Bit, Current-Sink Output DAC

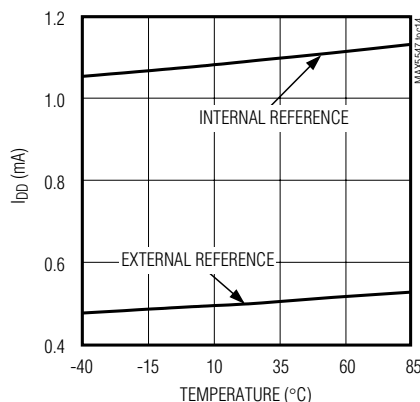
Typical Operating Characteristics (continued)

($V_{DD} = +3.0V$, $GND = 0$, external reference = $+2.5V$, $T_A = +25^\circ C$, unless otherwise noted.)

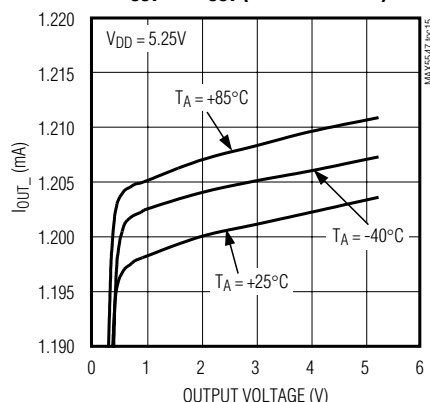
SUPPLY CURRENT vs. SUPPLY VOLTAGE



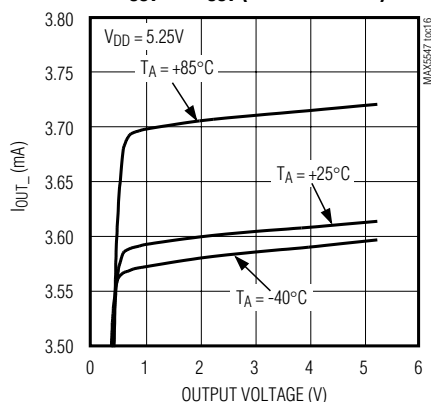
SUPPLY CURRENT vs. TEMPERATURE



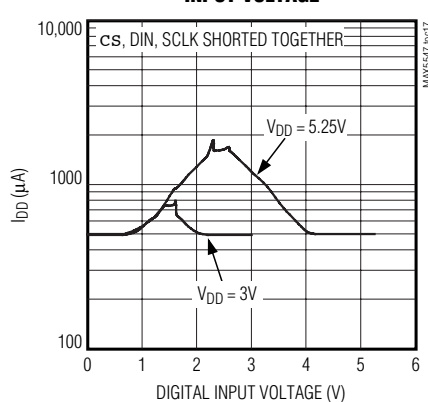
I_{OUT} vs. V_{OUT} (1.2mA SETTING)



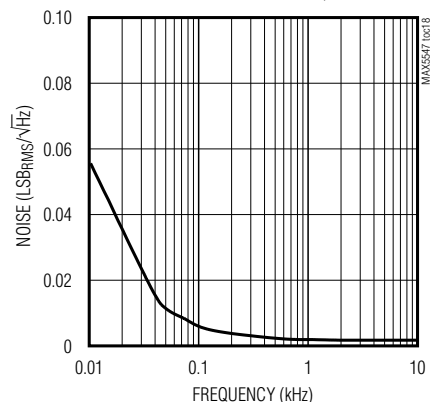
I_{OUT} vs. V_{OUT} (3.6mA SETTING)



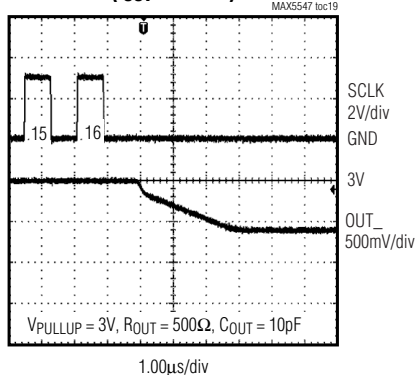
SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



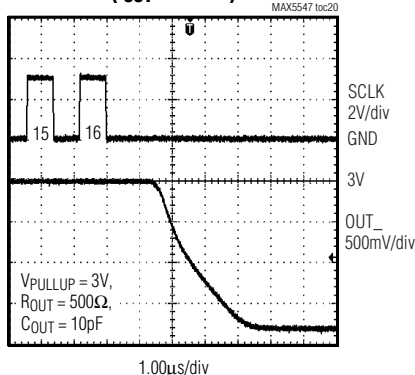
OUTPUT NOISE vs. FREQUENCY



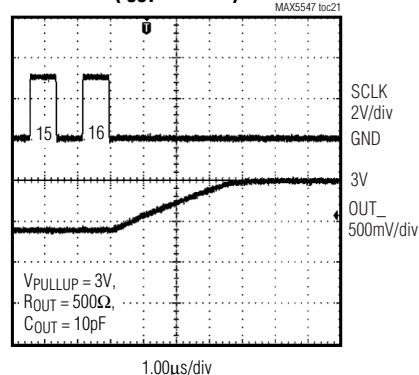
SETTLING TIME (FULL-SCALE POSITIVE STEP) (I_{OUT} = 1.2mA)



SETTLING TIME (FULL-SCALE POSITIVE STEP) (I_{OUT} = 3.6mA)



SETTLING TIME (FULL-SCALE NEGATIVE STEP) (I_{OUT} = 1.2mA)



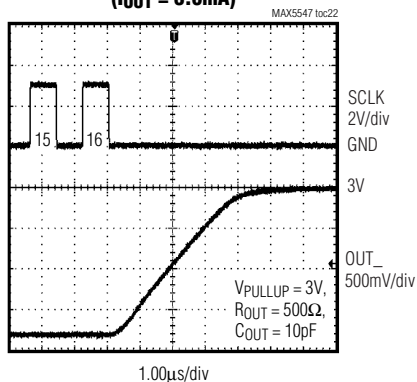
Dual, 10-Bit, Current-Sink Output DAC

MAX5547

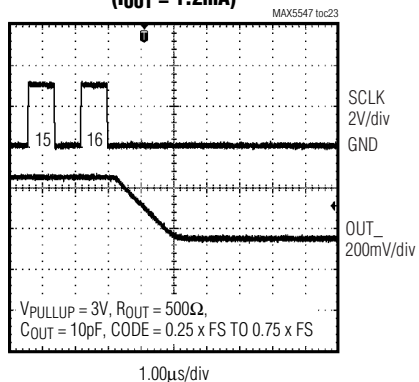
Typical Operating Characteristics (continued)

($V_{DD} = +3.0V$, $GND = 0$, external reference = $+2.5V$, $T_A = +25^\circ C$, unless otherwise noted.)

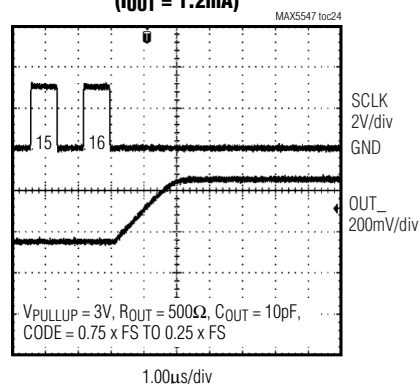
**SETTLING TIME
(FULL-SCALE NEGATIVE STEP)
($I_{OUT} = 3.6mA$)**



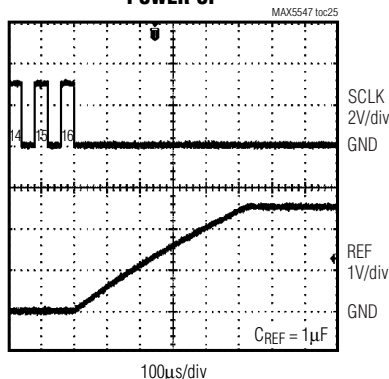
**SETTLING TIME
(HALF-SCALE POSITIVE STEP)
($I_{OUT} = 1.2mA$)**



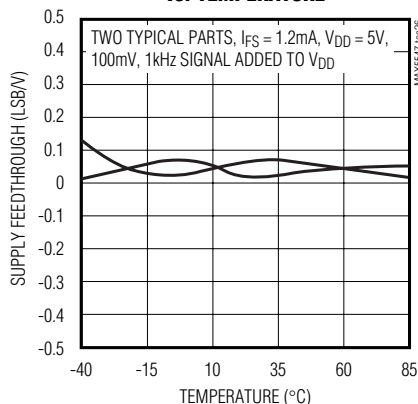
**SETTLING TIME
(HALF-SCALE NEGATIVE STEP)
($I_{OUT} = 1.2mA$)**



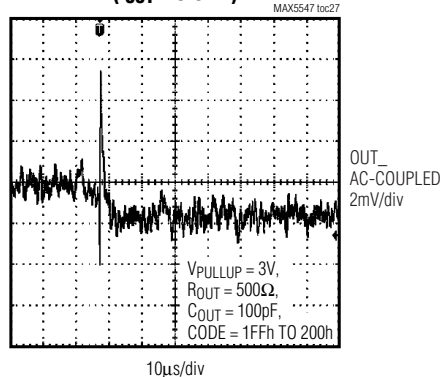
**INTERNAL REFERENCE
POWER-UP**



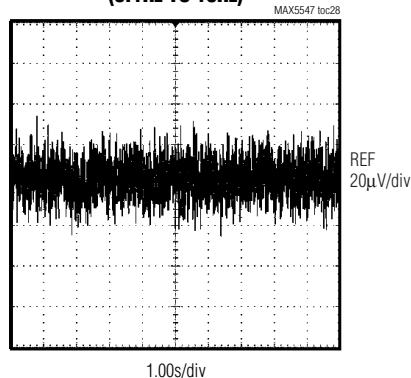
**SUPPLY FEEDTHROUGH
vs. TEMPERATURE**



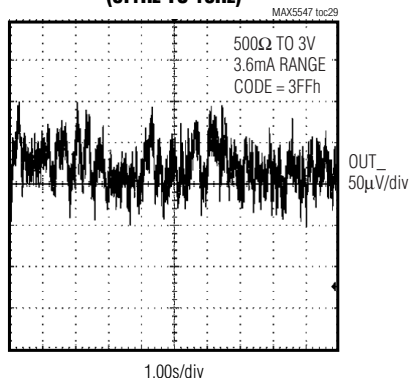
**GLITCH IMPULSE
(MAJOR CARRY TRANSITION)
($I_{OUT} = 3.6mA$)**



**INTERNAL REFERENCE NOISE
(0.1Hz TO 10Hz)**



**OUTPUT NOISE
(0.1Hz TO 10Hz)**



Dual, 10-Bit, Current-Sink Output DAC

Pin Description

PIN	NAME	FUNCTION
1	V _{DD}	Supply Voltage. Set V _{DD} between +2.7V to +5.25V. Bypass V _{DD} with a 0.1μF capacitor to GND, as close to the device as possible.
2	$\overline{\text{CS}}$	Active-Low Chip-Select Input. Set $\overline{\text{CS}}$ low to enable the serial interface.
3	SCLK	Serial-Clock Input
4	DIN	Serial-Data Input. DIN is clocked into the serial interface on the falling edge of SCLK.
5	GND	Ground
6	REF	External Reference Input/Internal Reference Output. When programmed for internal reference mode, REF is a +2.5V output. When programmed for external reference mode, apply a voltage between +2.45V and +2.55V (see Table 1). Connect a 1μF ceramic capacitor from REF to GND, as close to the device as possible.
7	OUTB	DAC B Current Output. OUTB sinks up to 3.6mA.
8	OUTA	DAC A Current Output. OUTA sinks up to 3.6mA.
—	EP	Exposed Pad. Connect to GND. Do not use as the ground connection.

Detailed Description

The MAX5547 10-bit, dual-range, current-sink DAC operates with serial data clock rates up to 10MHz. The double-buffered DAC input consists of a 16-bit input register and two 10-bit DAC registers, followed by a current-steering array (see the *Functional Diagram*). The MAX5547 sinks full-scale output currents of 1.2mA or 3.6mA per DAC. Each DAC's full-scale current can be independently programmed.

Operating from a single +2.7V to +5.25V supply, the MAX5547 typically consumes 1mA. The MAX5547 operates from an internal +2.5V reference or an external reference in the +2.45V to +2.55V range.

The MAX5547 is ideal as the digital/analog interface for laser-diode drivers with current-controlled inputs, such as the MAX3736 (see the *Typical Operating Circuit*). Set the current levels at the MAX3736's MODSET and BIASSET current-controlled inputs from the MAX5547's DAC outputs. The MAX3736's MODSET and BIASSET lines set the laser driver's desired modulation and bias currents.

Reference Architecture and Operation

The MAX5547 operates from an internal +2.5V reference or accepts an external reference voltage source between +2.45V and +2.55V. The internal reference is capable of sinking up to 50μA and sourcing up to 300μA. REF serves as the input for a low-impedance

reference source in external reference mode. Bypass REF to GND with a ceramic capacitor in the 0.1μF to 10μF range, as close to the device as possible, in both internal and external reference modes.

During startup, when power is first applied, the MAX5547 defaults to external reference mode, and to the 1.2mA full-scale current-range mode. Use software commands to select internal reference mode and 3.6mA full-scale current-range mode (see Table 1).

DAC Data

The MAX5547's internal registers set the DAC full-scale output currents (I_{FS}) to 1.2mA or 3.6mA (see Table 1). The 10-bit DAC data is decoded as straight binary, with 1 LSB = I_{FS} / 1023, and converted into the corresponding current as shown in Table 2.

Serial Interface

The MAX5547 operates through a 3-wire, 10MHz SPI-compatible serial interface. $\overline{\text{CS}}$, SCLK, and DIN control the serial interface timing and data. Ensure the SPI bus master, typically a microcontroller (μC), runs in master mode so that it generates the serial clock signal. Select an SCLK frequency of 10MHz or less and set the clock polarity (CPOL) and phase (CPHA) in the μC control registers to opposite values. The MAX5547 operates with SCLK idling high or low. Therefore, set CPOL = 0 and CPHA = 1, or CPOL = 1 and CPHA = 0.

Dual, 10-Bit, Current-Sink Output DAC

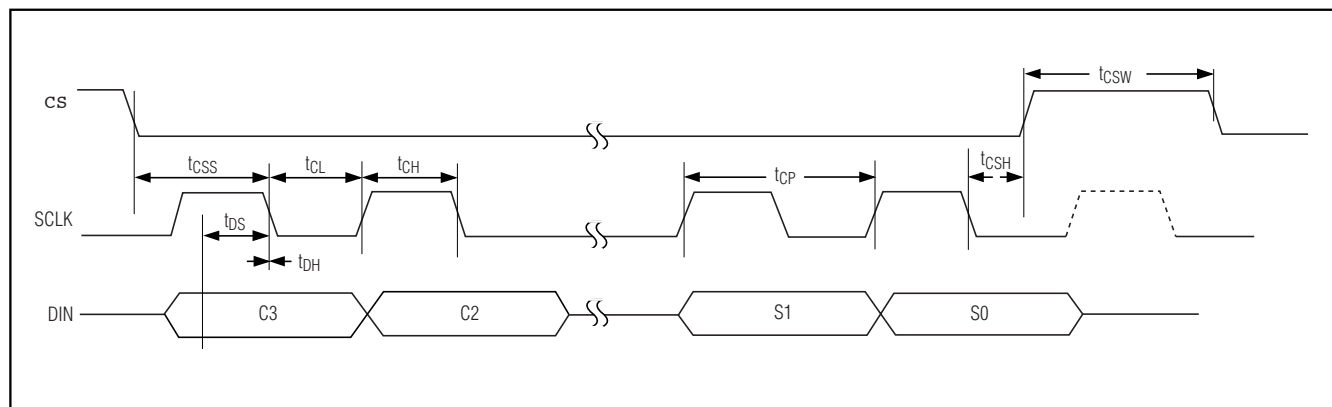


Figure 1. SPI Serial-Interface Timing Diagram

Set \overline{CS} low to begin clocking input data at DIN on the falling edge of SCLK (see Figure 1). Serial communications to the shift register consist of a 16-bit command word loaded from DIN. The first four control bits (C3–C0) determine the target register (see Table 1). The next 10 data bits set the current-sink level. D9 is the MSB and D0 the LSB. Set bits S1 and S0 to zero for proper operation. Data is latched into the appropriate DAC register on the 16th SCLK falling edge. After writing 16 bits, drive \overline{CS} high. Keep \overline{CS} low throughout the entire 16-bit word.

Write the command word to configure DAC registers A and B individually or both registers at the same time. The command word also determines whether the DACs use the internal or external reference.

The MAX5547 powers up in external reference mode with DAC registers A and B set to $I_{FS} = 1.2\text{mA}$ at code 000h.

Applications Information

Power Sequencing

Ensure the voltages applied at REF, OUTA, and OUTB do not exceed V_{DD} at any time. If proper power sequencing is not possible, connect an external Schottky diode between REF/OUTA/OUTB and V_{DD} to ensure compliance with the absolute maximum ratings.

Power-Supply Bypassing and Ground Management

Digital or AC transient signals on GND create noise at the analog output. Return GND to the highest quality ground plane available. For extremely noisy environments, bypass both REF and V_{DD} to GND with $10\mu\text{F}$ and $0.1\mu\text{F}$ capacitors in parallel, with the $0.1\mu\text{F}$ capacitor as close to the device as possible. Careful PC board ground layout minimizes crosstalk between the DAC outputs and digital inputs.

Dual, 10-Bit, Current-Sink Output DAC

14C3541

Table 1. Command Word Summary

CONTROL BITS				DATA BITS										LSB		REGISTER FUNCTION
C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S1	S0	
0	0	0	0	X	X	X	X	X	X	X	X	X	X	0	0	External reference mode (default state). Connect an external voltage source at REF from +2.45V to +2.55V.
1	0	0	0	X	X	X	X	X	X	X	X	X	X	0	0	Internal reference mode. Internal reference is +2.5V.
0	0	1	0	10-bit data										0	0	Load DAC register A and set IOUTA full-scale range to 1.2mA.
0	0	1	1	10-bit data										0	0	Load DAC register A and set IOUTA full-scale range to 3.6mA.
0	1	0	0	10-bit data										0	0	Load DAC register B and set IOUTB full-scale range to 1.2mA.
0	1	0	1	10-bit data										0	0	Load DAC register B and set IOUTB full-scale range to 3.6mA.
0	1	1	0	10-bit data										0	0	Load DAC registers A and B and set IOUTA and IOUTB full-scale ranges to 1.2mA (default state).
0	1	1	1	10-bit data										0	0	Load DAC registers A and B and set IOUTA and IOUTB ranges to 3.6mA.

X = Don't care. Unused codes are reserved for factory use.

Table 2. Ideal DAC Output Code Table

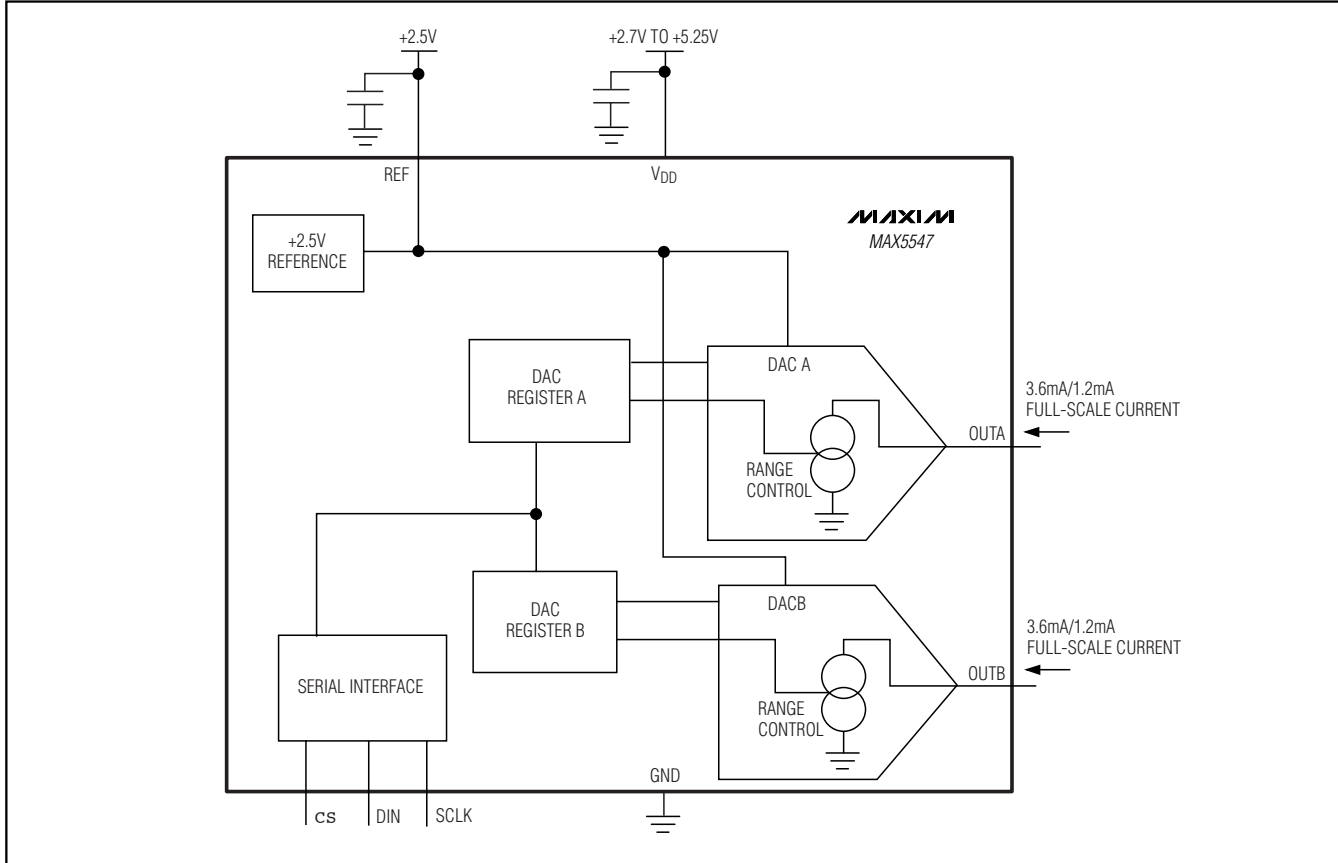
BINARY DAC CODE	I _{OUT}
11 1111 1111	$1023 \times \frac{I_{FS}}{1023}$
10 0000 0000	$512 \times \frac{I_{FS}}{1023}$
00 0000 0001	$\frac{I_{FS}}{1023}$
00 0000 0000	0

Chip Information

PROCESS: BiCMOS

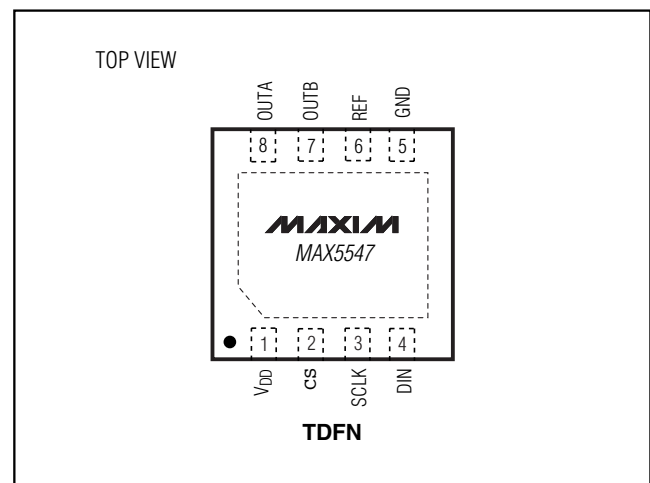
Dual, 10-Bit, Current-Sink Output DAC

Functional Diagram



MAX5547

Pin Configuration



WACHS

The drawing illustrates the mechanical specifications for a 6, 8, 10, & 14-pin DFN thin EPS package. It includes three main views: TOP VIEW, SIDE VIEW, and BOTTOM VIEW, along with a detailed cross-section (DETAIL A).

- TOP VIEW:** Shows the package footprint with dimensions D (width) and E (length). A shaded area labeled "PIN 1 INDEX AREA" is located in the top-left corner, with "1" indicating the pin 1 position.
- SIDE VIEW:** Shows the package profile with dimensions $A1$ (total height) and $A2$ (height of the terminal area).
- BOTTOM VIEW:** Shows the underside of the package with dimensions L (lead length), $D2$ (lead width), N (pitch), b (lead thickness), $E2$ (lead height), k (lead spacing), DAP (lead angle), $PIN 1 ID$ (pin 1 identification), 0.35×0.35 (lead thickness), e (lead thickness), and $[(N/2)-1] \times e$ (lead length).
- DETAIL A:** A cross-sectional view of the lead showing the "EVEN TERMINAL" and "ODD TERMINAL" configurations. It includes dimensions L (lead length), C (lead thickness), and R (lead radius, noted as optional). The "TERMINAL TIP" is also indicated.

PACKAGE OUTLINE: 6, 8, 10 & 14L, DFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL: **DALLAS SEMICONDUCTOR** **MAXIM**

TITLE: PACKAGE OUTLINE, 6, 8, 10 & 14L, DFN, EXPOSED PAD, 3x3x0.80 mm

DOC-NO. CONTROL NO.: 21-0137

REV. G 1/2

-DRAWING NOT TO SCALE-

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS									
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNSLOPES ALLOWED	
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO	
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO	
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO	
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO	
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES	
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO	
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	---	0.20±0.05	2.40 REF	YES	
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	---	0.20±0.05	2.40 REF	NO	

NOTES:

- NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
 2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
 3. WARPAGE SHALL NOT EXCEED 0.10 mm.
 4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
 5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
 6. "N" IS THE TOTAL NUMBER OF LEADS.
 7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

 DALLAS SEMICONDUCTOR					
TITLE PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm					
APPROVAL		DOCUMENT CONTROL NO. 21-0137		REV. G 2/2	

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