

Inverting Regulator - Buck, Boost, Switching

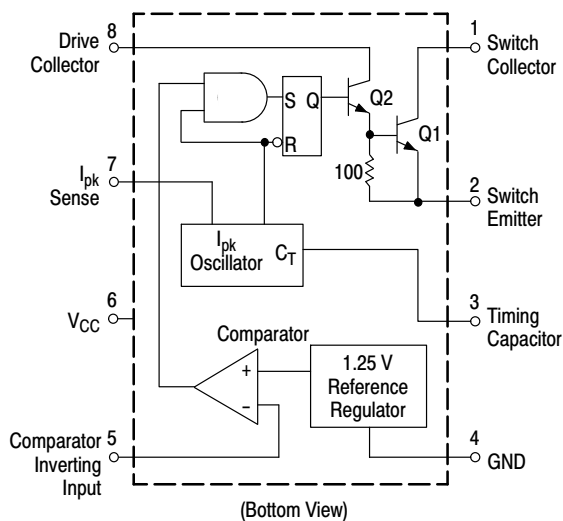
1.5 A

MC34063A, MC33063A, SC33063A, NCV33063A

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components. Refer to Application Notes AN920A/D and AN954/D for additional design information.

Features

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



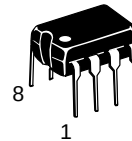
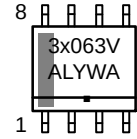
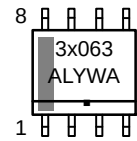
This device contains 79 active transistors.

Figure 1. Representative Schematic Diagram

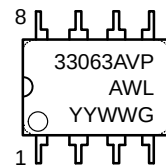
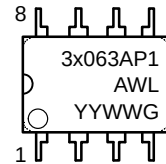


SOIC-8
D SUFFIX
CASE 751

MARKING DIAGRAMS



PDIP-8
P, P1 SUFFIX
CASE 626



x = 3 or 4
A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

MC34063A, MC33063A, SC33063A, NCV33063A

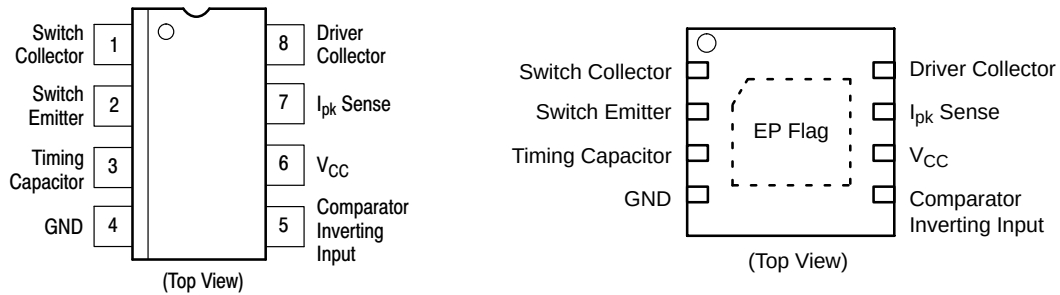


Figure 2. Pin Connections

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{Pin\ 1} = 40\ V$)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	A
Power Dissipation and Thermal Characteristics			
Plastic Package, P, P1 Suffix			
$T_A = 25^\circ C$	P_D	1.25	W
Thermal Resistance	$R_{\theta JA}$	115	$^\circ C/W$
SOIC Package, D Suffix			
$T_A = 25^\circ C$	P_D	625	mW
Thermal Resistance	$R_{\theta JA}$	160	$^\circ C/W$
Thermal Resistance	$R_{\theta JC}$	45	$^\circ C/W$
DFN Package			
$T_A = 25^\circ C$	P_D	1.25	mW
Thermal Resistance	$R_{\theta JA}$	80	$^\circ C/W$
Operating Junction Temperature	T_J	+150	$^\circ C$
Operating Ambient Temperature Range	T_A		$^\circ C$
MC34063A		0 to +70	
MC33063AV, NCV33063A		-40 to +125	
MC33063A, SC33063A		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Maximum package power dissipation limits must be observed.
- This device series contains ESD protection and exceeds the following tests: Human Body Model 4000 V per MIL-STD-883, Method 3015. Machine Model Method 400 V.
- NCV prefix is for automotive and other applications requiring site and change control.

MC34063A, MC33063A, SC33063A, NCV33063A

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = T_{low}$ to T_{high} [Note 4], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

OSCILLATOR

Frequency ($V_{Pin\ 5} = 0\text{ V}$, $C_T = 1.0\text{ nF}$, $T_A = 25^\circ\text{C}$)	f_{osc}	24	33	42	kHz
Charge Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$)	I_{chg}	24	35	42	μA
Discharge Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$)	I_{dischg}	140	220	260	μA
Discharge to Charge Current Ratio (Pin 7 to V_{CC} , $T_A = 25^\circ\text{C}$)	I_{dischg}/I_{chg}	5.2	6.5	7.5	–
Current Limit Sense Voltage ($I_{chg} = I_{dischg}$, $T_A = 25^\circ\text{C}$)	$V_{ipk(sense)}$	250	300	350	mV

OUTPUT SWITCH (Note 5)

Saturation Voltage, Darlington Connection ($I_{SW} = 1.0\text{ A}$, Pins 1, 8 connected)	$V_{CE(sat)}$	–	1.0	1.3	V
Saturation Voltage (Note 6) ($I_{SW} = 1.0\text{ A}$, $R_{Pin\ 8} = 82\ \Omega$ to V_{CC} , Forced $\beta \approx 20$)	$V_{CE(sat)}$	–	0.45	0.7	V
DC Current Gain ($I_{SW} = 1.0\text{ A}$, $V_{CE} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	h_{FE}	50	75	–	–
Collector Off-State Current ($V_{CE} = 40\text{ V}$)	$I_{C(off)}$	–	0.01	100	μA

COMPARATOR

Threshold Voltage $T_A = 25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	V_{th}	1.225 1.21	1.25 –	1.275 1.29	V
Threshold Voltage Line Regulation ($V_{CC} = 3.0\text{ V}$ to 40 V) MC33063, MC34063 MC33063V, NCV33063	Reg_{line}	– –	1.4 1.4	5.0 6.0	mV
Input Bias Current ($V_{in} = 0\text{ V}$)	I_{IB}	–	–20	–400	nA

TOTAL DEVICE

Supply Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $C_T = 1.0\text{ nF}$, Pin 7 = V_{CC} , $V_{Pin\ 5} > V_{th}$, Pin 2 = GND, remaining pins open)	I_{CC}	–	–	4.0	mA
---	----------	---	---	-----	----

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $T_{low} = 0^\circ\text{C}$ for MC34063, SC34063; -40°C for MC33063, SC33063, MC33063V, NCV33063
 $T_{high} = +70^\circ\text{C}$ for MC34063, SC34063; $+85^\circ\text{C}$ for MC33063, SC33063; $+125^\circ\text{C}$ for MC33063V, NCV33063
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
- If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ($\leq 300\text{ mA}$) and high driver currents ($\geq 30\text{ mA}$), it may take up to $2.0\ \mu\text{s}$ for it to come out of saturation. This condition will shorten the off time at frequencies $\geq 30\text{ kHz}$, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

$$\text{Forced } \beta \text{ of output switch : } \frac{I_{C \text{ output}}}{I_{C \text{ driver}} - 7.0\text{ mA}} \geq 10$$

* The $100\ \Omega$ resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

MC34063A, MC33063A, SC33063A, NCV33063A

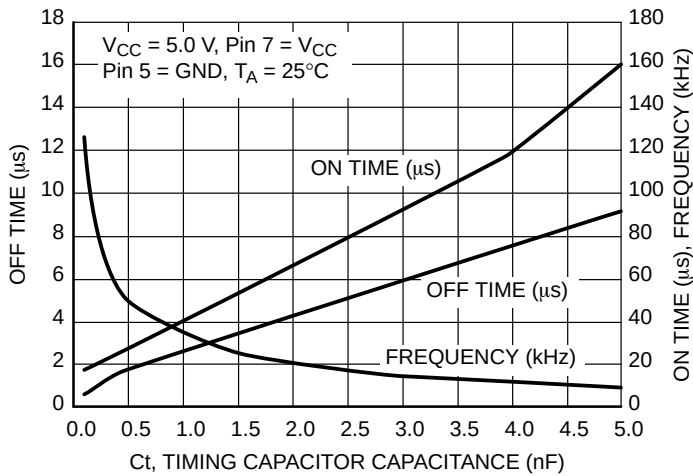


Figure 3. Oscillator Frequency

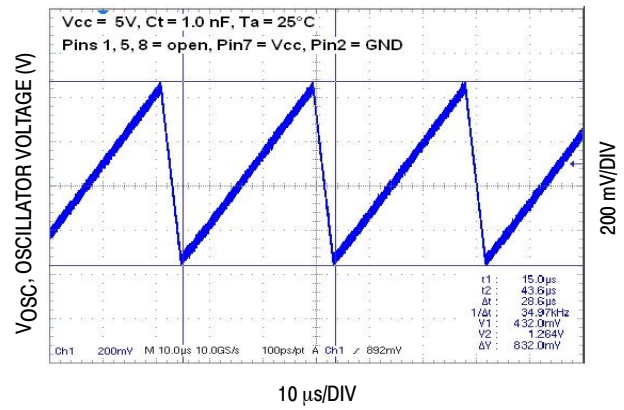


Figure 4. Timing Capacitor Waveform

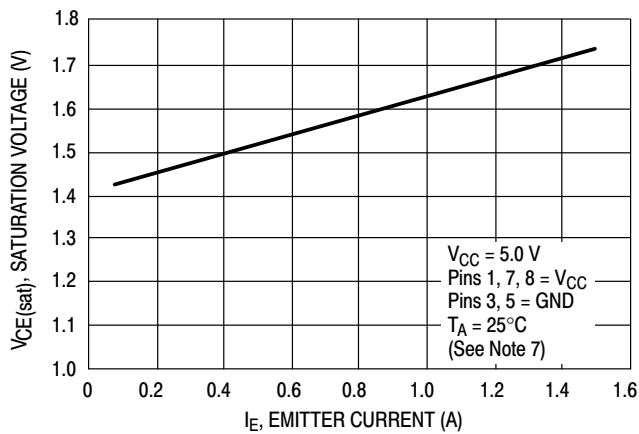


Figure 5. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

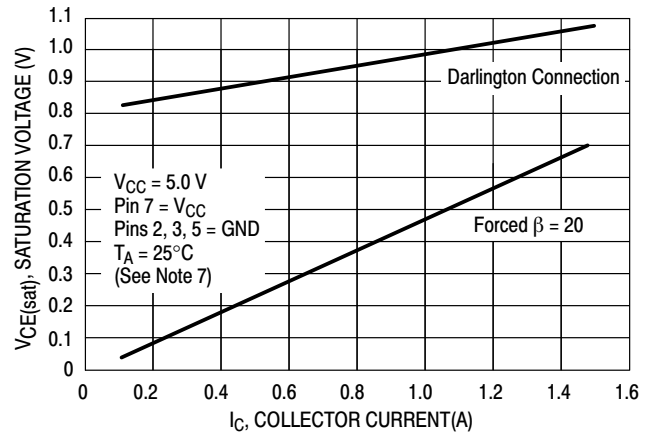


Figure 6. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

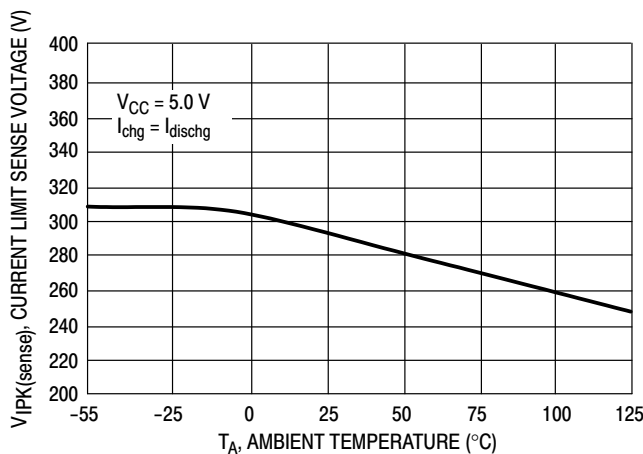


Figure 7. Current Limit Sense Voltage versus Temperature

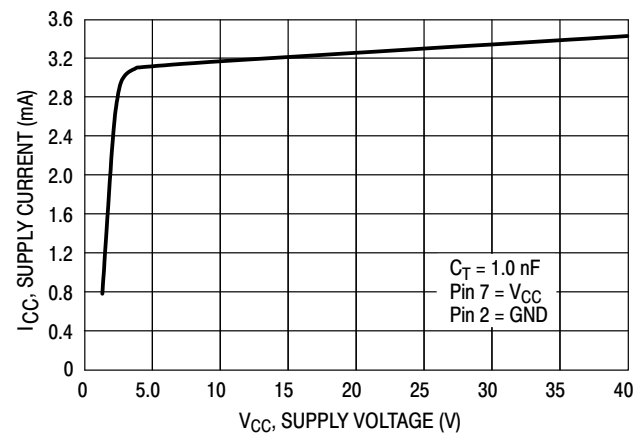
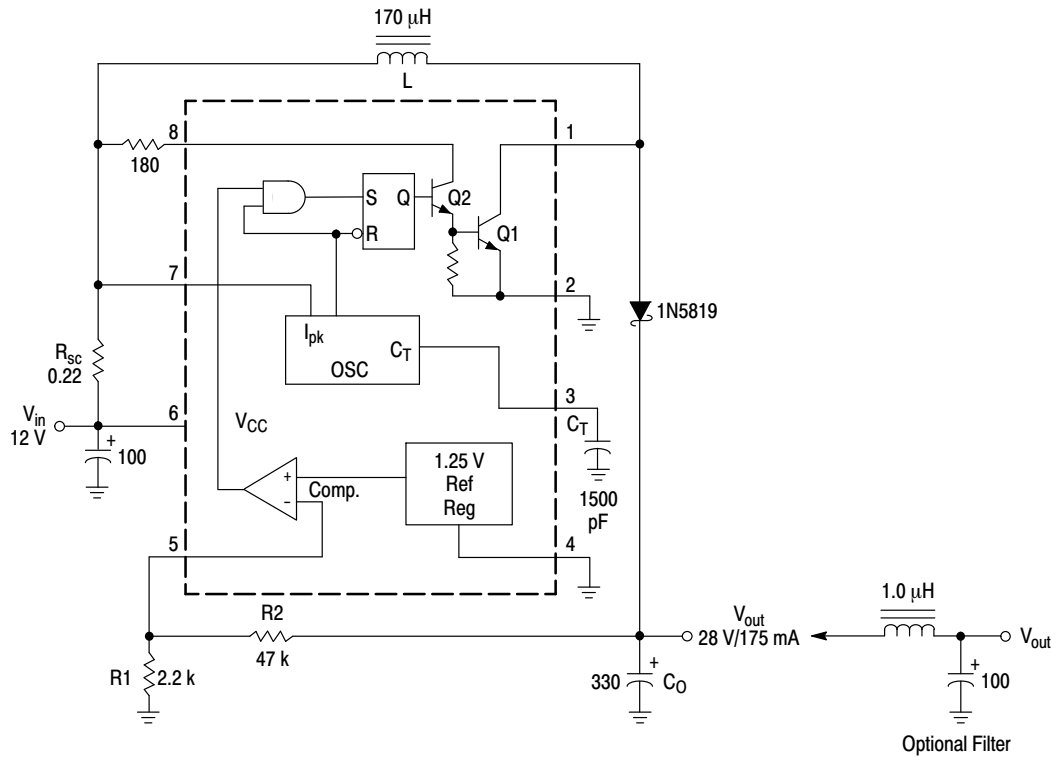


Figure 8. Standby Supply Current versus Supply Voltage

7. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

MC34063A, MC33063A, SC33063A, NCV33063A



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 16 \text{ V}$, $I_O = 175 \text{ mA}$	$30 \text{ mV} = \pm 0.05\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 75 \text{ mA to } 175 \text{ mA}$	$10 \text{ mV} = \pm 0.017\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 175 \text{ mA}$	400 mVpp
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 175 \text{ mA}$	87.7%
Output Ripple With Optional Filter	$V_{in} = 12 \text{ V}$, $I_O = 175 \text{ mA}$	40 mVpp

Figure 9. Step-Up Converter

MC34063A, MC33063A, SC33063A, NCV33063A

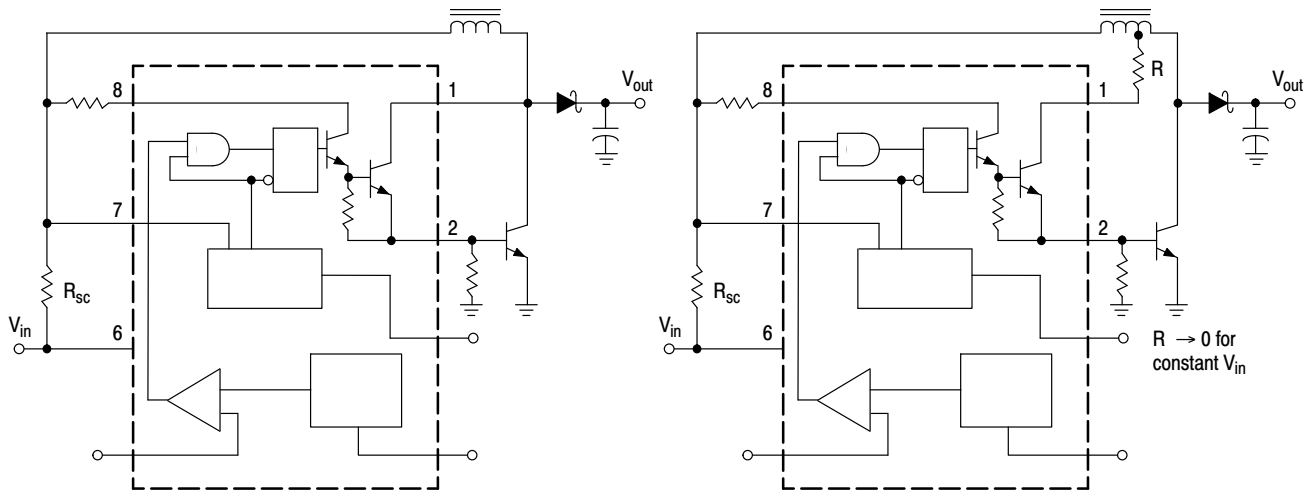


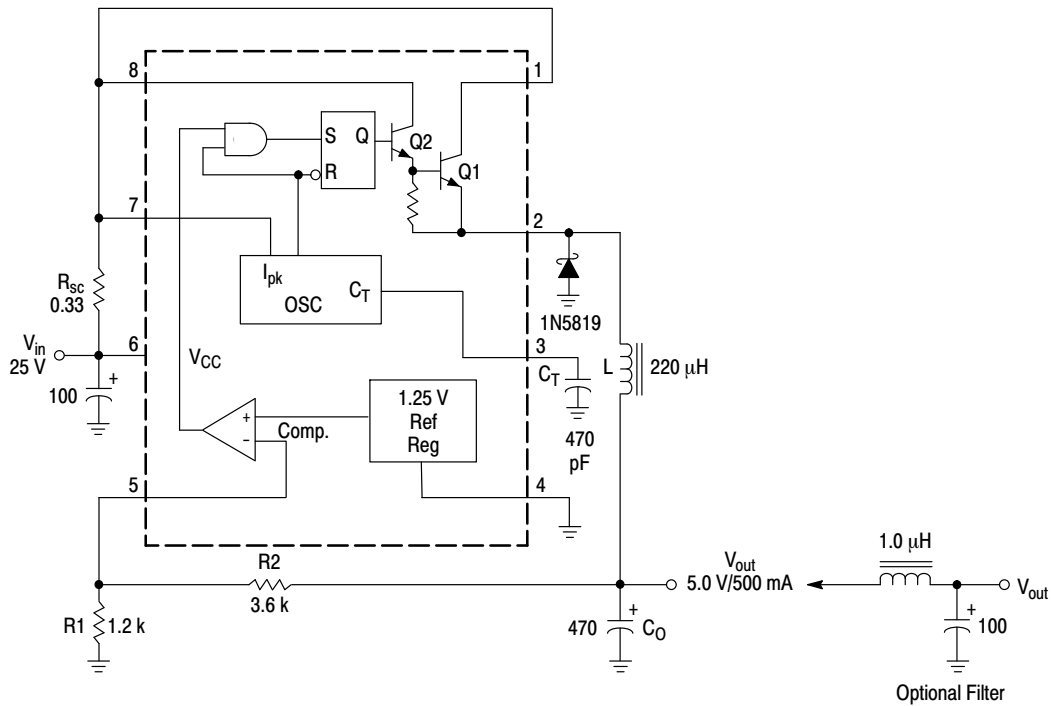
Figure 10. External Current Boost Connections for I_C Peak Greater than 1.5 A

9a. External NPN Switch

9b. External NPN Saturated Switch

(See Note 8)

8. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to $2.0 \mu\text{s}$ to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended.



Test	Conditions	Results
Line Regulation	$V_{in} = 15\text{ V to } 25\text{ V}$, $I_O = 500\text{ mA}$	$12\text{ mV} = \pm 0.12\%$
Load Regulation	$V_{in} = 25\text{ V}$, $I_O = 50\text{ mA to } 500\text{ mA}$	$3.0\text{ mV} = \pm 0.03\%$
Output Ripple	$V_{in} = 25\text{ V}$, $I_O = 500\text{ mA}$	120 mVpp
Short Circuit Current	$V_{in} = 25\text{ V}$, $R_L = 0.1\ \Omega$	1.1 A
Efficiency	$V_{in} = 25\text{ V}$, $I_O = 500\text{ mA}$	83.7%
Output Ripple With Optional Filter	$V_{in} = 25\text{ V}$, $I_O = 500\text{ mA}$	40 mVpp

Figure 11. Step-Down Converter

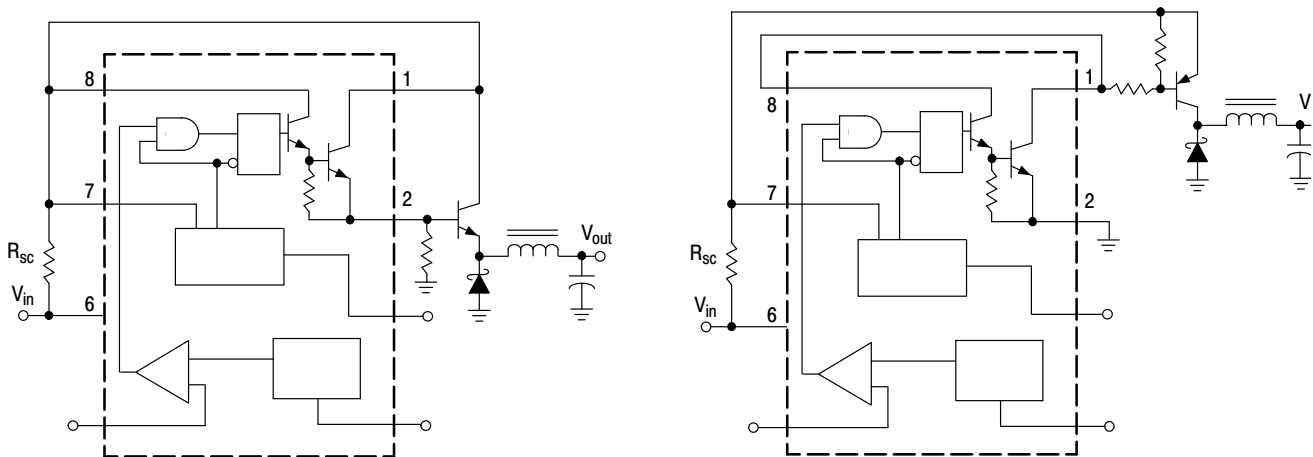
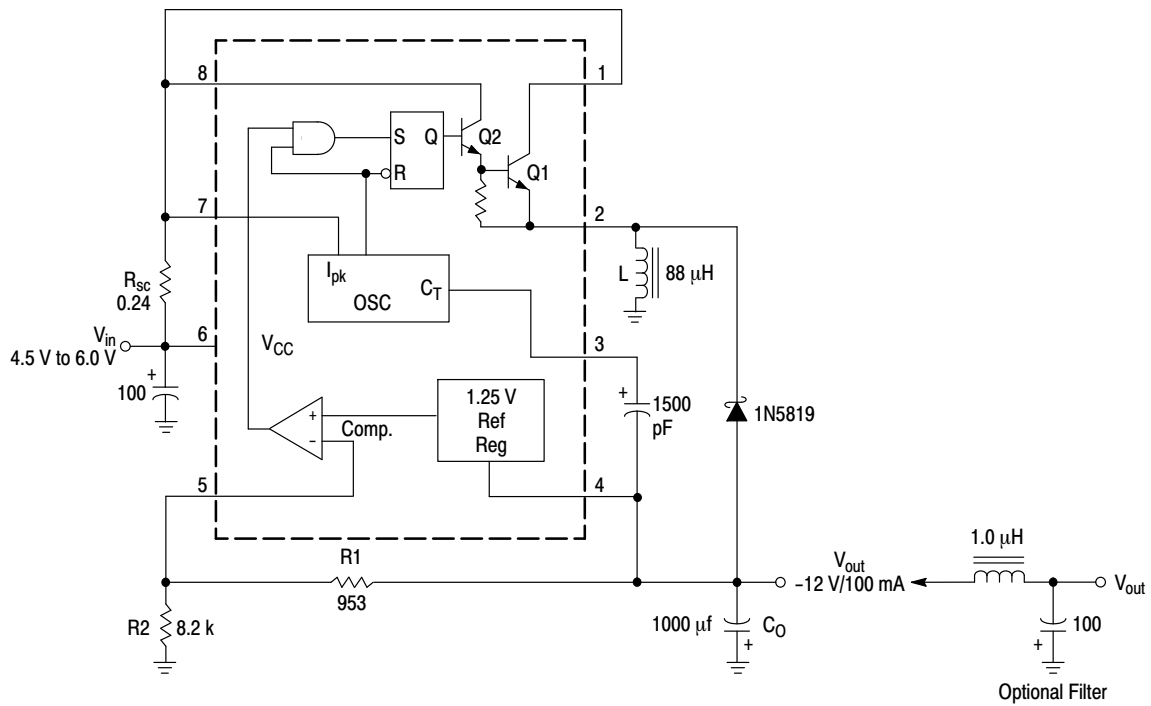


Figure 12. External Current Boost Connections for I_C Peak Greater than 1.5 A

11a. External NPN Switch

11b. External PNP Saturated Switch



Test	Conditions	Results
Line Regulation	$V_{in} = 4.5 \text{ V to } 6.0 \text{ V}$, $I_O = 100 \text{ mA}$	$3.0 \text{ mV} = \pm 0.012\%$
Load Regulation	$V_{in} = 5.0 \text{ V}$, $I_O = 10 \text{ mA to } 100 \text{ mA}$	$0.022 \text{ V} = \pm 0.09\%$
Output Ripple	$V_{in} = 5.0 \text{ V}$, $I_O = 100 \text{ mA}$	500 mVpp
Short Circuit Current	$V_{in} = 5.0 \text{ V}$, $R_L = 0.1 \Omega$	910 mA
Efficiency	$V_{in} = 5.0 \text{ V}$, $I_O = 100 \text{ mA}$	62.2%
Output Ripple With Optional Filter	$V_{in} = 5.0 \text{ V}$, $I_O = 100 \text{ mA}$	70 mVpp

Figure 13. Voltage Inverting Converter

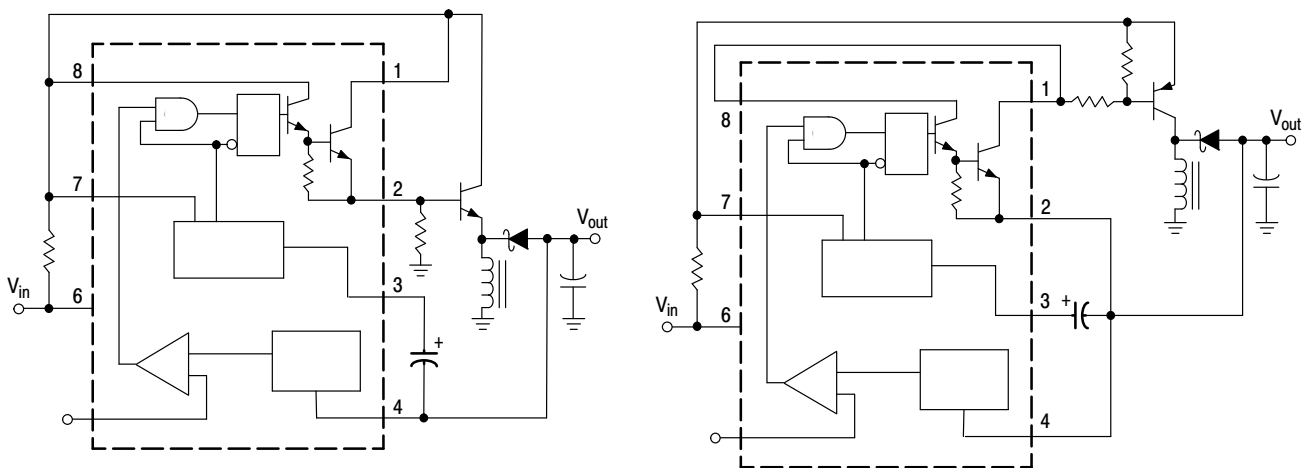
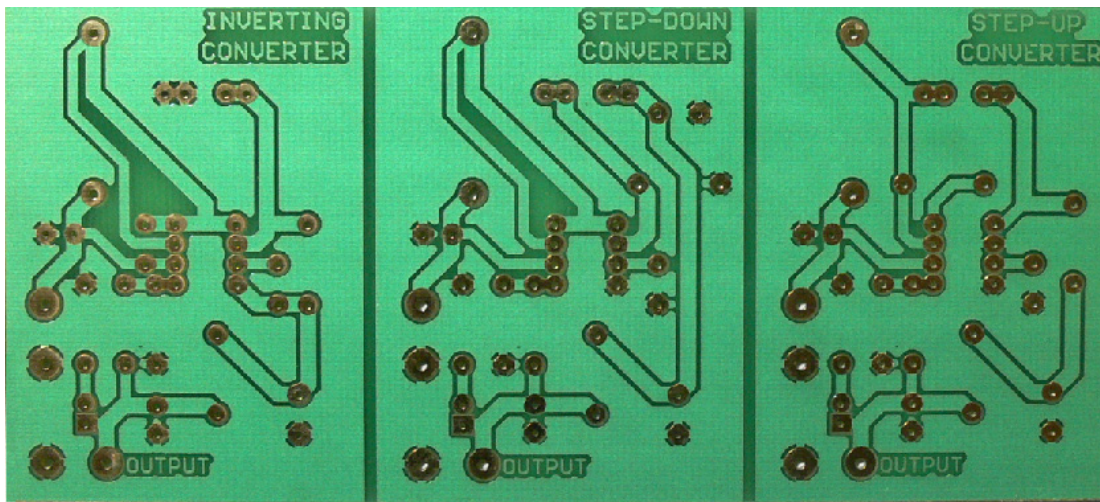


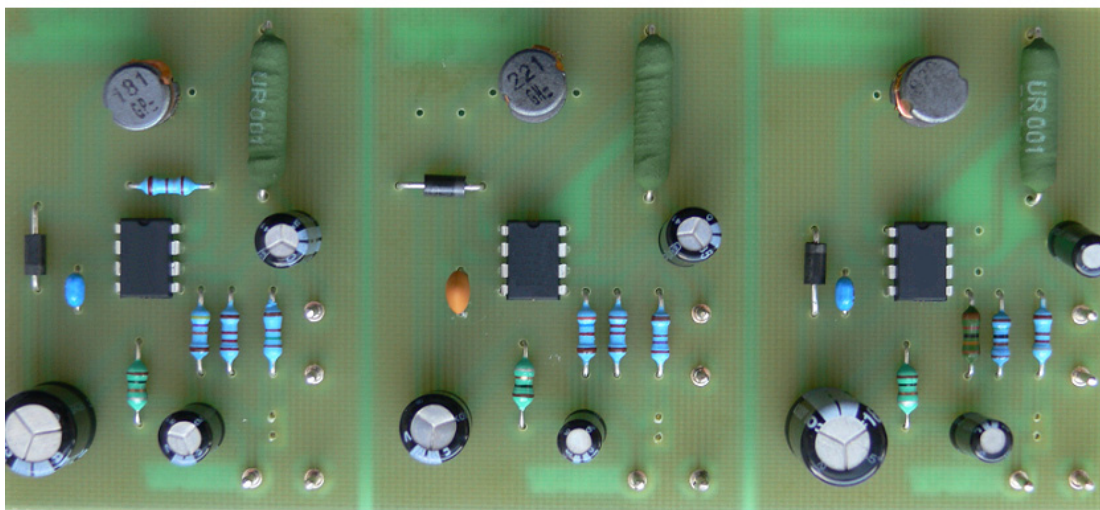
Figure 14. External Current Boost Connections for I_C Peak Greater than 1.5 A

13a. External NPN Switch

13b. External PNP Saturated Switch



(Bottom Side)



(Top View, Component Side)

Figure 15. Printed Circuit Board and Component Layout
(Circuits of Figures 9, 11, 13)

INDUCTOR DATA

Converter	Inductance (μH)	Turns/Wire
Step-Up	170	38 Turns of #22 AWG
Step-Down	220	48 Turns of #22 AWG
Voltage-Inverting	88	28 Turns of #22 AWG

All inductors are wound on Magnetics Inc. 55117 toroidal core.

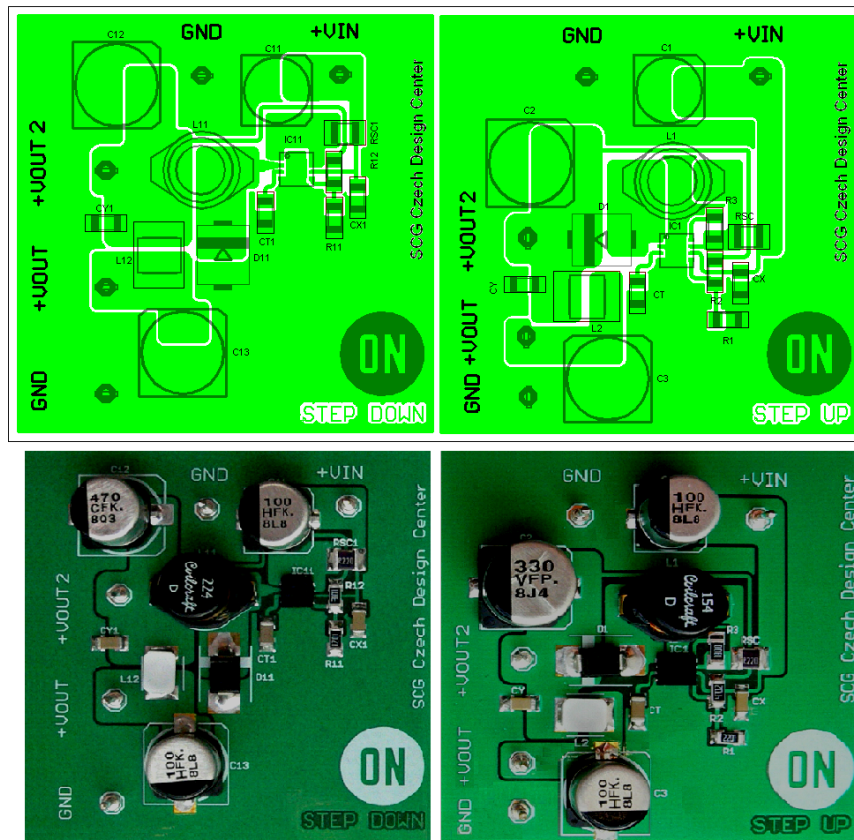


Figure 16. Printed Circuit Board for DFN Device

MC34063A, MC33063A, SC33063A, NCV33063A

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R_{sc}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}} \right) t_{on(max)}$
C_O	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.

V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage.

V_{out} – Desired output voltage, $|V_{out}| = 1.25 \left(1 + \frac{R_2}{R_1} \right)$

I_{out} – Desired output current.

f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_O .

$V_{ripple(pp)}$ – Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

NOTE: For further information refer to Application Note AN920A/D and AN954/D.

Figure 17. Design Formula Table

MC34063A, MC33063A, SC33063A, NCV33063A

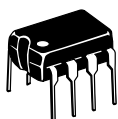
ORDERING INFORMATION

Device	Package	Shipping [†]
MC33063ADG	SOIC-8 (Pb-Free)	98 Units / Rail
MC33063ADR2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
SC33063ADR2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
MC33063AP1G	PDIP-8 (Pb-Free)	50 Units / Rail
MC33063AVDG	SOIC-8 (Pb-Free)	98 Units / Rail
MC33063AVDR2G	SOIC-8 (Pb-Free)	
NCV33063AVDR2G*	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
MC33063AVPG	PDIP-8 (Pb-Free)	50 Units / Rail
MC34063ADG	SOIC-8 (Pb-Free)	98 Units / Rail
MC34063ADR2G	SOIC-8 (Pb-Free)	2500 Units / Tape & Reel
MC34063AP1G	PDIP-8 (Pb-Free)	50 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NCV33063A: T_{low} = -40°C, T_{high} = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

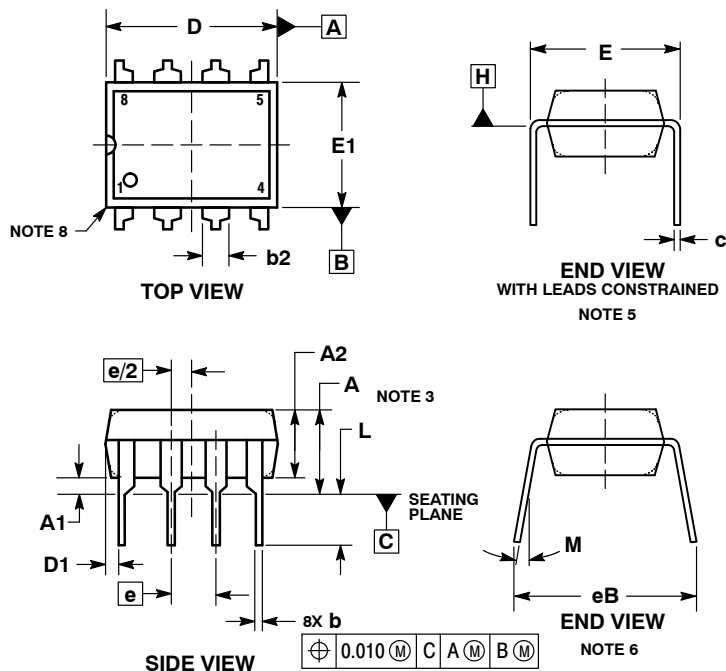
SENSEFET is a trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.



SCALE 1:1

PDIP-8
CASE 626-05
ISSUE P

DATE 22 APR 2015



STYLE 1:

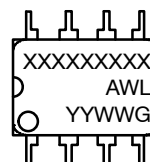
- PIN 1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.015	0.210	0.38	5.33
A1	0.015		0.38	
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005		0.13	
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB		0.430		10.92
L	0.115	0.150	2.92	3.81
M		10 ⁻³		10 ⁻³

GENERIC MARKING DIAGRAM*

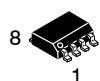


- XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP-8	PAGE 1 OF 1

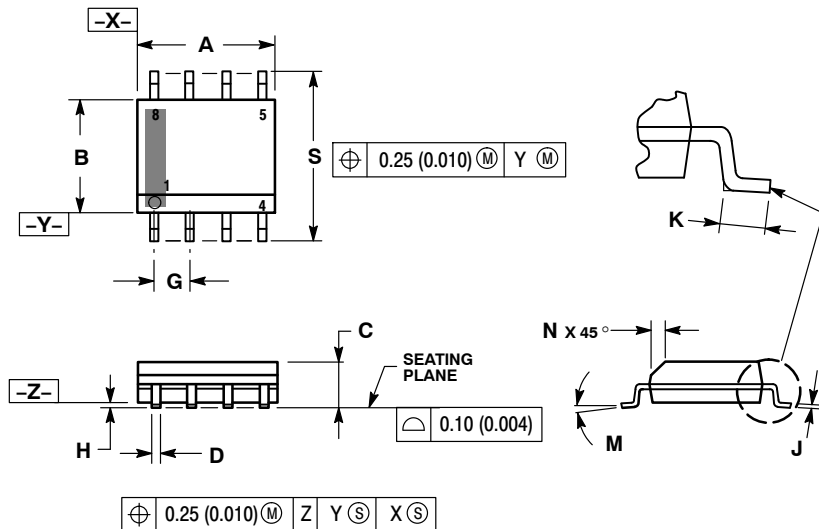
onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

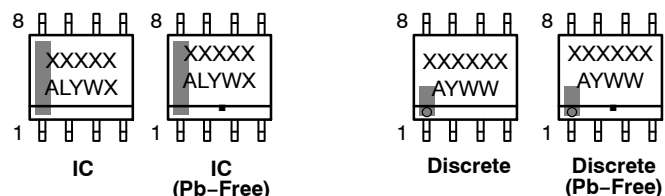
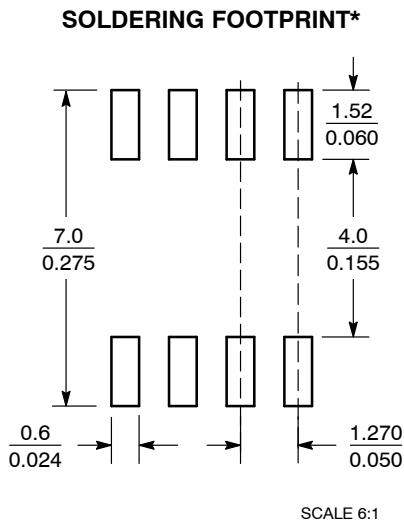


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales