

MOSFET – Power, Single N-Channel

40 V, 0.92 mΩ, 300 A

NVMFS5C410N

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C410NWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Value	Unit
Drain-to-Source Voltage			40	V
Gate-to-Source Voltage			±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25\text{ }^{\circ}\text{C}$	300	A
		$T_C = 100\text{ }^{\circ}\text{C}$	212	
Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 25\text{ }^{\circ}\text{C}$	166	W
		$T_C = 100\text{ }^{\circ}\text{C}$	83	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25\text{ }^{\circ}\text{C}$	46	A
		$T_A = 100\text{ }^{\circ}\text{C}$	32	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_A = 25\text{ }^{\circ}\text{C}$	3.9	W
		$T_A = 100^{\circ}\text{C}$	1.9	
Pulsed Drain Current	$T_A = 25\text{ }^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$		900	A
Operating Junction and Storage Temperature Range			−55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)			158	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 34\text{ A}$)			578	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			260	$^{\circ}\text{C}$

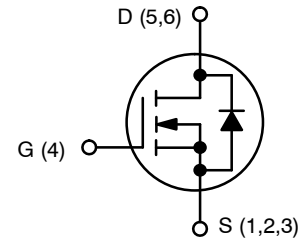
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

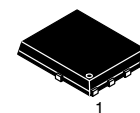
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	0.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	0.92 mΩ @ 10 V	300 A

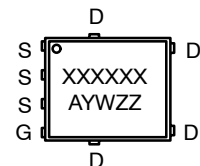


N-CHANNEL MOSFET



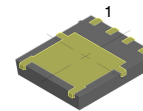
DFN5
(SO-8FL)
CASE 488AA
STYLE 1

MARKING DIAGRAMS



XXXXXX = 5C410N
(NVMFS5C410N) or
410NWF
(NVMFS5C410NWF)

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability



DFNW5
(SO-8FL WF)
CASE 507BA



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

NVMFS5C410N

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			5		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25\text{ }^{\circ}\text{C}$		10	μA
			$T_J = 125\text{ }^{\circ}\text{C}$		100	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.5		3.5	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient			-8.6		mV/ $^{\circ}\text{C}$
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		0.76	0.92	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 50\text{ A}$		190		S

CHARGES, CAPACITANCES & GATE RESISTANCE

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$		6100		pF
C_{OSS}	Output Capacitance			3400		
C_{RSS}	Reverse Transfer Capacitance			70		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}; I_D = 50\text{ A}$		86		nC
$Q_{G(TH)}$	Threshold Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}; I_D = 50\text{ A}$		18		
Q_{GS}	Gate-to-Source Charge			28		
Q_{GD}	Gate-to-Drain Charge			14		
V_{GP}	Plateau Voltage			4.9		V

SWITCHING CHARACTERISTICS (Note 5)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}, I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$		54		ns
t_r	Rise Time			162		
$t_{d(OFF)}$	Turn-Off Delay Time			227		
t_f	Fall Time			173		

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 50 A	T _J = 25 °C		0.8	1.2	V
			T _J = 125 °C		0.65		
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A			91		ns
t _a	Charge Time				42		
t _b	Discharge Time				49		
Q _{RR}	Reverse Recovery Charge				159		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

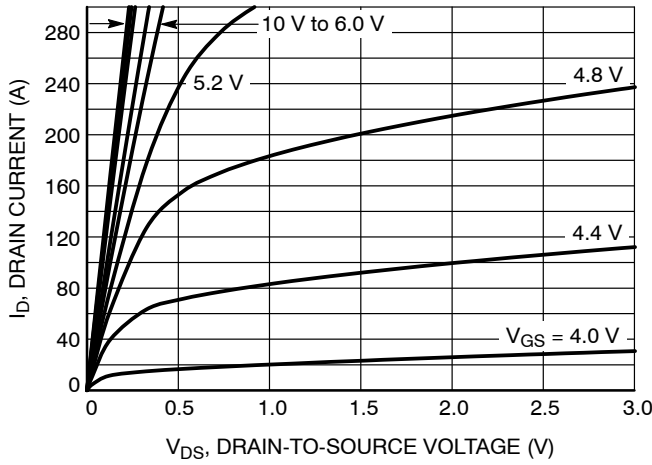


Figure 1. On-Region Characteristics

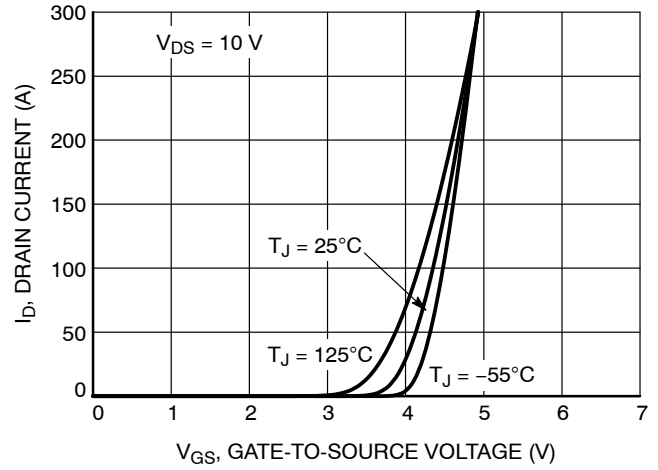


Figure 2. Transfer Characteristics

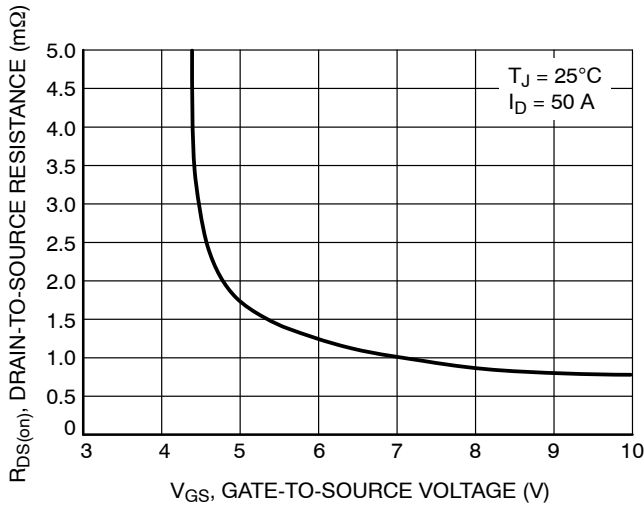


Figure 3. On-Resistance vs. Gate-to-Source Voltage

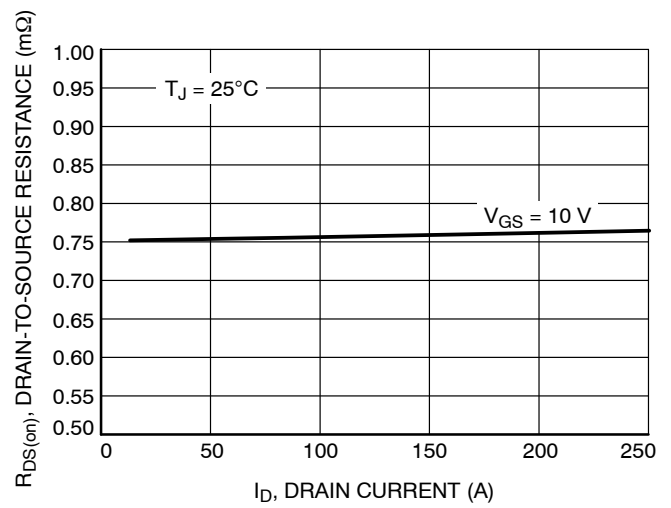


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

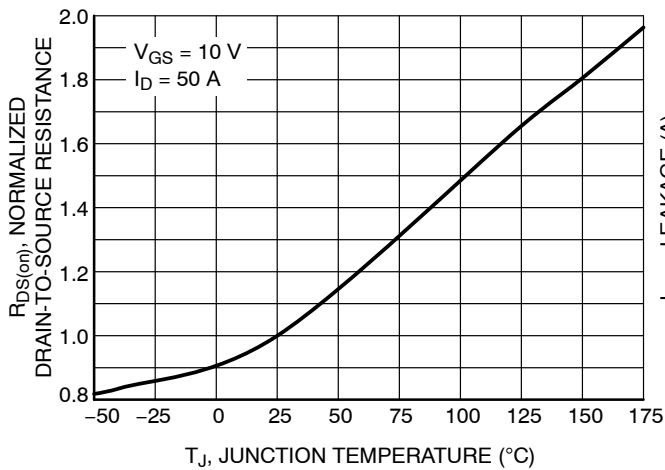


Figure 5. On-Resistance Variation with Temperature

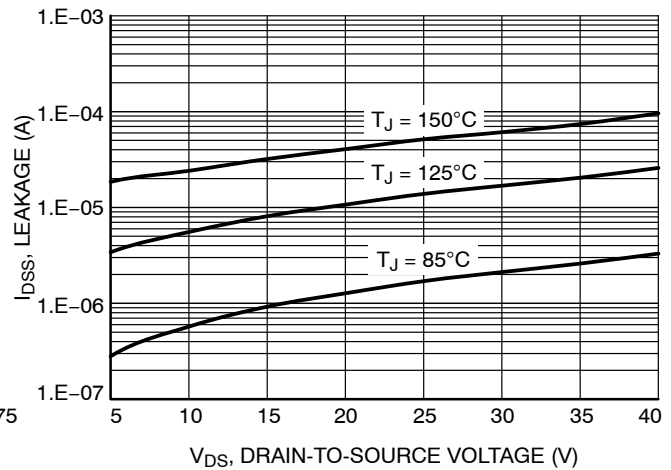


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

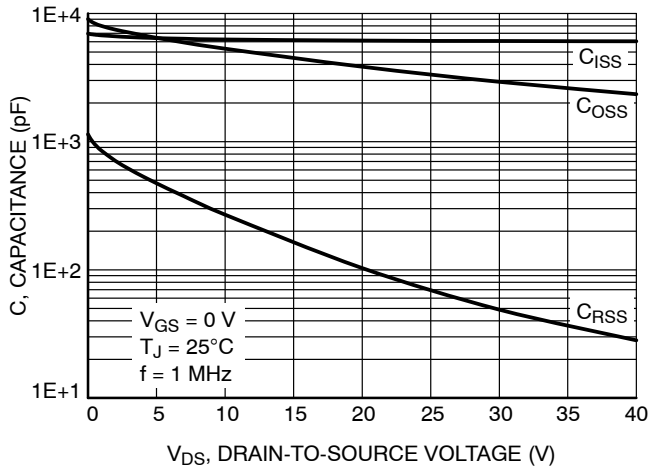


Figure 7. Capacitance Variation

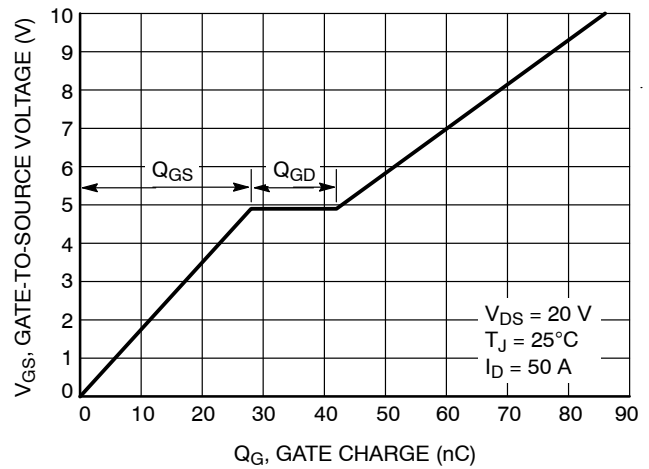


Figure 8. Gate-to-Source Voltage vs. Charge

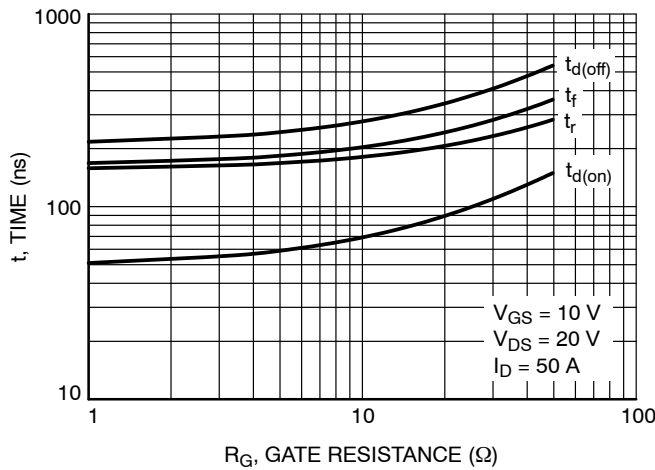


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

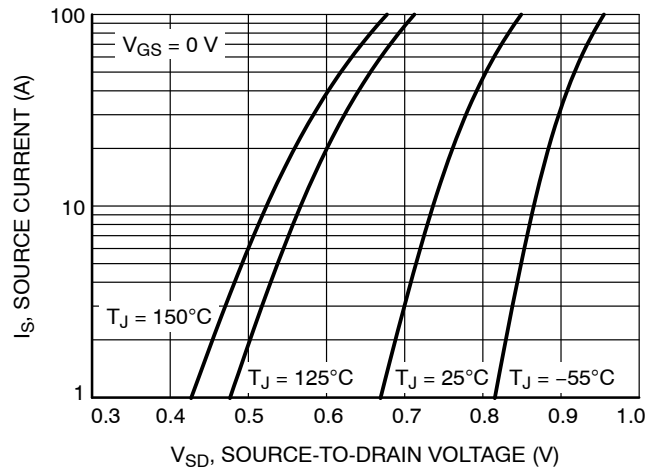


Figure 10. Diode Forward Voltage vs. Current

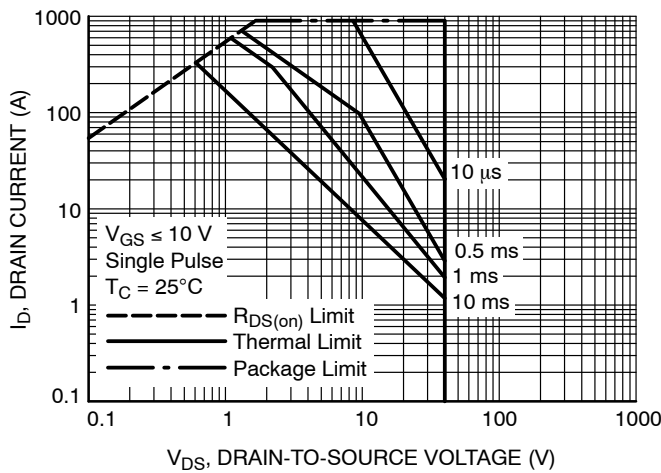


Figure 11. Maximum Rated Forward Biased Safe Operating Area

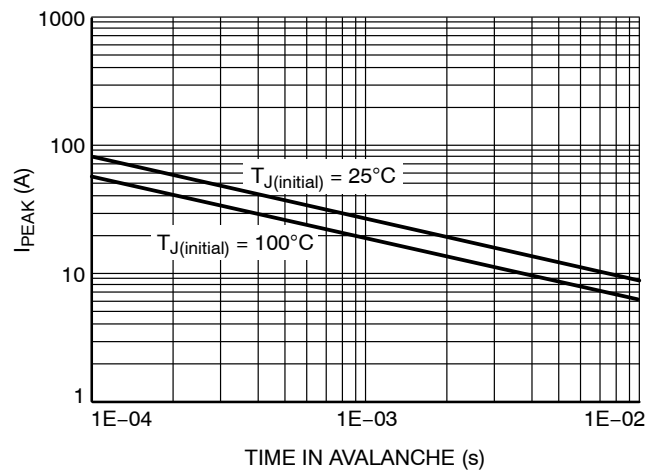


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMFS5C410N

TYPICAL CHARACTERISTICS (continued)

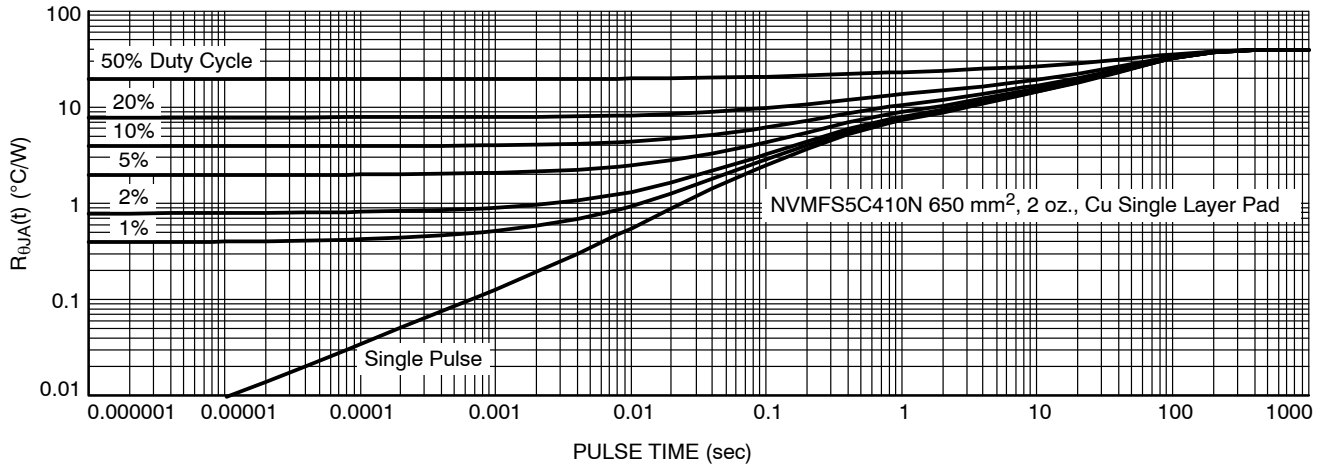


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS5C410NWF1G	410NWF	DFNW5 (Pb-Free, Wettable Flanks)	1,500 / Tape & Reel
NVMFS5C410NAFT1G	5C410N	DFN5 (Pb-Free)	1,500 / Tape & Reel
NVMFS5C410NWFA1G	410NWF	DFNW5 (Pb-Free, Wettable Flanks)	1,500 / Tape & Reel
NVMFS5C410NWFET1G	410NWF	DFNW5 (Pb-Free, Wettable Flanks)	1,500 / Tape & Reel

DISCONTINUED (Note 6)

NVMFS5C410NT1G	5C410N	DFN5 (Pb-Free)	1,500 / Tape & Reel
NVMFS5C410NWF3G	410NWF	DFNW5 (Pb-Free, Wettable Flanks)	5,000 / Tape & Reel
NVMFS5C410NT3G	5C410N	DFN5 (Pb-Free)	5,000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

6. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

NVMFS5C410N

REVISION HISTORY

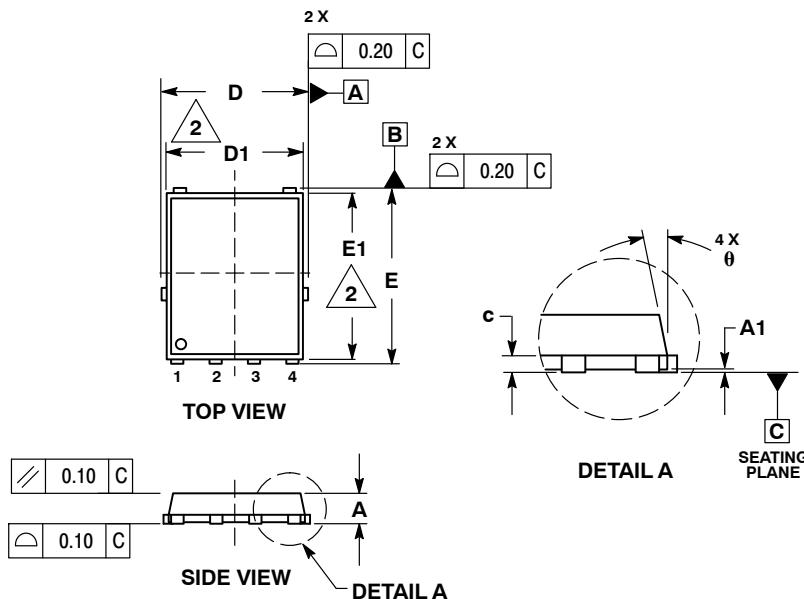
Revision	Description of Changes	Date
8	Update wettable flank package to DFNW5 in device ordering information.	06/19/2025
9	NVMFS5C410NT1G OPN Marked as Discontinued.	07/14/2025



SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC
MARKING DIAGRAM*


XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

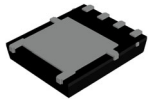
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

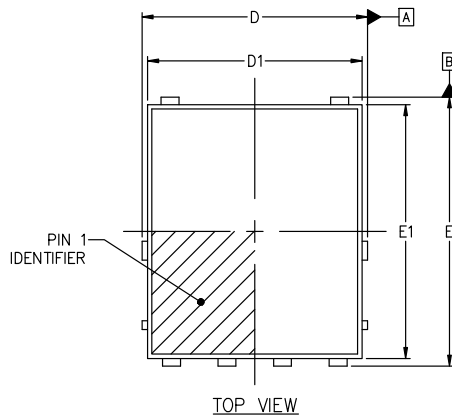
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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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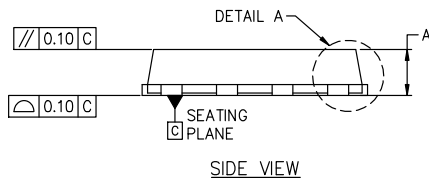


DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C

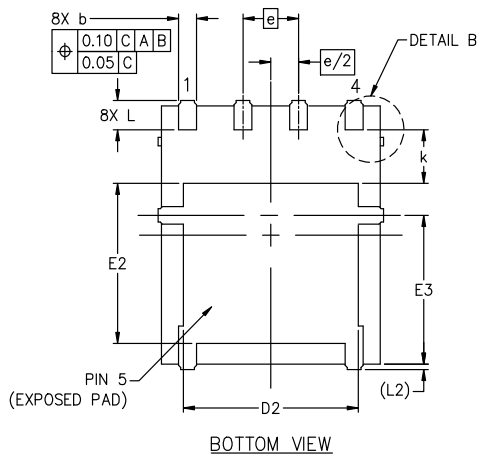
DATE 19 SEP 2024



TOP VIEW



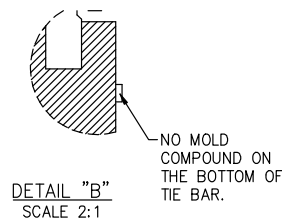
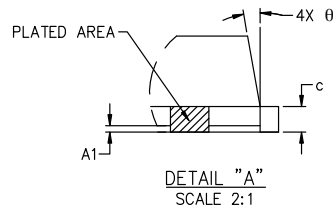
SIDE VIEW



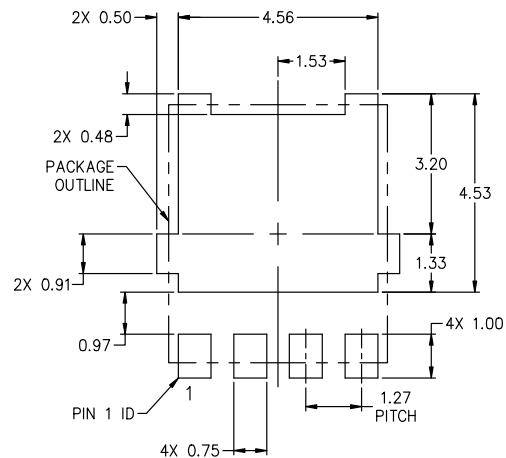
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DFNW5 4.90x5.90x1.00, 1.27P	PAGE 1 OF 1

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