

Preliminary Technical Data

AD5259

FEATURES

- Nonvolatile memory maintains wiper settings
- 256-position
- Compact MSOP-10 (3 mm × 4.9 mm) package
- I²C[®] compatible interface
- V_{LOGIC} pin provides increased interface flexibility.
- End-to-end resistance 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
- Resistance tolerance stored in EEMEM (0.1% accuracy)
- Power On EEMEM Refresh Time < 1ms
- Software write protect command
- Tri-state address decode pins AD0 and AD1
- 100-year typical data retention at 55°C
- Wide operating temperature –40°C to +85°C
- +3V to +5V single-supply

APPLICATIONS

- LCD panel V_{COM} adjustment
- LCD panel brightness and contrast control
- Mechanical potentiometer replacement in new designs
- Programmable power supplies
- RF amplifier biasing
- Automotive electronics adjustment
- Gain control and offset adjustment
- Low resolution DAC replacement
- Electronics level settings

GENERAL OVERVIEW

The AD5259 provides a compact nonvolatile 3 mm × 4.9 mm packaged solution for 256-position adjustment applications. These devices perform the same electronic adjustment function as mechanical potentiometers or variable resistors, with enhanced resolution and solid-state reliability.

The wiper settings are controllable through an I²C compatible digital interface, which can also be used to read back the wiper register and EEMEM content. Resistor tolerance is also stored within EEMEM and can be used to provide an end-to-end tolerance accuracy of 0.1%. In order to provide added security, command bits are available to place the part into a write protect mode in which data can not be written to the EEMEM register.

In addition, a separate V_{LOGIC} pin provides the user with increased interface flexibility. For users who need multiple

parts on one bus, address bits AD0 and AD1 allow up to nine devices on the same bus.

FUNCTIONAL BLOCK DIAGRAMS

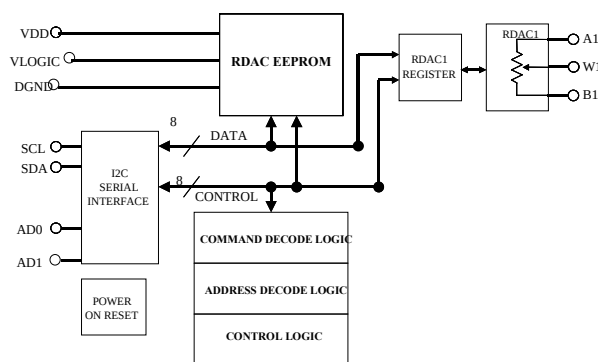


Figure 1.

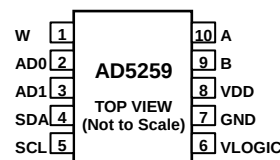


Figure 3. Pinout.

Note:

The terms *digital potentiometer*, *VR*, and *RDAC* are used interchangeably.

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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REVISION HISTORY

Revision 0: Initial Version

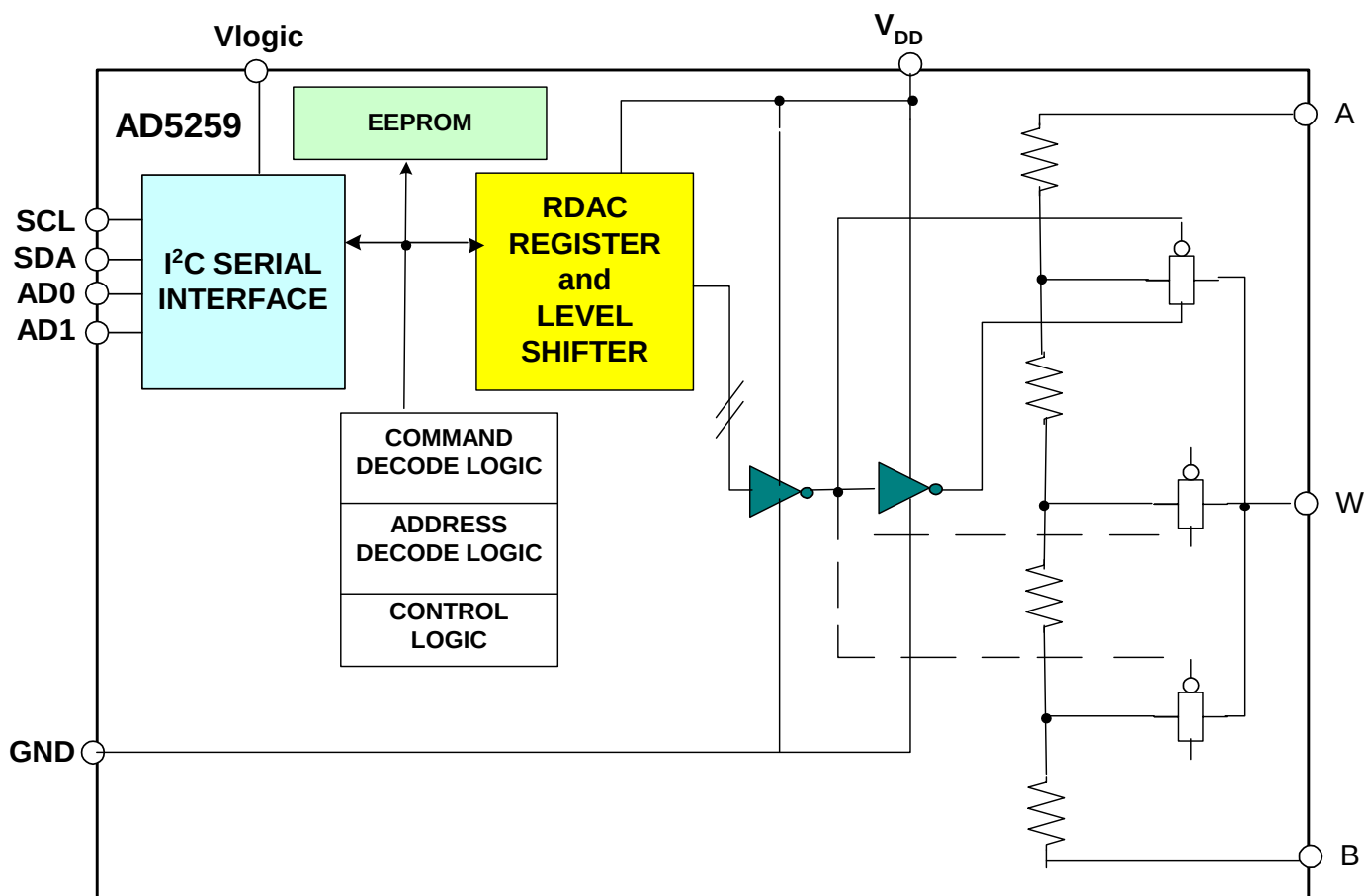


Figure 3. Block diagram showing level shifters

ELECTRICAL CHARACTERISTICS—5 k Ω , 10 k Ω , 50 k Ω , 100 k Ω VERSIONS(V_{DD} = 5 V $\pm$ 10%, or 3 V $\pm$ 10%; V_A = V_{DD}; V_B = 0 V; -40°C < T_A < +85°C; unless otherwise noted.)

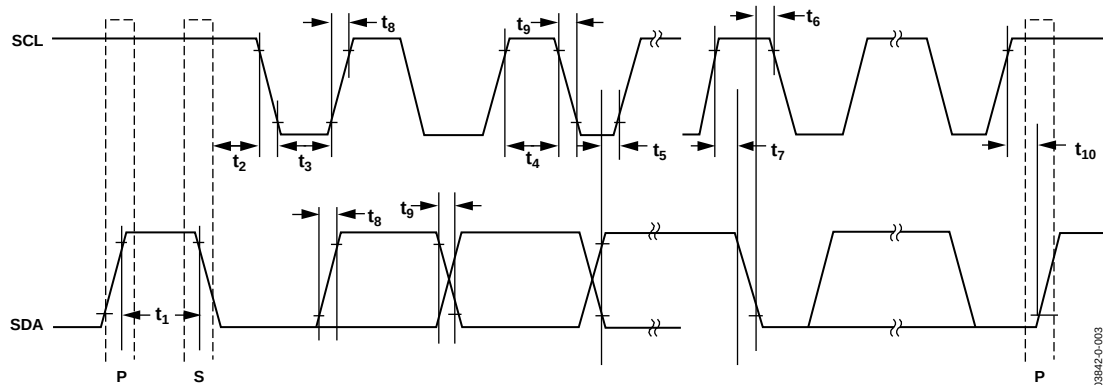
Table 1.

Parameter	Symbol	Conditions	Min		Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity	R-DNL	R _{WB} , V _A = no connect	-1	± 0.1	+1	LSB
Resistor Integral Nonlinearity	R-INL	R _{WB} , V _A = no connect	-2	± 0.25	+2	LSB
Nominal Resistor Tolerance	ΔR_{AB}	T _A = 25°C	-30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V _{AB} = V _{DD} , Wiper = no connect		650		ppm/°C
R _{WB}	R _{WB}	Code = 0x00		50	120	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity	DNL		-1	± 0.1	+1	LSB
Integral Nonlinearity	INL		-1	± 0.3	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		30		ppm/°C
Full-Scale Error	V _{WFSE}	Code = 0xFF	-3	-1	0	LSB
Zero-Scale Error	V _{WZSE}	Code = 0x00	0	1	3	LSB
RESISTOR TERMINALS						
Voltage Range	V _{A,B,W}		V _{SS}		V _{DD}	V
Capacitance A, B	C _{A,B}	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance W	C _W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Common-Mode Leakage	I _{CM}	V _A = V _B = V _{DD} /2		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V _{IH}		0.7 $\times$ V _L		V _L +0.5	V
Input Logic Low	V _{IL}		-0.5		0.3 $\times$ V _L	V
Input Current	I _{IL}	V _{IN} = 0 V or 5 V			± 1	μ A
Input Capacitance	C _{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V _{DD}		2.7		5.5	V
Positive Supply Current	I _{DD}	V _{IH} = 5 V or V _{IL} = 0 V			1	μ A
Logic Supply(must match logic levels)	V _{LOGIC}		2.7		V _{DD}	
Programming Mode Current(EEMEM)	I _{LOGIC(PROG)}	V _{IH} = 5 V or V _{IL} = 0 V		35		mA
Power Dissipation	P _{DISS}	V _{IH} = 5 V or V _{IL} = 0 V, V _{DD} = 5 V		18	50	μ W
Power Supply Sensitivity	PSS	V _{DD} = +5 V $\pm$ 10%, Code = Midscale		± 0.02	± 0.05	%/%
DYNAMIC CHARACTERISTICS						
Bandwidth -3dB	BW	R _{AB} = 5k Ω / 10 k Ω /50 k Ω /100 k Ω , Code = 0x80		2000/600/ 100/40		kHz
Total Harmonic Distortion	THD _W	V _A = 1 V rms, V _B = 0 V, f = 1 kHz, R _{AB} = 10 k Ω		0.1		%
V _W Settling Time (1k Ω /10 k Ω /50 k Ω /100 k Ω)	t _S	V _A = 5 V, V _B = 0 V, ± 1 LSB error band		2		μ s
Resistor Noise Voltage Density	e _{N_WB}	R _{WB} = 5 k Ω , R _S = 0		9		nV/ $\sqrt$ Hz

TIMING CHARACTERISTICS—5 k Ω , 10 k Ω , 50 k Ω , 100 k Ω VERSIONS(V_{DD} = +5V $\pm$ 10%, or +3V $\pm$ 10%; V_A = V_{DD}; V_B = 0 V; -40°C < T_A < +85°C; unless otherwise noted.)

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I ² C INTERFACE TIMING CHARACTERISTICS ¹ (Specifications Apply to All Parts)						
SCL Clock Frequency	f _{SCL}	After this period, the first clock pulse is generated.	0		400	kHz
t _{BUF} Bus Free Time between STOP and START	t ₁		1.3			μ s
t _{HD;STA} Hold Time (Repeated START)	t ₂		0.6			μ s
t _{LOW} Low Period of SCL Clock	t ₃		1.3			μ s
t _{HIGH} High Period of SCL Clock	t ₄		0.6			μ s
t _{SU;STA} Setup Time for Repeated START Condition	t ₅		0.6			μ s
t _{HD;DAT} Data Hold Time	t ₆		0	0.9		μ s
t _{SU;DAT} Data Setup Time	t ₇		100			ns
t _F Fall Time of Both SDA and SCL Signals	t ₈				300	ns
t _R Rise Time of Both SDA and SCL Signals	t ₉				300	ns
t _{SU;STO} Setup Time for STOP Condition	t ₁₀		0.6			μ s

Figure 4. I²C Interface Timing Diagram

I²C INTERFACE

Table 3. Generic Interface Format

S	Device Address* (7-bit)	R/ $\overline{W}$	SA	C2	C1	C0	A4	A3	A2	A1	A0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte				Instruction Byte									Data Byte								

Table 4. Device Address Lookup*

(Note that AD1 and AD0 are tri-state address pins)

Device Address	AD1	AD0
0011000	0	0
0011001	NC	0
0011010	1	0
0101001	0	NC
0101010	NC	NC
0101011	1	NC
1001100	0	1
1001101	NC	1
1001110	1	1

S = Start Condition

P = Stop Condition

SA = Slave Acknowledge

MA = Master Acknowledge

NA = No Acknowledge

X = Don't Care

$\overline{W}$ = Write

R = Read

Table 5. RDAC-to-EEMEM Interface Command Descriptions

C2	C1	C0	Command Description
0	0	0	Operation between I ² C and RDAC
0	0	1	Operation between I ² C and EEPROM
0	1	0	Operation between I ² C and WP register
1	0	0	NOP
1	0	1	Restore EEPROM to RDAC
1	1	0	Store RDAC to EEPROM

Write Modes

Table 6. Writing to RDAC register

S	Device Address* (7-bit)	0	SA	0	0	0	0	0	0	0	0	0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte				Instruction Byte										Data Byte								

Table 7. Writing to EEPROM register

S	Device Address* (7-bit)	0	SA	0	0	1	0	0	0	0	0	0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte				Instruction Byte										Data Byte								

Table 8. Activating Software Write Protect

S	Device Address* (7-bit)	0	SA	0	1	0	0	0	0	0	0	0	SA	0	0	0	0	0	0	0	WP	SA	P
	Slave Address Byte				Instruction Byte										Data Byte								

Store/Restore Modes

Table 9. Storing RDAC value to EEPROM

S	Device Address* (7-bit)	0	SA	1	1	0	0	0	0	0	0	0	SA	P
	Slave Address Byte				Instruction Byte									

Table 10. Restoring EEPROM to RDAC

S	Device Address* (7-bit)	0	SA	1	0	1	0	0	0	0	0	0	SA	P
	Slave Address Byte				Instruction Byte									

S = Start Condition

P = Stop Condition

SA = Slave Acknowledge

MA = Master Acknowledge

NA = No Acknowledge

X = Don't Care

$\overline{W}$ = Write

R = Read

Read Modes

Table 11. Traditional Read back of RDAC Register value

C																																																	
S	Device Address* (7-bit)												0	SA	0	0	0	0	0	0	0	0	0	SA	S	Device Address* (7-bit)												1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte					Instruction Byte										Slave Address Byte					Read Back Data																												



Repeat start

Table 12. Traditional Read back of stored EEPROM value

S	Device Address* (7-bit)	0	SA	0	0	1	0	0	0	0	0	SA	S	Device Address* (7-bit)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P	
	Slave Address Byte			Instruction Byte											Slave Address Byte			Read Back Data									



Repeat start

Table 13. Traditional Read back of Tolerance

i. Consecutively

S	Device Address* (7-bit)	0	SA	0	0	1	1	1	1	1	0	SA	S	Device Address* (7-bit)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	MA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte			Instruction Byte										Slave Address Byte		Sign + Integer Byte									Decimal Byte										



Repeat start

ii. Individually

S	Device Address* (7-bit)	0	SA	0	0	1	1	1	1	1	0	SA	S	Device Address* (7-bit)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA		P
	Slave Address Byte																										



Repeat start

S	Device Address* (7-bit)	0	SA	0	0	1	1	1	1	1	1	SA	S	Device Address* (7-bit)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA		P
	Slave Address Byte																										



Repeat start

Note: Read modes above are referred to as traditional because the first two bytes for all three cases are “dummy” bytes which function to place the pointer towards the correct register. This is the reason for the Repeat Start. In theory, this step can be avoided if the user is interested in reading a register that was previously written to. For example, if the EEPROM was just written to, then the user can skip the

two dummy bytes and proceed directly to the “Slave Address Byte” which would be followed by the “Read Back Data”.

Calculating R_{AB} Tolerance Stored in Read-Only Memory

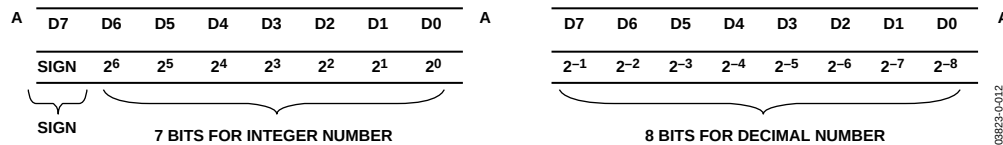


Figure 5. Format of Stored Tolerance in Sign Magnitude Format with Bit Position Descriptions. (Unit is percent. Only data bytes are shown.)

The AD5259 features a patented R_{AB} tolerance storage in the nonvolatile memory. The tolerance is stored in the memory during factory production and can be read by users at any time. The knowledge of stored tolerance allows users to calculate R_{AB} accurately. This feature is valuable for precision, rheostat mode, and open-loop applications where knowledge of absolute resistance is critical.

The stored tolerance resides in the read-only memory, and is expressed as a percentage. The tolerance is stored in two memory locations in sign magnitude binary form (see Figure 5). The two EEMEM address bytes are 11110 (sign+integer) and 11111 (decimal number). The two bytes can be accessed individually in two separate commands (see Table 13ii). Alternatively, in order to allow read back of the first byte followed by the second byte in one command (see Table 13i), the memory pointer will automatically increment from the first to the second EEMEM locations (increments from 11110 to 11111) if read consecutively.

In the first memory location, the MSB is designated for the sign (0 = + and 1 = -) and the 7 LSBs are designated for the integer portion of the tolerance. In the second memory location, all eight data bits are designated for the decimal portion of tolerance. For example, if the rated $R_{AB} = 10 \text{ k}\Omega$ and the data readback from Address 11110 shows 0001 1100 and Address 11111 shows 0000 1111, then the tolerance can be calculated as

MSB: 0 = +

Next 7 MSB: 001 1100 = 28

8 LSB: 0000 1111 = $15 \times 2^{-8} = 0.06$

Tolerance = +28.06% and therefore

$R_{AB_ACTUAL} = 12.806 \text{ k}\Omega$

EEMEM Write-Acknowledge Polling

After each write operation to the EEMEM registers, an internal write cycle begins. The I²C interface of the device is disabled. To determine if the internal write cycle is complete and the I²C interface is enabled, interface polling can be executed. I²C interface polling can be conducted by sending a start condition followed by the slave address + the write bit. If the I²C interface responds with an ACK, the write cycle is complete and the interface is ready to proceed with further operations. Other-wise, I²C interface polling can be repeated until it succeeds.

I²C COMPATIBLE 2-WIRE SERIAL BUS

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 4). The following byte is the Slave Address Byte, which consists of the slave address followed by an R/W bit (this bit determines whether data is read from or written to the slave device).

The AD5259 has two tri-state configurable address bits, AD0 and AD1 (see Table 4). The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/W bit is high, the master reads from the slave device. If the R/W bit is low, the master writes to the slave device.

2. **Writing:** In the write mode, the last bit(R/W) of the Address Byte is logic low. The second byte is the Instruction Byte. The first 3 bits of the Instruction Byte are the command bits(see Table 5). The final 5 bits indicate which EEMEM location the pointer moves to. The user must choose whether to write to the RDAC register, EEMEM register, or activate the software write protect(see Tables 6-8).

The final byte is the Data Byte MSB first. In the case of the write protect mode, data is not being stored. Rather, a logic high in the LSB will enable write protect and a logic low will disable write protect.

3. **Storing/Restoring:** In this mode, only two bytes are necessary; Address and Instruction Bytes. The last bit (R/W) of the Address Byte is logic low. The first 3 bits of the Instruction Byte are the command bits(see Table 5). The two choices are transfer data from RDAC to EEMEM(Store) or from EEMEM to RDAC(Restore). The final 5 bits are all zeros(see Tables 9-10).

4. **Reading:** Assuming the register of interest was not just written to, it is necessary to write a dummy Address and Instruction Byte. The Instruction Byte will vary depending on whether the data that is wanted is the RDAC register, EEMEM register, or Tolerance register(see Tables 11-13). The Tolerance register can be read back consecutively(Table 13i) or individually(Table 13ii). Refer to page 8 for detailed information on the interpretation of the tolerance bytes. After the dummy Address and Instruction Bytes are sent, a repeat start is necessary. After the repeat start, another Address Byte is needed except this time, the R/W bit is logic **high**. Following this Address Byte is the Read Back Byte containing the information requested in the Instruction Byte.
5. After all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a STOP condition (see Figure 6). In read mode, the master issues a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, and then raises SDA high to establish a STOP condition (see Figure 7).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its Slave Address and Instruction Bytes in the write mode, the RDAC output is updated on each successive byte. If different instructions are needed, the write/read mode has to start again with a new Slave Address, Instruction, and Data Byte. Similarly, a repeated read function of the RDAC is also allowed.

The diagram shows an MCU connected to an AD5259 DAC. The MCU's VCC is connected to a 3.3V supply (VCC(~3.3V)) through a 1μF capacitor (C1). The MCU's GND is connected to ground. The MCU's SCL and SDA pins are connected to the AD5259's VDD and VLOGIC pins, respectively. The AD5259's GND pin is connected to ground. The AD5259's VDD pin is connected to a 5V supply through a 70k resistor (R1). The AD5259's VLOGIC pin is connected to a 14.4V supply through a 70k resistor (R2). The AD5259's SCL pin is connected to a 10k resistor (R3) which is connected to ground. The AD5259's SDA pin is connected to a 25k resistor (R4) which is connected to ground. The AD5259's SCL and SDA pins are also connected to an AD8565 comparator. The AD8565's non-inverting input (+) is connected to the SCL pin and a 10k resistor (R5) which is connected to ground. The AD8565's inverting input (-) is connected to the SDA pin and a 10k resistor (R6) which is connected to ground. The AD8565's output is connected to a 3.5V supply (3.5V < Vcom < 4.5V).

The diagram shows an MCU connected to an AD5259 digital potentiometer. The AD5259 is powered by a 14.4V supply through a 70k resistor (R1) and has its wiper connected to ground through a 25k resistor (R3). The MCU's VCC is connected to a 3.3V supply through a 1uF capacitor (C1). The MCU's SCL and SDA lines are connected to the AD5259's VLOGIC and VDD pins, respectively. The AD5259's VLOGIC pin is also connected to a 10k resistor (R2) which is connected to the non-inverting input of an AD8565 precision centrer. The AD8565 is configured as a voltage follower with its output connected to its inverting input. The output of the AD8565 is labeled as 3.5V < Vcom < 4.5V. A text box indicates that the 14.4V supply also powers the logic supply of the digital pot.

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ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C, unless otherwise noted.)

Table 4

Parameter	Value
V _{DD} to GND	−0.3 V to +7 V
V _A , V _B , V _W to GND	V _{SS} −0.3V, V _{DD} +0.3V
I _{MAX}	
Pulsed ¹	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to +7 V
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature (T _{JMAX})	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance ² θ _{JA} : MSOP-10	200°C/W

NOTES

¹ Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

² Package power dissipation = (T_{JMAX} − T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

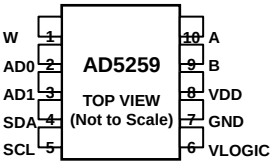


Figure 2. AD5172 Pin Configuration

Table 5. AD5259 Pin Function Descriptions

Pin	Mnemonic	Description
1	W	W Terminal. $GND \leq V_W \leq V_{DD}$.
2	ADO	Programmable Tri-State Address Bit 0 for Multiple Package Decoding.
3	AD1	Programmable Tri-State Address Bit 1 for Multiple Package Decoding.
4	SDA	Serial Data Input/Output.
5	SCL	Serial Clock Input. Positive edge triggered.
6	VLOGIC	Logic power supply.
7	GND	Digital Ground.
8	VDD	Positive Power Supply.
9	B	B Terminal. $GND \leq V_B \leq V_{DD}$.
10	A	A Terminal. $GND \leq V_A \leq V_{DD}$.

Outline Dimensions

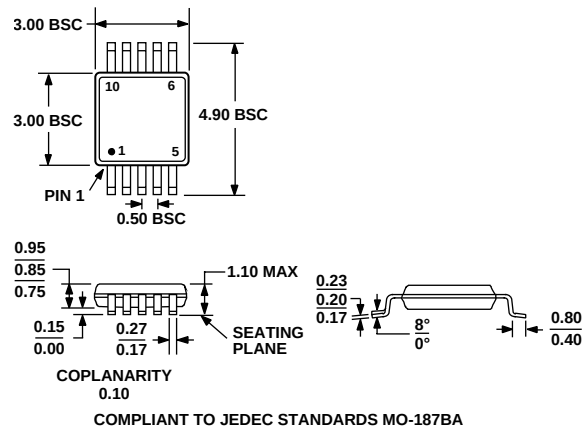


Figure 3. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (Ω)	Temperature	Package Description	Package Option	Branding
AD5259BRMZ5 ¹	5k	-40°C to +85°C	MSOP-10	RM-10	D4P
AD5259BRMZ5-RL7 ¹	5k	-40°C to +85°C	MSOP-10	RM-10	D4P
AD5259BRMZ10 ¹	10k	-40°C to +85°C	MSOP-10	RM-10	D4Q
AD5259BRMZ10-RL7 ¹	10k	-40°C to +85°C	MSOP-10	RM-10	D4Q
AD5259BRMZ50 ¹	50k	-40°C to +85°C	MSOP-10	RM-10	D4R
AD5259BRMZ50-RL7 ¹	50k	-40°C to +85°C	MSOP-10	RM-10	D4R
AD5259BRMZ100 ¹	100k	-40°C to +85°C	MSOP-10	RM-10	D4S
AD5259BRMZ100-RL7 ¹	100k	-40°C to +85°C	MSOP-10	RM-10	D4S

¹ Z = Pb-free part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



NOTES