



NBM™ in a VIA Package Bus Converter

NBM3814x60E12A7yzz



Non-Isolated, Fixed-Ratio DC-DC Converter

Features & Benefits

- Up to 170A continuous low voltage side current
- Fixed transformation ratio (K) of 1/5
- Up to 1046W/in³ power density
- 97.8% peak efficiency
- Bidirectional operation capability
- Integrated ceramic capacitance filtering
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 3814 package
- High MTBF
- Thermally enhanced VIA package

Typical Applications

- DC Power Distribution
- Information and Communication Technology (ICT) Equipment
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Energy Systems
- Transportation



| Product Ratings | |
|---|-------------------------------|
| $V_{HI} = 54V$ (36 – 60V) | $I_{LO} = \text{up to } 170A$ |
| $V_{LO} = 10.8V$ (7.2 – 12.0V) (NO LOAD) | $K = 1/5$ |

Product Description

The NBM3814x60E12A7yzz in a VIA package is a high efficiency Bus Converter, operating from a 36 to 60V_{DC} high voltage bus to deliver a non-isolated 7.2 to 12V_{DC} unregulated, low voltage.

This unique, ultra-low profile module incorporates DC-DC conversion and integrated filtering in a chassis or PCB mount form factor.

The NBM offers low noise, fast transient response and industry leading efficiency and power density.

Leveraging the thermal and density benefits of Vicor VIA packaging technology, the NBM module offers flexible thermal management options with very low top and bottom side thermal impedances.

When combined with downstream Vicor DC-DC conversion components and regulators, the NBM allows the Power Design Engineer to employ a simple, low-profile design, which will differentiate the end system without compromising on cost or performance metrics.

The NBM non-isolated topology allows start up and steady state operation in forward and reverse directions. It provides bidirectional protections. However if the powertrain is disabled by any protection and V_{LO} is present, then a voltage equal to V_{LO} minus two diode drops will appear on the high voltage side.

Size:
3.76 x 1.40 x 0.37in
[95.59 x 35.54 x 9.40mm]

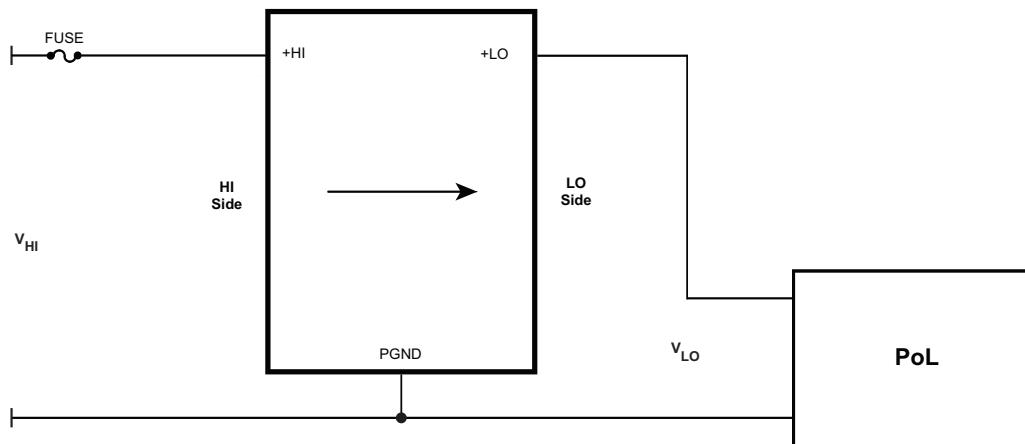
Part Ordering Information

| Product Function | Package Length | Package Width | Package Type | Max High Side Voltage | High Side Voltage Range Ratio | Max Low Side Voltage | Max Low Side Current | Product Grade (Case Temperature) | Option Field |
|--|--------------------------|-------------------------|----------------------------------|-----------------------|-------------------------------|----------------------|----------------------|--|---|
| NBM | 38 | 14 | x | 60 | E | 15 | A7 | y | zz |
| NBM = Non-Isolated Bus Converter Module | Length in Inches x 10 | Width in Inches x 10 | B = Board VIA V = Chassis VIA | | Internal Reference | | | C = -20 to 100°C ^[a] T = -40 to 100°C ^[a] | 00 = Chassis/Always On 04 = Short Pin/Always On 08 = Long Pin/Always On |

^[a] High Temperature Current Derating may apply; See Figure 1, specified thermal operating area.

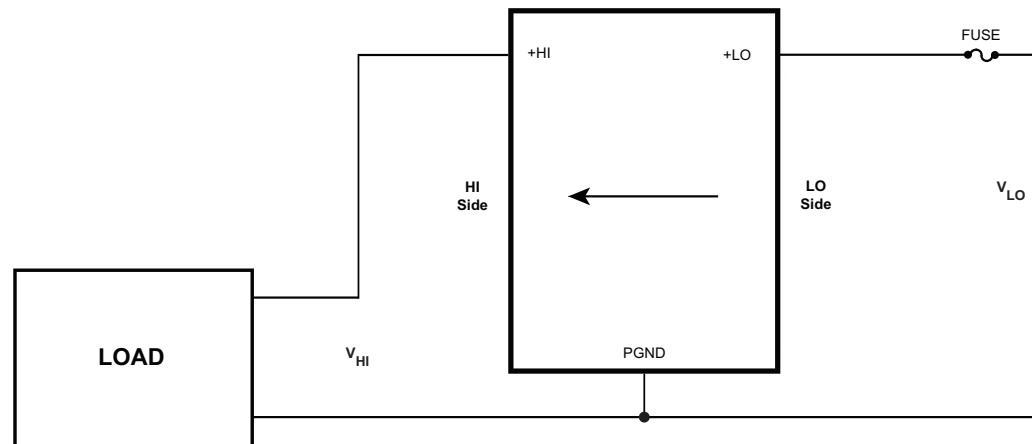
Typical Applications

NBM in a VIA Package



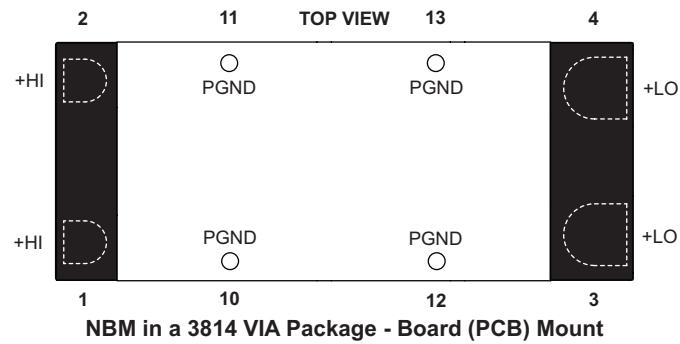
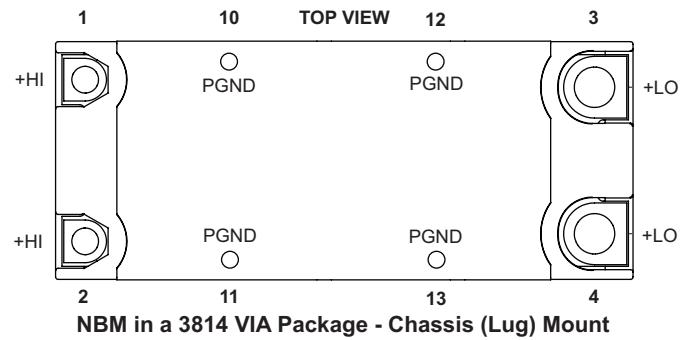
NBM3814x60E12A7yzz at point of load providing fixed ratio step-down DC-DC conversion to PoL devices.
NBM is operating in forward direction.

NBM in a VIA Package



NBM3814x60E12A7yzz providing fixed ratio step-up DC-DC conversion. NBM is operating in reverse direction.

Pin Configuration



Pin Descriptions

| Pin Number | Signal Name | Type | Function |
|----------------|-------------|-----------------|---|
| 1, 2 | +HI | HIGH SIDE POWER | High voltage side positive power terminal |
| 3, 4 | +LO | LOW SIDE POWER | Low voltage side positive power terminal |
| 10, 11, 12, 13 | PGND | POWER RETURN | Common negative power terminal |

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

| Parameter | Comments | Min | Max | Unit |
|---|---------------------------------------|-----|-----|-----------------|
| +HI to PGND | | -1 | 80 | V |
| HI_DC or LO_DC Slew Rate | | | 1 | V/μs |
| +LO to PGND | | -1 | 16 | V |
| Isolation Voltage / Dielectric Withstand ^[b] | High voltage side to case | N/A | | V _{DC} |
| | High voltage side to low voltage side | N/A | | V _{DC} |
| | Low voltage side to case | N/A | | V _{DC} |

[b] The PGND of the NBM in a VIA package is directly connected to the case. The NBM does not contain any insulation (isolation) from high voltage side to low voltage side.

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{CASE}} \leq 100^{\circ}\text{C}$ (T-Grade); all other specifications are at $T_{\text{CASE}} = 25^{\circ}\text{C}$ unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|-----------------------------|--|-------------|------|-------------|------------------|
| General Powertrain Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side) | | | | | | |
| HI Side Voltage Range, (Continuous) | $V_{\text{HI_DC}}$ | | 36 | | 60 | V |
| HI Side Voltage Initialization Threshold | $V_{\mu\text{C_ACTIVE}}$ | Hi side voltage where internal controller is initialized, (powertrain inactive) | | | 15 | V |
| HI Side Quiescent Current | $I_{\text{HI_Q}}$ | Disabled, $V_{\text{HI_DC}} = 54\text{V}$ | | 7 | | mA |
| | | $T_{\text{CASE}} \leq 100^{\circ}\text{C}$ | | | 12 | |
| No Load Power Dissipation | $P_{\text{HI_NL}}$ | $V_{\text{HI_DC}} = 54\text{V}, T_{\text{CASE}} = 25^{\circ}\text{C}$ | | 10 | 12 | W |
| | | $V_{\text{HI_DC}} = 54\text{V}$ | 8 | | 19 | |
| | | $V_{\text{HI_DC}} = 36 - 60\text{V}, T_{\text{CASE}} = 25^{\circ}\text{C}$ | | | 14 | |
| | | $V_{\text{HI_DC}} = 36 - 60\text{V}$ | | | 22 | |
| HI Side Inrush Current Peak | $I_{\text{HI_INR_PK}}$ | $V_{\text{HI_DC}} = 60\text{V}, C_{\text{LO_EXT}} = 3000\mu\text{F}, R_{\text{LOAD_LO}} = 20\%$ of full load current | | 15 | | A |
| | | $T_{\text{CASE}} \leq 100^{\circ}\text{C}$ | | | 50 | |
| DC HI Side Current | $I_{\text{HI_IN_DC}}$ | At $I_{\text{LO_OUT_DC}} = 170\text{A}, T_{\text{CASE}} \leq 90^{\circ}\text{C}$ | | | 34.4 | A |
| Transformation Ratio | K | High voltage to low voltage, $K = V_{\text{LO_DC}} / V_{\text{HI_DC}}$, at no load | | 1/5 | | V/V |
| LO Side Current (Continuous) | $I_{\text{LO_OUT_DC}}$ | $T_{\text{CASE}} \leq 90^{\circ}\text{C}$ | | | 170 | A |
| LO Side Current (Pulsed) | $I_{\text{LO_OUT_PULSE}}$ | 10ms pulse, 25% duty cycle, $I_{\text{LO_OUT_AVG}} \leq 50\%$ rated $I_{\text{LO_OUT_DC}}$ | | | 200 | A |
| Efficiency (Ambient) | η_{AMB} | $V_{\text{HI_DC}} = 54\text{V}, I_{\text{LO_OUT_DC}} = 170\text{A}$ | 96.5 | 97 | | % |
| | | $V_{\text{HI_DC}} = 36\text{V to } 60\text{V}, I_{\text{LO_OUT_DC}} = 170\text{A}$ | 95.6 | | | |
| | | $V_{\text{HI_DC}} = 54\text{V}, I_{\text{LO_OUT_DC}} = 85\text{A}$ | 97.3 | 97.8 | | |
| Efficiency (Hot) | η_{HOT} | $V_{\text{HI_DC}} = 54\text{V}, I_{\text{LO_OUT_DC}} = 170\text{A}, T_{\text{CASE}} = 90^{\circ}\text{C}$ | 96.2 | 96.5 | | % |
| Efficiency (Over Load Range) | $\eta_{20\%}$ | $34\text{A} < I_{\text{LO_OUT_DC}} < 170\text{A}$ | 95 | | | % |
| LO Side Output Resistance | $R_{\text{LO_COLD}}$ | $V_{\text{HI_DC}} = 54\text{V}, I_{\text{LO_OUT_DC}} = 170\text{A}, T_{\text{CASE}} = -40^{\circ}\text{C}$ | 0.5 | 1.1 | 1.5 | $\text{m}\Omega$ |
| | $R_{\text{LO_AMB}}$ | $V_{\text{HI_DC}} = 54\text{V}, I_{\text{LO_OUT_DC}} = 170\text{A}$ | 0.8 | 1.3 | 1.8 | |
| | $R_{\text{LO_HOT}}$ | $V_{\text{HI_DC}} = 54\text{V}, I_{\text{LO_OUT_DC}} = 170\text{A}, T_{\text{CASE}} = 90^{\circ}\text{C}$ | 1.1 | 1.7 | 2.0 | |
| Switching Frequency | F_{SW} | LO side voltage ripple frequency = $2 \times F_{\text{SW}}$ | 1.02 | 1.07 | 1.12 | MHz |
| LO Side Voltage Ripple | $V_{\text{LO_OUT_PP}}$ | $C_{\text{LO_EXT}} = 0\mu\text{F}, I_{\text{LO_OUT_DC}} = 170\text{A}, V_{\text{HI_DC}} = 54\text{V}, 20\text{MHz BW}$ | | 125 | | mV |
| | | $T_{\text{CASE}} \leq 100^{\circ}\text{C}$ | | | 400 | |

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of $-40^\circ\text{C} \leq T_{\text{CASE}} \leq 100^\circ\text{C}$ (T-Grade); all other specifications are at $T_{\text{CASE}} = 25^\circ\text{C}$ unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|--|-------------------------------|--|------------|-------|-------------|------------------|
| General Powertrain Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side), Cont. | | | | | | |
| Effective HI Side Capacitance (Internal) | $C_{\text{HI_INT}}$ | Effective value at $54V_{\text{HI_DC}}$ | | 16.80 | | μF |
| Effective LO Side Capacitance (Internal) | $C_{\text{LO_INT}}$ | Effective value at $10.8V_{\text{LO_DC}}$ | | 140 | | μF |
| Rated LO Side Capacitance (External) | $C_{\text{LO_OUT_EXT}}$ | Excessive capacitance may drive module into short circuit protection | | | 3000 | μF |
| Rated LO Side Capacitance (External), Parallel Array Operation | $C_{\text{LO_OUT_AEXT}}$ | $C_{\text{LO_OUT_AEXT}} \text{ Max} = N \cdot 0.5 \cdot C_{\text{LO_OUT_EXT MAX}}$, where $N = \text{the number of units in parallel}$ | | | | |
| Powertrain Protection Specification – Forward Direction Operation (High Voltage Side to Low Voltage Side) | | | | | | |
| Auto Restart Time | $t_{\text{AUTO_RESTART}}$ | Start up into a persistent fault condition. Non-latching fault detection given $V_{\text{HI_DC}} > V_{\text{HI_UVLO+}}$ | 940 | | 1010 | ms |
| HI Side Overvoltage Lockout Threshold | $V_{\text{HI_OVLO+}}$ | | 63 | 66 | 69 | V |
| Hi Side Overvoltage Recovery Threshold | $V_{\text{HI_OVLO-}}$ | | 60 | 63 | 66 | V |
| HI Side Overvoltage Lockout Hysteresis | $V_{\text{HI_OVLO_HYST}}$ | | | 3 | | V |
| HI Side Overvoltage Lockout Response Time | $t_{\text{HI_OVLO}}$ | | | 30 | | μs |
| HI Side Undervoltage Lockout Threshold | $V_{\text{HI_UVLO-}}$ | | 28 | 30 | 32 | V |
| HI Side Undervoltage Recovery Threshold | $V_{\text{HI_UVLO+}}$ | | 32 | 34 | 36 | V |
| HI Side Undervoltage Lockout Hysteresis | $V_{\text{HI_UVLO_HYST}}$ | | | 4 | | V |
| HI Side Undervoltage Lockout Response Time | $t_{\text{HI_UVLO}}$ | | | 100 | | μs |
| HI Side Undervoltage Start-Up Delay | $t_{\text{HI_UVLO+_DELAY}}$ | From $V_{\text{HI_DC}} = V_{\text{HI_UVLO+}}$ to powertrain active (i.e., one time start-up delay from application of $V_{\text{HI_DC}}$ to $V_{\text{LO_DC}}$) | | 30 | | ms |
| HI Side Soft-Start Time | $t_{\text{HI_SOFT-START}}$ | From powertrain active. Fast current limit protection disabled during soft start | | 1 | | ms |
| LO Side Overcurrent Trip Threshold | $I_{\text{LO_OUT_OCP}}$ | | 201 | 220 | 320 | A |
| LO Side Overcurrent Response Time Constant | $t_{\text{LO_OUT_OCP}}$ | Effective internal RC filter | | 4 | | ms |
| LO Side Short Circuit Protection Trip Threshold | $I_{\text{LO_OUT_SCP}}$ | | 250 | | | A |
| LO Side Short Circuit Protection Response Time | $t_{\text{LO_OUT_SCP}}$ | | | 1 | | μs |
| Overtemperature Shutdown Threshold | $t_{\text{OTP+}}$ | Temperature sensor located inside controller IC | 125 | | | $^\circ\text{C}$ |
| Overtemperature Recovery Threshold | $t_{\text{OTP-}}$ | | 105 | 110 | 115 | $^\circ\text{C}$ |
| Undertemperature Shutdown Threshold | t_{UTP} | Temperature sensor located inside controller IC; Protection not available for M-Grade units. | | | -45 | $^\circ\text{C}$ |
| Undertemperature Restart Time | $t_{\text{UTP_RESTART}}$ | Start up into a persistent fault condition. Non-latching fault detection given $V_{\text{HI_DC}} > V_{\text{HI_UVLO+}}$ | | 3 | | s |

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{CASE}} \leq 100^{\circ}\text{C}$ (T-Grade); all other specifications are at $T_{\text{CASE}} = 25^{\circ}\text{C}$ unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|---|-----------------------------|---|-------------|------|-------------|------------------|
| General Powertrain Specification – Reverse Direction Operation (Low Voltage Side to High Voltage Side) | | | | | | |
| LO Side Voltage Range, (Continuous) | $V_{\text{LO_DC}}$ | | 7.2 | | 12.0 | V |
| No Load Power Dissipation | $P_{\text{LO_NL}}$ | $V_{\text{LO_DC}} = 10.8\text{V}, T_{\text{CASE}} = 25^{\circ}\text{C}$ | | 10 | 12 | W |
| | | $V_{\text{LO_DC}} = 10.8\text{V}$ | 8.0 | | 19 | |
| | | $V_{\text{LO_DC}} = 7.2 - 12.0\text{V}, T_{\text{CASE}} = 25^{\circ}\text{C}$ | | | 14 | |
| | | $V_{\text{LO_DC}} = 7.2 - 12.0\text{V}$ | | | 22 | |
| DC LO Side Current | $I_{\text{LO_IN_DC}}$ | At $I_{\text{HI_DC}} = 34\text{A}, T_{\text{CASE}} \leq 90^{\circ}\text{C}$ | | | 172 | A |
| HI Side Current (Continuous) | $I_{\text{HI_OUT_DC}}$ | $T_{\text{CASE}} \leq 90^{\circ}\text{C}$ | | | 34 | A |
| HI Side Current (Pulsed) | $I_{\text{HI_OUT_PULSE}}$ | 10ms pulse, 25% duty cycle, $I_{\text{HI_OUT_AVG}} \leq 50\%$ rated $I_{\text{HI_OUT_DC}}$ | | | 40.8 | A |
| Efficiency (Ambient) | η_{AMB} | $V_{\text{LO_DC}} = 10.8\text{V}, I_{\text{HI_OUT_DC}} = 34\text{A}$ | 96.1 | 96.6 | | % |
| | | $V_{\text{LO_DC}} = 7.2\text{V to } 12.0\text{V}, I_{\text{HI_OUT_DC}} = 34\text{A}$ | 95.2 | | | |
| | | $V_{\text{LO_DC}} = 10.8\text{V}, I_{\text{HI_OUT_DC}} = 17\text{A}$ | 97.3 | 97.8 | | |
| Efficiency (Hot) | η_{HOT} | $V_{\text{LO_DC}} = 10.8\text{V}, I_{\text{HI_OUT_DC}} = 34\text{A}, T_{\text{CASE}} = 90^{\circ}\text{C}$ | 95.8 | 96.1 | | % |
| Efficiency (Over Load Range) | $\eta_{20\%}$ | $6.80\text{A} < I_{\text{HI_OUT_DC}} < 34\text{A}$ | 94.5 | | | % |
| HI Side Output Resistance | $R_{\text{HI_COLD}}$ | $V_{\text{LO_DC}} = 10.8\text{V}, I_{\text{HI_OUT_DC}} = 34\text{A}, T_{\text{CASE}} = -40^{\circ}\text{C}$ | 22 | 39 | 49 | $\text{m}\Omega$ |
| | $R_{\text{HI_AMB}}$ | $V_{\text{LO_DC}} = 10.8\text{V}, I_{\text{HI_OUT_DC}} = 34\text{A}$ | 28 | 49 | 72 | |
| | $R_{\text{HI_HOT}}$ | $V_{\text{LO_DC}} = 10.8\text{V}, I_{\text{HI_OUT_DC}} = 34\text{A}, T_{\text{CASE}} = 90^{\circ}\text{C}$ | 36 | 58 | 70 | |
| HI Side Voltage Ripple | $V_{\text{HI_OUT_PP}}$ | $C_{\text{HI_OUT_EXT}} = 0\mu\text{F}, I_{\text{HI_OUT_DC}} = 34\text{A}, V_{\text{LO_DC}} = 10.8\text{V, 20MHz BW}$ | | 625 | | mV |
| | | $T_{\text{CASE}} \leq 100^{\circ}\text{C}$ | | | 1500 | |

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{CASE}} \leq 100^{\circ}\text{C}$ (T-Grade); all other specifications are at $T_{\text{CASE}} = 25^{\circ}\text{C}$ unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|--|---------------------------|---|-------------|------|-------------|---------------|
| Powertrain Protection Specification – Reverse Direction Operation (Low Voltage Side to High Voltage Side) | | | | | | |
| Rated HI Side Capacitance (External) | $C_{\text{HI_OUT_EXT}}$ | Excessive capacitance may drive module into short circuit protection when starting from low voltage side to high voltage side | | | 100 | μF |
| LO Side Overvoltage Lockout Threshold | $V_{\text{LO_OVLO+}}$ | | 12.8 | 13.2 | 13.6 | V |
| LO Side Overvoltage Recovery Threshold | $V_{\text{HI_OVLO-}}$ | | 12 | 12.6 | 13.2 | V |
| LO Side Overvoltage Lockout Response Time | $t_{\text{HI_OVLO}}$ | | | 30 | | μs |
| LO Side Undervoltage Lockout Threshold | $V_{\text{LO_UVLO-}}$ | | 5.6 | 6 | 6.4 | V |
| LO Side Undervoltage Recovery Threshold | $V_{\text{HI_UVLO+}}$ | | 6.4 | 6.8 | 7.2 | V |
| LO Side Undervoltage Lockout Response Time | $t_{\text{LO_UVLO}}$ | | | 100 | | μs |
| HI Side Overcurrent Trip Threshold | $I_{\text{HI_OUT_OCP}}$ | Powertrain is stopped but current can flow from LO Side to HI Side through MOSFET body diodes | 40 | 44 | 64 | A |
| HI Side Overcurrent Response Time Constant | $t_{\text{HI_OUT_OCP}}$ | Effective internal RC filter | | 4 | | ms |
| HI Side Short Circuit Protection Trip Threshold | $I_{\text{HI_SCP}}$ | Powertrain is stopped but current can flow from LO Side to HI Side through MOSFET body diodes | 50 | | | A |
| HI Side Short Circuit Protection Response Time | $t_{\text{HI_SCP}}$ | | | 1 | | μs |

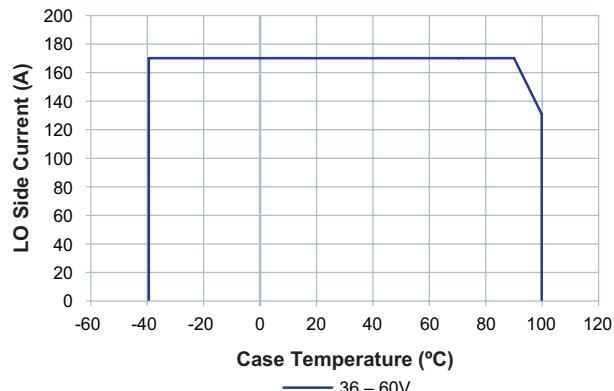


Figure 1 — Specified thermal operating area

1. The NBM in a VIA package is cooled through the bottom case (bottom housing).
2. The thermal rating is based on typical measured device efficiency.
3. The case temperature in the graph is the measured temperature of the bottom housing, such that the internal operating temperature does not exceed 125°C.

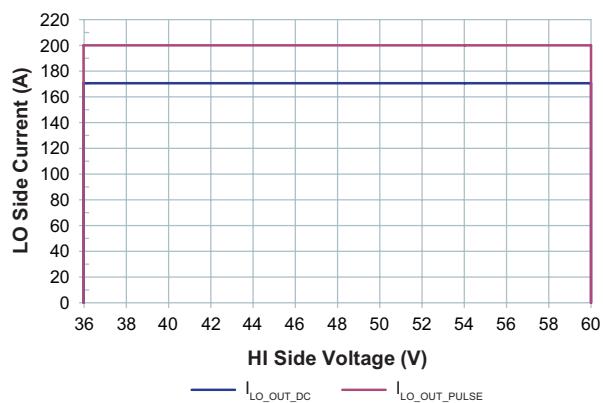
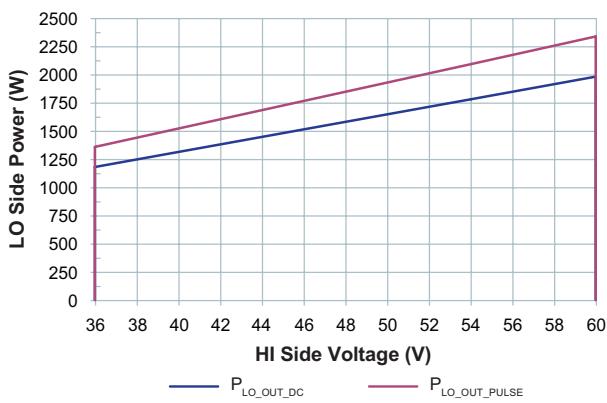


Figure 2 — Specified electrical operating area using rated R_{LO_HOT}

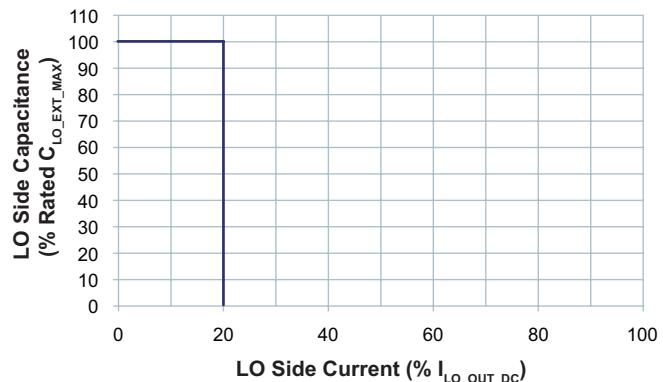
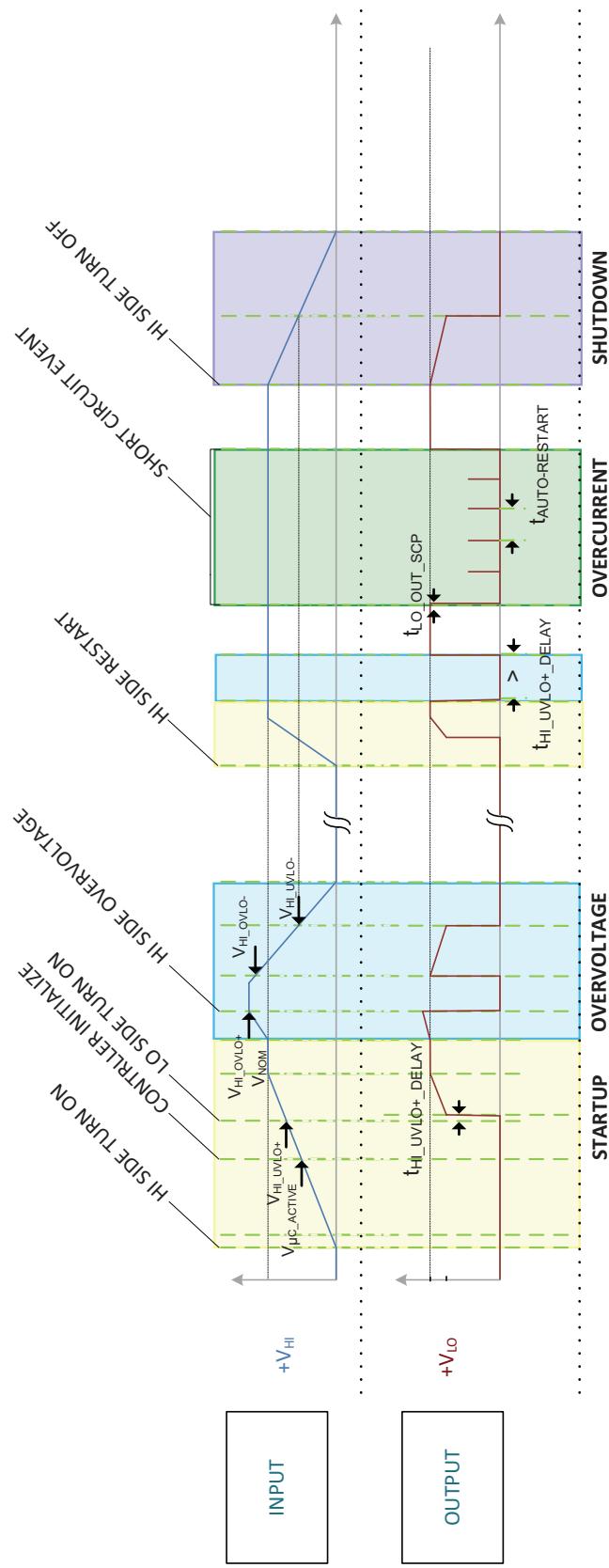
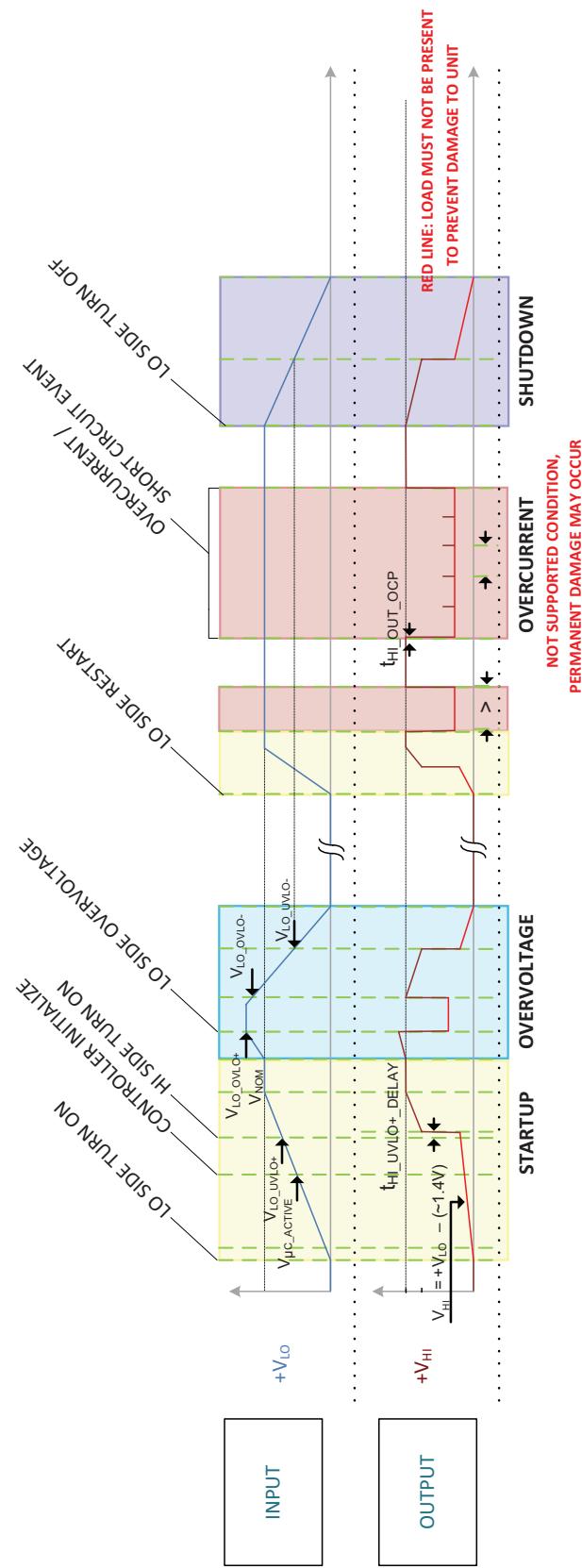


Figure 3 — Specified HI side start-up into load current and external capacitance

Timing Diagram (Forward Direction)



Timing Diagram (Reverse Direction)



Application Characteristics

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high voltage side to low voltage side). See associated figures for general trend data.

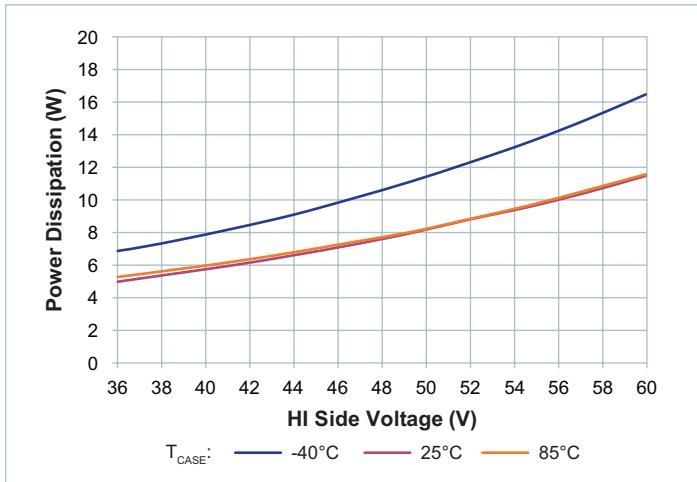


Figure 4—No load power dissipation vs. V_{HI_DC}

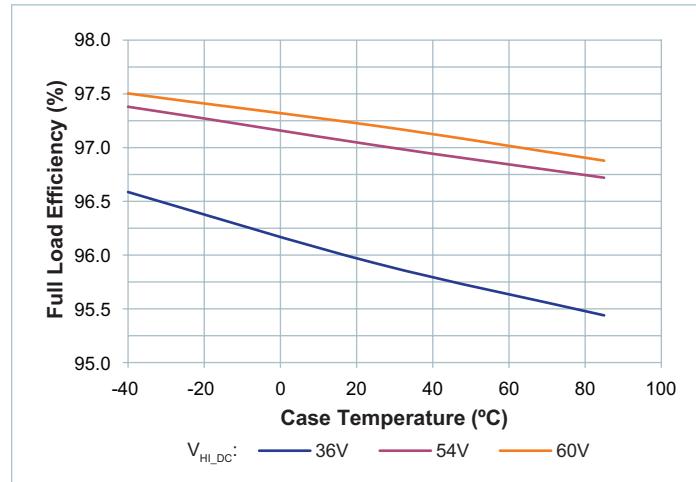


Figure 5—Full load efficiency vs. temperature

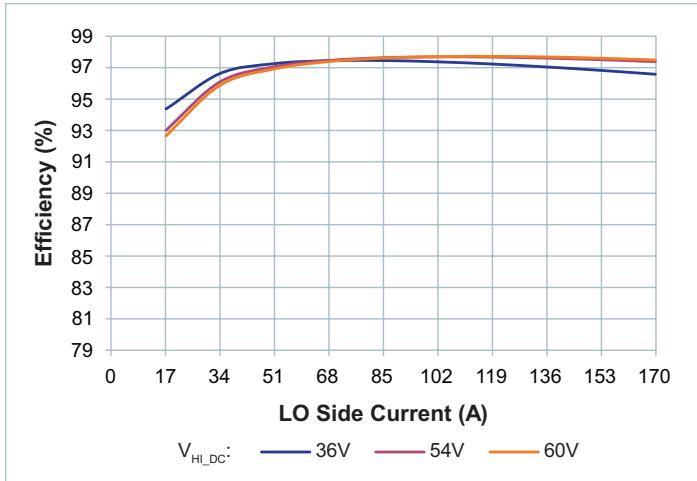


Figure 6—Efficiency at $T_{CASE} = -40^{\circ}\text{C}$

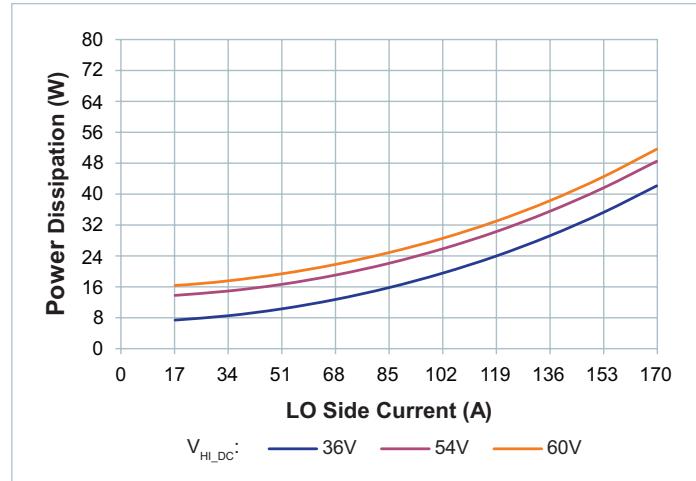


Figure 7—Power dissipation at $T_{CASE} = -40^{\circ}\text{C}$

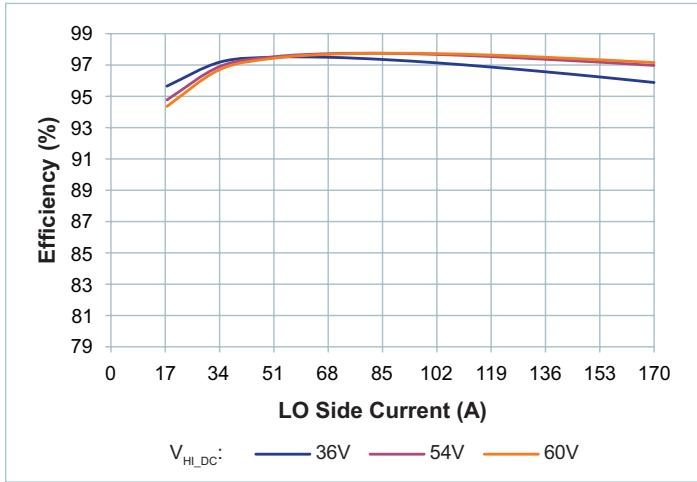


Figure 8—Efficiency at $T_{CASE} = 25^{\circ}\text{C}$

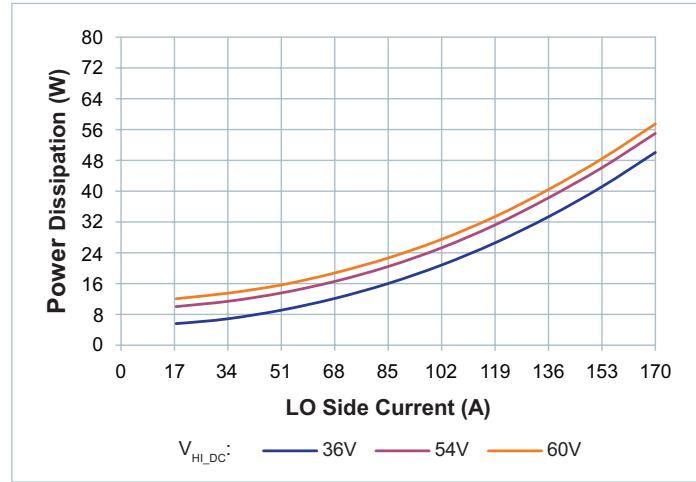


Figure 9—Power dissipation at $T_{CASE} = 25^{\circ}\text{C}$

Application Characteristics (Cont.)

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high voltage side to low voltage side). See associated figures for general trend data.

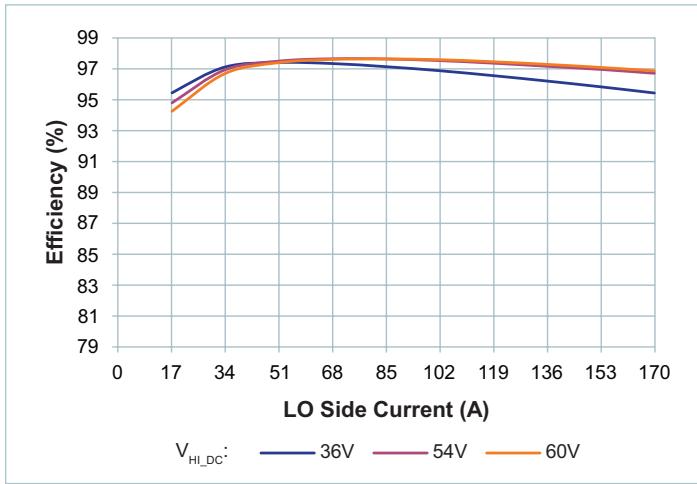


Figure 10 — Efficiency at $T_{CASE} = 85^\circ\text{C}$

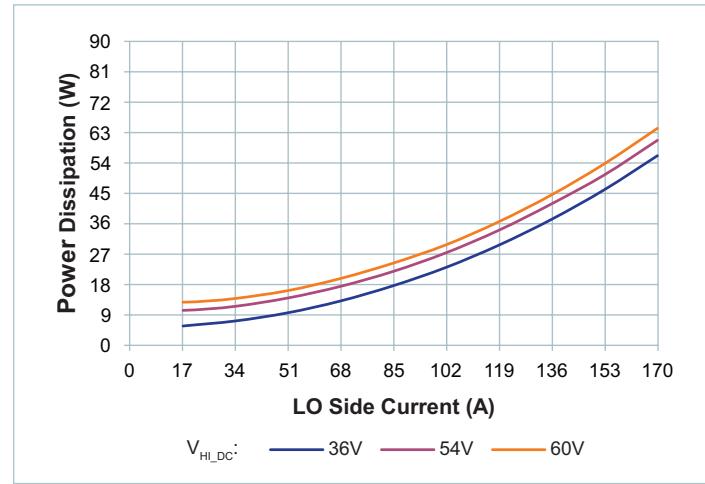


Figure 11 — Power dissipation at $T_{CASE} = 85^\circ\text{C}$

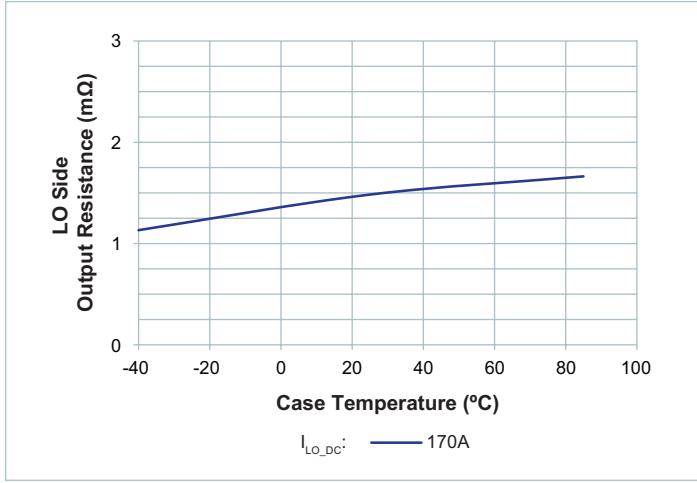


Figure 12 — R_{LO} vs. temperature; Nominal V_{HI_DC}
 $I_{LO_DC} = 170\text{A}$ at $T_{CASE} = 85^\circ\text{C}$

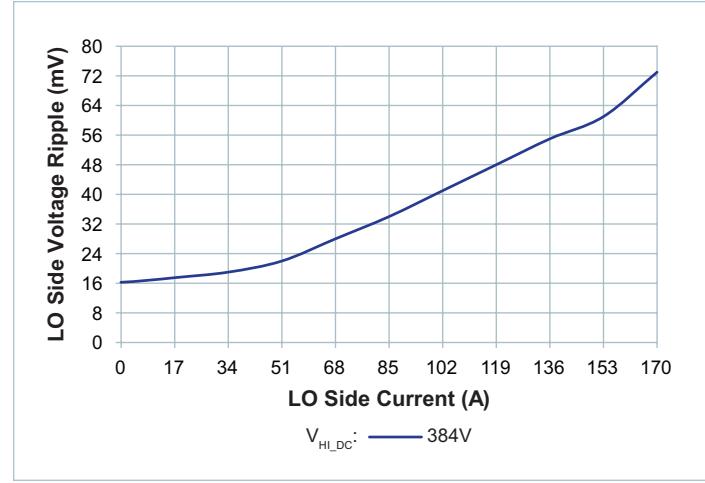


Figure 13 — $V_{LO_OUT_PP}$ vs. I_{LO_DG} ; No external $C_{LO_OUT_EXT}$. Board mounted module, scope setting: 20MHz analog BW

Application Characteristics (Cont.)

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high voltage side to low voltage side). See associated figures for general trend data.

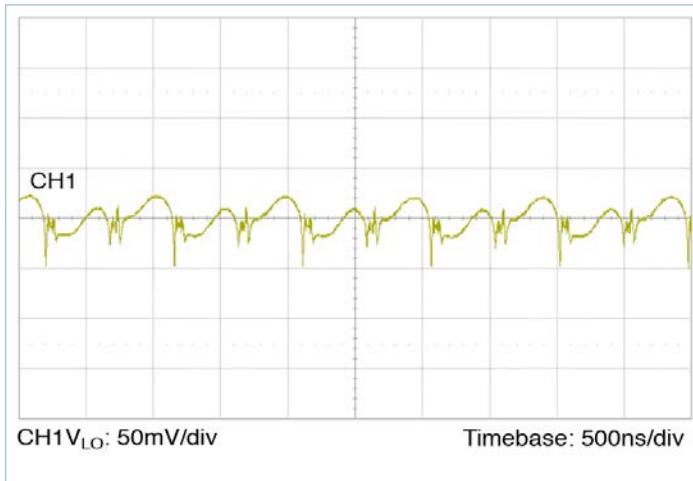


Figure 14 — Full load LO side voltage ripple, $300\mu\text{F}$ $C_{\text{HI_IN_EXT}}$,
No external $C_{\text{LO_OUT_EXT}}$. Board mounted module,
scope setting: 20MHz analog BW

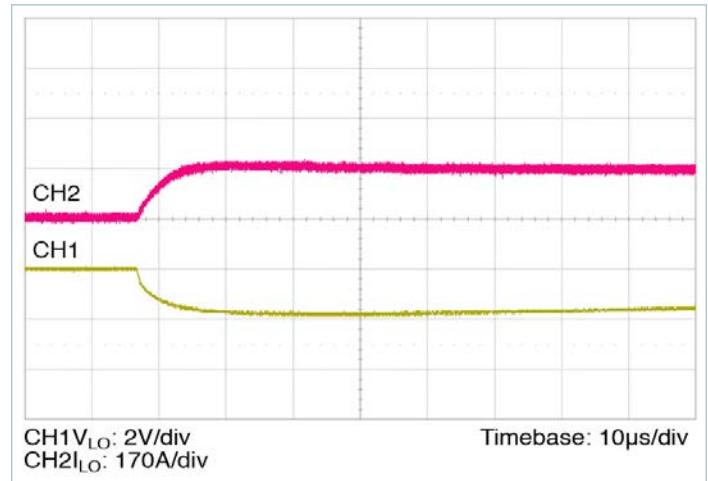


Figure 15 — 0A – 170A transient response:
 $C_{\text{HI_IN_EXT}} = 300\mu\text{F}$, no external $C_{\text{LO_OUT_EXT}}$

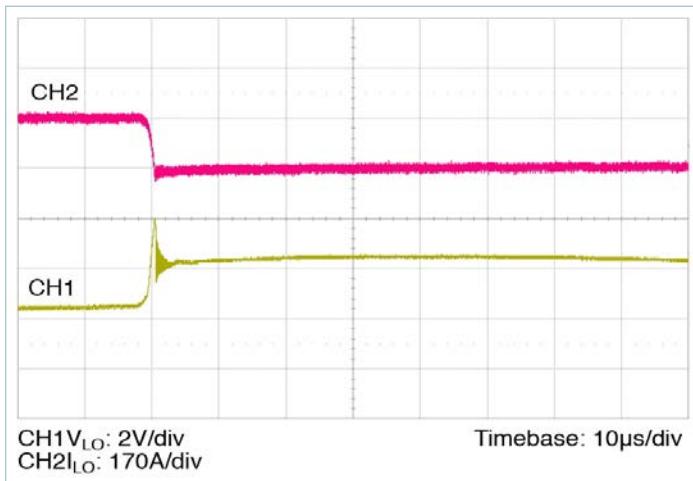


Figure 16 — 170A – 0A transient response:
 $C_{\text{HI_IN_EXT}} = 300\mu\text{F}$, no external $C_{\text{LO_OUT_EXT}}$

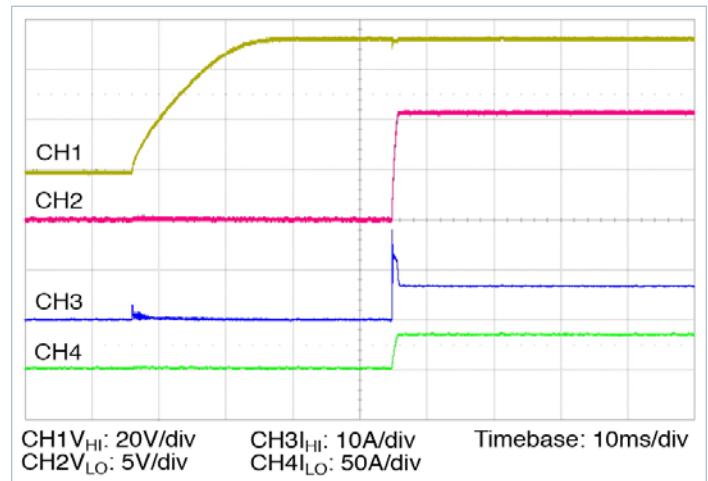


Figure 17 — Forward start up from application of $V_{\text{HI_DC}} = 54\text{V}$, 20%
 $I_{\text{LO_DG}}$ 100% $C_{\text{LO_OUT_EXT}}$

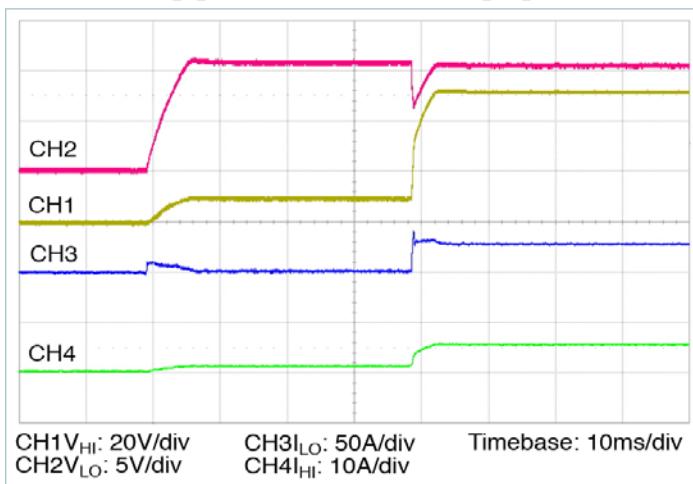


Figure 18 — Reverse start up from application of
 $V_{\text{LO_DC}} = 10.8\text{V}$, 20% $I_{\text{HI_DG}}$ 100% $C_{\text{HI_OUT_EXT}}$

General Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{CASE}} \leq 100^{\circ}\text{C}$ (T-Grade); all other specifications are at $T_{\text{CASE}} = 25^{\circ}\text{C}$ unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|--|----------------------|---|---------------|--------------|---------------|------------------------------------|
| Mechanical | | | | | | |
| Length | L | Lug (Chassis) Mount | 95.34 [3.75] | 95.59 [3.76] | 95.84 [3.77] | mm [in] |
| Length | L | PCB (Board) Mount | 95.34 [3.75] | 95.59 [3.76] | 95.84 [3.77] | mm [in] |
| Width | W | | 35.29 [1.39] | 35.54 [1.40] | 35.79 [1.41] | mm [in] |
| Height | H | | 9.019 [0.355] | 9.40 [0.37] | 9.781 [0.385] | mm [in] |
| Volume | Vol | Without heatsink | | 31.93 [1.95] | | cm ³ [in ³] |
| Weight | W | | | 130.4 [4.6] | | g [oz] |
| Pin Material | | C145 copper, 1/2 hard | | | | |
| Underplate | | Low-stress ductile Nickel | 50 | | 100 | μin |
| Pin Finish (Gold) | | Palladium | 0.8 | | 6 | μin |
| | | Soft Gold | 0.12 | | 2 | |
| Pin Finish (Tin) | | Whisker-resistant matte Tin | 200 | | 400 | μin |
| Thermal | | | | | | |
| Operating Internal Temperature | T _{INT} | NBM3814x60E12A7yzz (T-Grade) | -40 | | 125 | °C |
| | | NBM3814x60E12A7yzz (C-Grade) | -20 | | 125 | |
| Operating Case Temperature | T _{CASE} | NBM3814x60E12A7yzz (T-Grade), derating applied, see safe thermal operating area | -40 | | 100 | |
| | | NBM3814x60E12A7yzz (C-Grade), derating applied, see safe thermal operating area | -20 | | 100 | |
| Thermal Resistance Top Side | θ _{INT_TOP} | Estimated thermal resistance to maximum temperature internal component from isothermal top | | 1.21 | | °C/W |
| Thermal Resistance Coupling Between Top Case and Bottom Case | θ _{HOU} | Estimated thermal resistance of thermal coupling between the top and bottom case surfaces | | 0.47 | | °C/W |
| Thermal Resistance Bottom Side | θ _{INT_BOT} | Estimated thermal resistance to maximum temperature internal component from isothermal bottom | | 0.70 | | °C/W |
| Thermal Capacity | | | | 52 | | Ws/°C |
| Assembly | | | | | | |
| Storage Temperature | T _{ST} | NBM3814x60E12A7yzz (T-Grade) | -40 | | 125 | °C |
| | | NBM3814x60E12A7yzz (C-Grade) | -40 | | 125 | °C |
| ESD Withstand | ESD _{HBM} | Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to <2kV) | 1000 | | | |
| | ESD _{CDM} | Charge Device Model, "JESD 22-C101-E" Class II (200V to <500V) | 200 | | | |

General Characteristics (Cont.)

Specifications apply over all line, load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of $-40^{\circ}\text{C} \leq T_{\text{CASE}} \leq 100^{\circ}\text{C}$ (T-Grade); all other specifications are at $T_{\text{CASE}} = 25^{\circ}\text{C}$ unless otherwise noted.

| Attribute | Symbol | Conditions / Notes | Min | Typ | Max | Unit |
|------------------------------|---------------------|--|-----|-----|-----|------|
| Safety | | | | | | |
| Isolation Capacitance | $C_{\text{HI_LO}}$ | Unpowered unit | N/A | N/A | N/A | pF |
| Isolation Resistance | $R_{\text{HI_LO}}$ | At 500V _{DC} | 0 | | | MΩ |
| MTBF | | MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer | | 2.2 | | MHrs |
| | | Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled | | 3.6 | | MHrs |
| Agency Approvals / Standards | | cTÜVus EN 60950-1 | | | | |
| | | cURus UL60950-1 | | | | |
| | | CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable | | | | |

NBM in a VIA Package

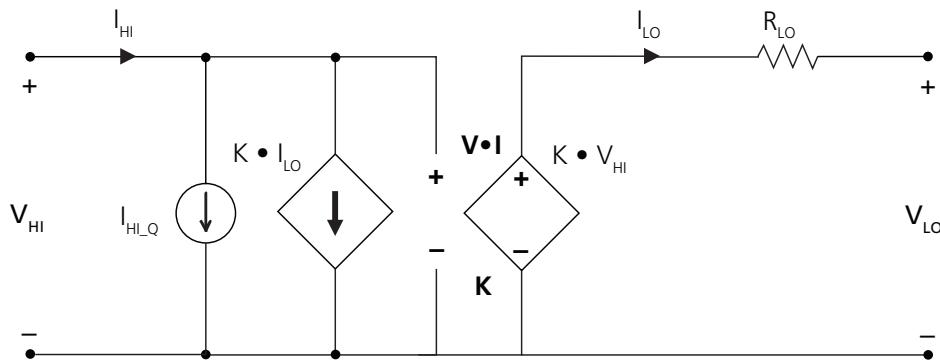


Figure 19 — NBM DC model (Forward direction)

The NBM uses a high frequency resonant tank to move energy from the high voltage side to the low voltage side and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the HI side voltage and the LO side current. A small amount of capacitance embedded in the high voltage side and low voltage side stages of the module is sufficient for full functionality and is key to achieving high power density.

The NBM3814x60E12A7yzz can be simplified into the model shown in Figure 19.

At no load:

$$V_{LO} = V_{HI} \cdot K \quad (1)$$

K represents the "turns ratio" of the NBM.

Rearranging Eq (1):

$$K = \frac{V_{LO}}{V_{HI}} \quad (2)$$

In the presence of a load, V_{LO} is represented by:

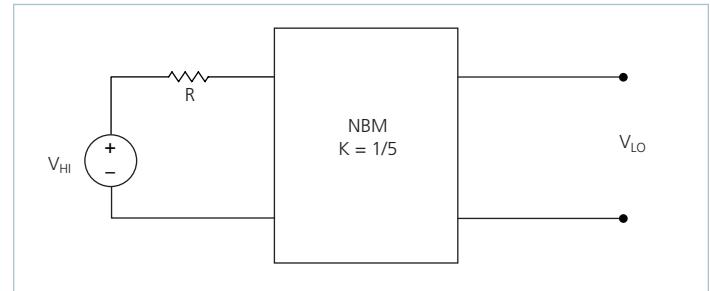
$$V_{LO} = V_{HI} \cdot K - I_{LO} \cdot R_{LO} \quad (3)$$

and I_{LO} is represented by:

$$I_{LO} = \frac{I_{HI} - I_{HI_Q}}{K} \quad (4)$$

R_{LO} represents the impedance of the NBM and is a function of the $R_{DS\text{ON}}$ of the HI side and LO side MOSFETs, PC board resistance of HI side and LO side boards and the winding resistance of the power auto-transformer. I_{HI_Q} represents the HI side quiescent current of the NBM controller, gate drive circuitry, and core losses.

The effective DC voltage transformer action provides additional interesting attributes. Assuming that $R_{LO} = 0\Omega$ and $I_{HI_Q} = 0A$, Equation 3 now becomes Equation 1 and is essentially load independent, resistor R is now placed in series with V_{HI} .

Figure 20 — $K = 1/5$ NBM with series HI side resistor

The relationship between V_{HI} and V_{LO} becomes:

$$V_{LO} = (V_{HI} - I_{HI} \cdot R) \cdot K \quad (5)$$

Substituting the simplified version of Equation 4 (I_{HI_Q} is assumed = 0A) into Equation 5 yields:

$$V_{LO} = V_{HI} \cdot K - I_{LO} \cdot R \cdot K^2 \quad (6)$$

This is similar in form to Equation 3, where R_{LO} is used to represent the characteristic impedance of the NBM. However, in this case a real resistor, R, on the high voltage side of the NBM is effectively scaled by K^2 with respect to the low voltage side.

Assuming that $R = 1\Omega$, the effective R as seen from the low voltage side is $40m\Omega$, with $K = 1/5$.

A similar exercise can be performed with the addition of a capacitor or shunt impedance at the high voltage side of the NBM. A switch in series with V_{HI} is added to the circuit. This is depicted in Figure 21.

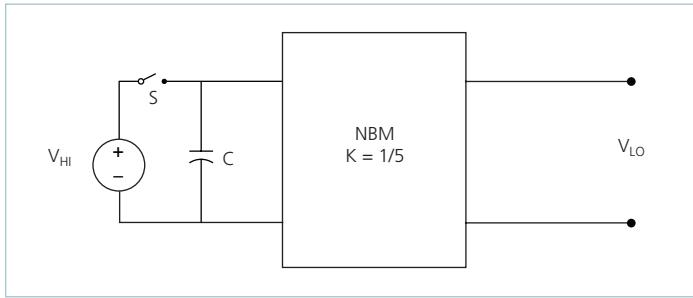


Figure 21 — NBM with HI side capacitor

A change in V_{HI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C \frac{dV_{HI}}{dt} \quad (7)$$

Assume that with the capacitor charged to V_{HI} , the switch is opened and the capacitor is discharged through the idealized NBM. In this case,

$$I_C = I_{LO} \cdot K \quad (8)$$

substituting Equation 1 and 8 into Equation 7 reveals:

$$I_{LO}(t) = \frac{C}{K^2} \cdot \frac{dV_{LO}}{dt} \quad (9)$$

The equation in terms of the LO side has yielded a K^2 scaling factor for C , specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the low voltage side when expressed in terms of the high voltage side. With a $K = 1/5$ as shown in Figure 21, $C = 1\mu F$ would appear as $C = 25\mu F$ when viewed from the low voltage side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a NBM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the NBM is too high. The impedance of the NBM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the NBM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the NBM module are:

- No load power dissipation (P_{HI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{LO}}$): refers to the power loss across the NBM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{HI_NL} + P_{R_{LO}} \quad (10)$$

Therefore,

$$P_{LO_OUT} = P_{HI_IN} - P_{DISSIPATED} = P_{HI_IN} - P_{HI_NL} - P_{R_{LO}} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{LO_OUT}}{P_{HI_IN}} = \frac{P_{HI_IN} - P_{HI_NL} - P_{R_{LO}}}{P_{HI_IN}} \quad (12)$$

$$= \frac{V_{HI} \cdot I_{HI} - P_{HI_NL} - (I_{LO})^2 \cdot R_{LO}}{V_{HI} \cdot I_{HI}}$$

$$= 1 - \left(\frac{P_{HI_NL} + (I_{LO})^2 \cdot R_{LO}}{V_{HI} \cdot I_{HI}} \right)$$

Filter Design

A major advantage of NBM systems versus conventional PWM converters is that the auto-transformer based NBM does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of HI side voltage and LO side current and efficiently transfers charge through the auto-transformer. A small amount of capacitance embedded in the high voltage side and low voltage side stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

■ **Guarantee low source impedance:**

To take full advantage of the NBM module's dynamic response, the impedance presented to its HI side terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the HI side should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1μF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

■ **Further reduce HI side and/or LO side voltage ripple without sacrificing dynamic response:**

Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the HI side source will appear at the LO side of the module multiplied by its K factor.

■ **Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:**

The module high/low side voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating HI side range. Even when disabled, the powertrain is exposed to the applied voltage and the power MOSFETs must withstand it.

Total load capacitance of the NBM module shall not exceed the specified maximum. Owing to the wide bandwidth and small LO side impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the HI side of the module. At frequencies <500kHz the module appears as an impedance of R_{LO} between the source and load.

Within this frequency range, capacitance at the HI side appears as effective capacitance on the LO side per the relationship defined in Equation 13.

$$C_{LO_EXT} = \frac{C_{HI_EXT}}{K^2} \quad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

The VIA package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the top surface, the bottom surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a VIA, as can be seen from the specified thermal operating area in Figure 1. Since the VIA has a maximum internal temperature rating, it is necessary to estimate this temperature based on a system-level thermal solution. For this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 22 shows the "thermal circuit" for the VIA module.

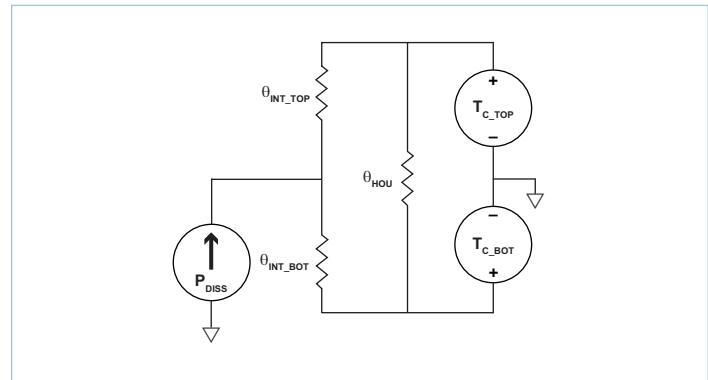


Figure 22 — Double-sided cooling VIA thermal model

In this case, the internal power dissipation is P_{DISS} , θ_{INT_TOP} and θ_{INT_BOT} are thermal resistance characteristics of the VIA module and the top and bottom surface temperatures are represented as T_{C_TOP} and T_{C_BOT} . It is interesting to note that the package itself provides a high degree of thermal coupling between the top and bottom case surfaces (represented in the model by the resistor θ_{HOU}). This feature enables two main options regarding thermal designs:

- Single side cooling: the model of Figure 22 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for bottom side cooling only is shown in Figure 23.

In this case, θ_{INT} can be derived as following:

$$\theta_{INT} = \frac{(\theta_{INT_TOP} + \theta_{HOU}) \cdot \theta_{INT_BOT}}{\theta_{INT_TOP} + \theta_{HOU} + \theta_{INT_BOT}} \quad (14)$$

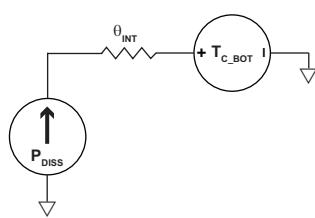


Figure 23 — Single-sided cooling VIA thermal model

- Double side cooling: while this option might bring limited advantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, like for example heatsinks with independent airflows or a combination of chassis/air cooling.

Current Sharing

The performance of the NBM is based on efficient transfer of energy through an auto-transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal auto-transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple NBM modules of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load. Ensuring equal current sharing among modules requires that NBM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes/wires within the PCB/Chassis to deliver and return the current to the modules.
- Provide as symmetric a PCB/Wiring layout as possible among modules.

For further details see:

[AN:016 Using BCM Bus Converters in High Power Arrays.](#)

Fuse Selection

In order to provide flexibility in configuring power systems, NBM in a VIA package modules are not internally fused. Input line fusing of NBM products is recommended at the system level to provide thermal protection in case of catastrophic failure.

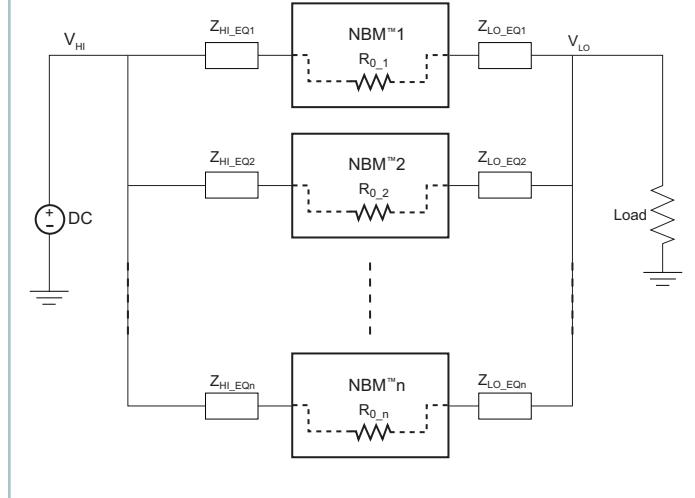


Figure 24 — NBM module array

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum current of NBM module)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: ≤60A Littelfuse TLS Series or Littlefuse 456 series rated 40A (HI side)

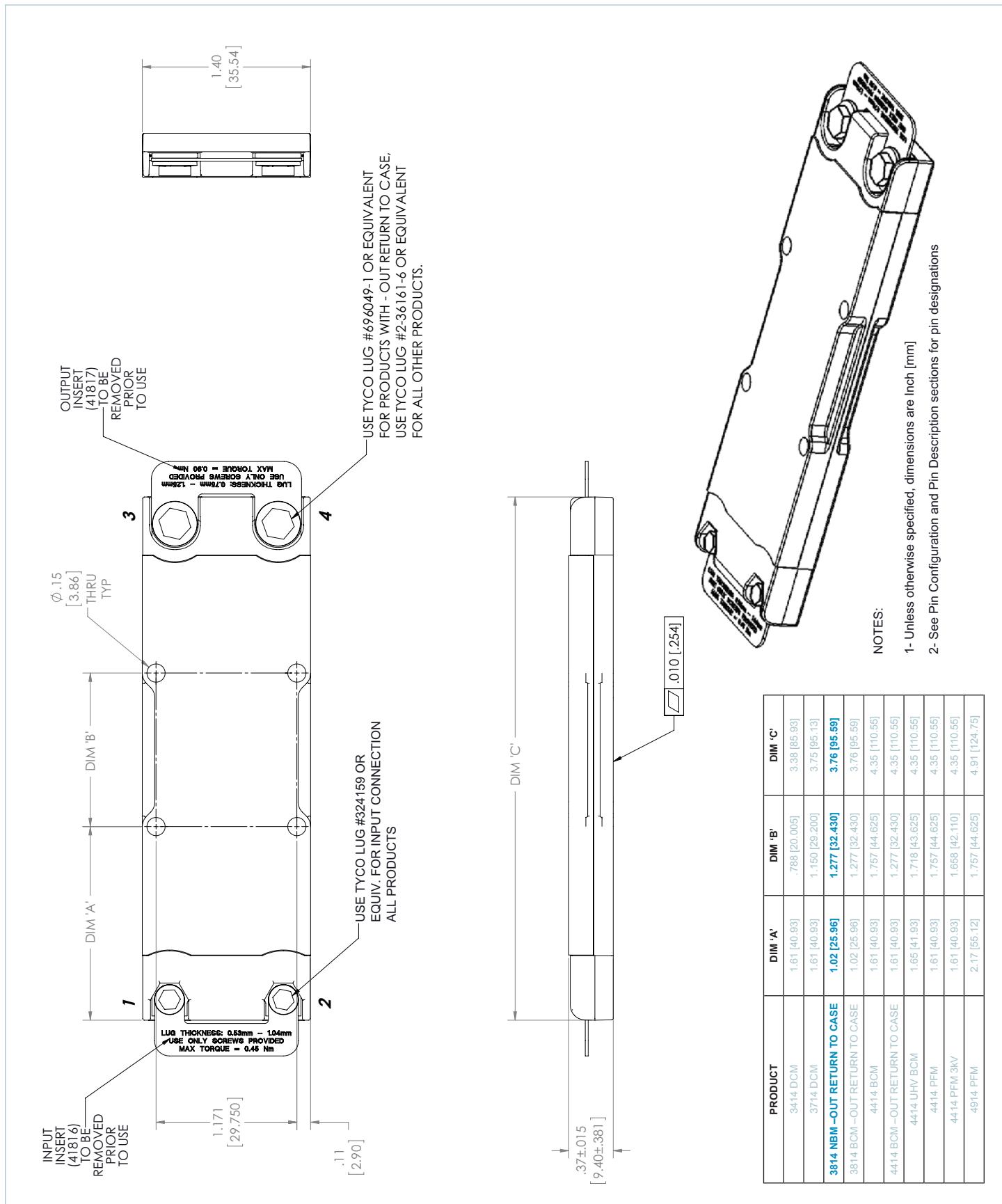
Start Up and Reverse Operation

The NBM3814x60E12A7yzz is capable of start up in forward and reverse direction once the applied voltage is greater than the undervoltage lockout threshold.

The non-isolated bus converter modules are capable of reverse power operation. Once the unit is enabled, energy can be transferred from low voltage side back to the high voltage side whenever the low side voltage exceeds $V_{HI} \cdot K$. The module will continue operation in this fashion for as long as no faults occur.

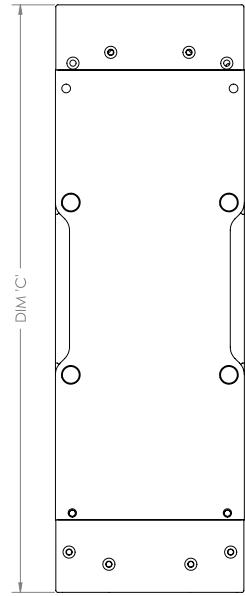
Start-up loading must be no greater than 20% of rated max current respectively in the forward or reverse direction. A load must not be present on the $+V_{HI}$ pin if the powertrain is not actively switching. High voltage side MOSFET body diode conduction will occur if the unit stops switching while a load is present on $+V_{HI}$ and $+V_{LO}$ voltage is two diodes drop higher than $+V_{HI}$. Remove $+V_{HI}$ load prior to disabling the module using $+V_{LO}$ power or prior to faults.

NBM in VIA Package Chassis (Lug) Mount Package Mechanical Drawing

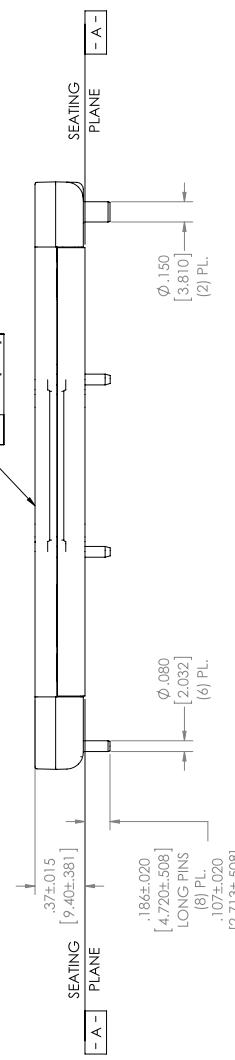


NBM in VIA Package PCB (Board) Mount Package Mechanical Drawing

| PRODUCT | DIM 'A' | DIM 'B' | DIM 'C' | DIM 'D' | DIM 'F' |
|------------------------------|--------------|----------------|---------------|-----------------|----------------|
| 3814 NBM -OUT RETURN TO CASE | 1.02 [25.96] | 1.277 [32.430] | 3.76 [95.59] | 3.368 [85.554] | .850 [21.560] |
| 3814 BOM -OUT RETURN TO CASE | 1.02 [25.96] | 1.277 [32.430] | 3.76 [95.59] | 3.368 [85.554] | .850 [21.560] |
| 4414 BOM -OUT RETURN TO CASE | 1.61 [40.93] | 1.277 [32.430] | 4.35 [110.55] | 3.957 [100.517] | 1.439 [36.554] |

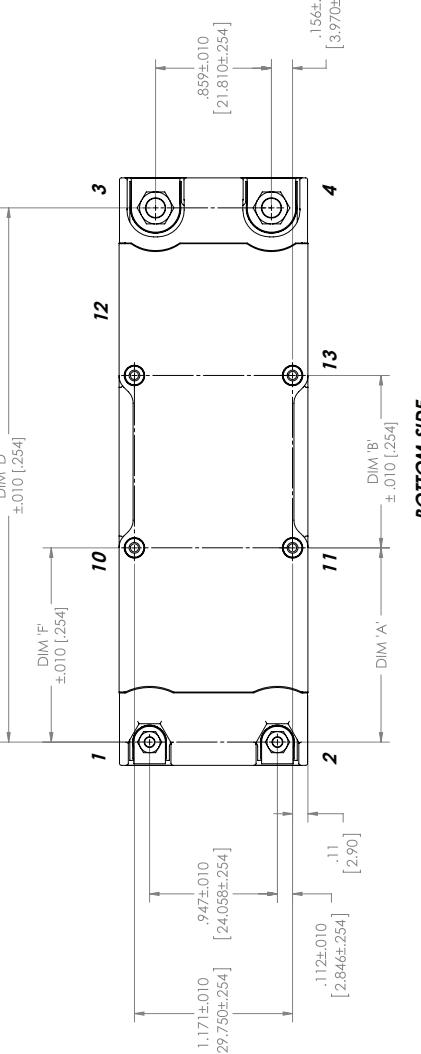


TOP VIEW
(COMPONENT SIDE)



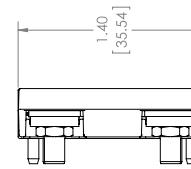
SEATING PLANE
DIM 'A' [A-]
DIM 'B'
DIM 'C'
DIM 'D'
DIM 'F' [F-]

SEATING PLANE
[.37±.015] [9.40±.351]
.186±.020 [4.720±.508]
LONG PINS (8) PL.
.107±.020 [2.713±.508]
SHORT PINS (8) PL.



BOTTOM SIDE

NOTES:
1- Unless otherwise specified, dimensions are inch [mm]
2- See Pin Configuration and Pin Description sections for pin designations



[.3970±.254]

[3.970±.254]

[.156±.010]

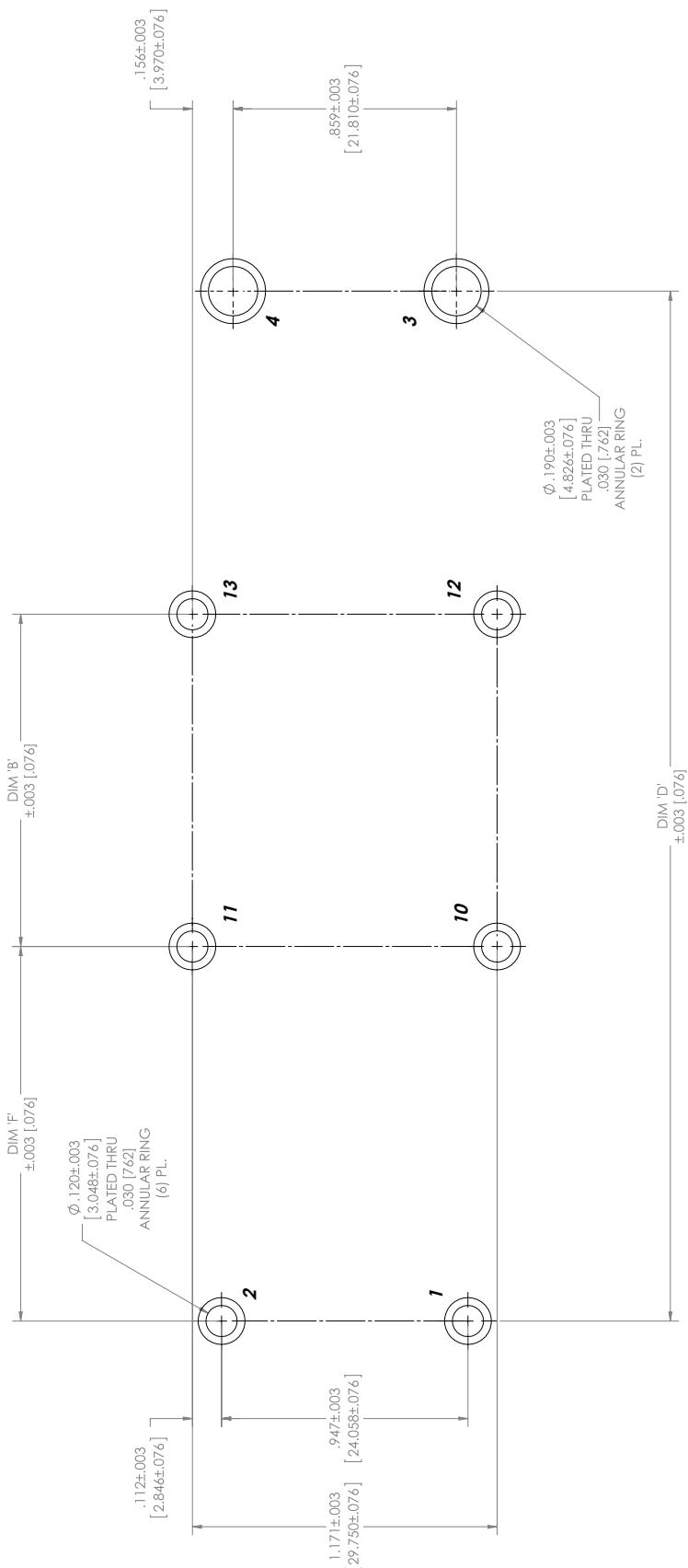
[3.554]

[1.40]

[35.54]

NBM in VIA Package PCB (Board) Mount Package Recommended Hole Pattern

| PRODUCT | DIM 'A' | DIM 'B' | DIM 'C' | DIM 'D' | DIM 'F' |
|-------------------------------------|---------------------|-----------------------|---------------------|-----------------------|----------------------|
| 3814 NBM -OUT RETURN TO CASE | 1.02 [25.96] | 1.277 [32.430] | 3.76 [95.59] | 3.368 [85.554] | .850 [21.590] |
| 3814 BOM -OUT RETURN TO CASE | 1.02 [25.96] | 1.277 [32.430] | 3.76 [95.59] | 3.368 [85.554] | .850 [21.590] |
| 4414 BOM -OUT RETURN TO CASE | 1.61 [40.93] | 1.277 [32.430] | 4.355 [110.55] | 3.957 [100.517] | 1.439 [36.554] |



RECOMMENDED HOLE PATTERN
(COMPONENT SIDE)

NOTES:

1- Unless otherwise specified, dimensions are inch [mm]

2- See Pin Configuration and Pin Description sections for pin designations

Revision History

| Revision | Date | Description | Page Number(s) |
|----------|----------|---|----------------|
| 1.0 | 03/03/16 | Initial release | n/a |
| 1.1 | 05/02/16 | New Power Pin Nomenclature | All |
| 1.2 | 04/11/17 | Content improvements Package drawings update | All 21 – 23 |
| 1.3 | 09/21/17 | Updated overcurrent protection specifications | 6, 8 |
| 1.4 | 01/24/18 | Updated mechanical drawings | 21 – 23 |
| 1.5 | | Updated agency approvals | 1, 16 |

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