

# SPANSION™ Flash Memory

## Data Sheet



September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

### **Continuity of Specifications**

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

### **Continuity of Ordering Part Numbers**

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

### **For More Information**

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.



# FLASH MEMORY

CMOS

## 2M (256K × 8) BIT

### MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

#### ■ GENERAL DESCRIPTION

The MBM29F002TC/BC is a 2 M-bit, 5.0 V-Only Flash memory organized as 256K bytes of 8 bits each. The MBM29F002TC/BC is offered in a 32-pin TSOP(1) and 32-pin PLCC packages. This device is designed to be programmed in-system with the standard system 5.0 V  $V_{CC}$  supply. A 12.0 V  $V_{PP}$  is not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard MBM29F002TC/BC offers access times between 55 ns and 90 ns allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ( $\overline{CE}$ ), write enable ( $\overline{WE}$ ), and output enable ( $\overline{OE}$ ) controls.

The MBM29F002TC/BC is command set compatible with JEDEC standard E<sup>2</sup>PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The MBM29F002TC/BC is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Each sector can be programmed and verified in less than 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

#### ■ PRODUCT LINE UP

Part No.		MBM29F002TC/BC		
Ordering Part No.	$V_{CC} = 5.0 \text{ V} \pm 5\%$	-55	—	—
	$V_{CC} = 5.0 \text{ V} \pm 10\%$	—	-70	-90
Max Address Access Time (ns)		55	70	90
Max $\overline{CE}$ Access Time (ns)		55	70	90
Max $\overline{OE}$ Access Time (ns)		30	30	35

(Continued)

This device also features a sector erase architecture. The sector erase mode allows for sectors of memory to be erased and reprogrammed without affecting other sectors. A sector is typically erased and verified within 1 second (if already completely preprogrammed). The MBM29F002TC/BC is erased when shipped from the factory.

The MBM29F002TC/BC device also features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 6).

Fujitsu has implemented an Erase Suspend feature that enables the user to put erase on hold for any period of time to read data from or program data to a non-busy sector. Thus, true background erase can be achieved.

The device features single 5.0 V power supply operation for both read and program functions. Internally generated and regulated voltages are provided for the program and erase operations. A low  $V_{CC}$  detector automatically inhibits write operations during power transitions. The end of program or erase is detected by  $\overline{\text{Data}}$  Polling of DQ<sub>7</sub>, or by the Toggle Bit I feature on DQ<sub>6</sub>. Once the end of a program or erase cycle has been completed, the device automatically resets to the read mode.

The MBM29F002TC/BC also has a hardware  $\overline{\text{RESET}}$  pin. When this pin is driven low, execution of any Embedded Program or Embedded Erase operations will be terminated. The internal state machine will then be reset into the read mode. The  $\overline{\text{RESET}}$  pin may be tied to the system reset circuitry. Therefore, if a system reset occurs during the Embedded Program or Embedded Erase operation, the device will be automatically reset to a read mode. This will enable the system microprocessor to read the boot-up firmware from the Flash memory.

Fujitsu's Flash technology combines years of EPROM and E<sup>2</sup>PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29F002TC/BC memory electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

## ■ FEATURES

- **Single 5.0 V read, write, and erase**  
Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**  
Pinout and software compatible with single-power supply Flash  
Superior inadvertent write protection
- **32-pin TSOP(1) (Package Suffix: PFTN-Normal Bend Type, PFTR-Reverse Bend Type)**  
**32-pin PLCC (Package Suffix: PD)**
- **Minimum 100,000 write/erase cycles**
- **High performance**  
55 ns maximum access time
- **Sector erase architecture**  
One 16K byte, two 8K bytes, one 32K byte, and three 64K bytes  
Any combination of sectors can be erased. Also supports full chip erase
- **Boot Code Sector Architecture**  
T = Top sector  
B = Bottom sector
- **Embedded Erase™\* Algorithms**  
Automatically pre-programs and erases the chip or any sector
- **Embedded Program™\* Algorithms**  
Automatically programs and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**

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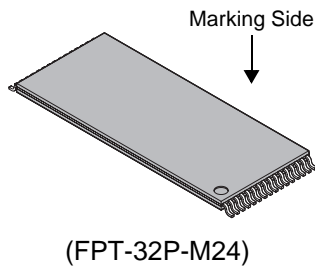
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- **Low  $V_{CC}$  write inhibit  $\leq 3.2$  V**
- **Hardware  $\overline{RESET}$  pin**  
Resets internal state machine to the read mode
- **Erase Suspend/Resume**  
Supports reading or programming data to a sector not being erased
- **Sector protection**  
Hardware method that disables any combination of sector from write or erase operation
- **Temporary sector unprotection**  
Temporary sector unprotection via the  $\overline{RESET}$  pin

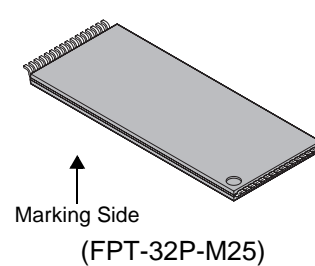
\* : Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

## ■ PACKAGES

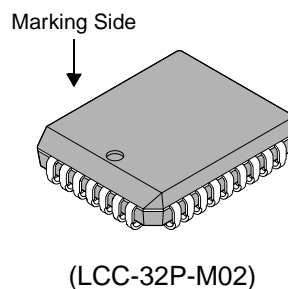
32-pin plastic TSOP(1)



32-pin plastic TSOP(1)

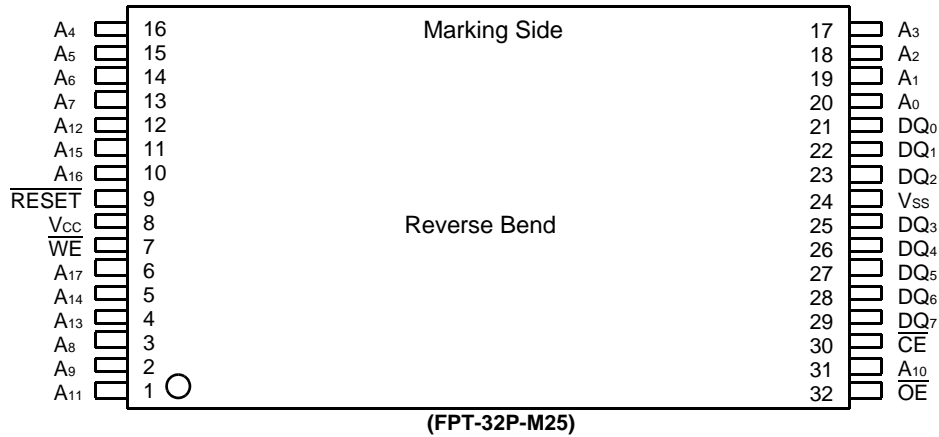
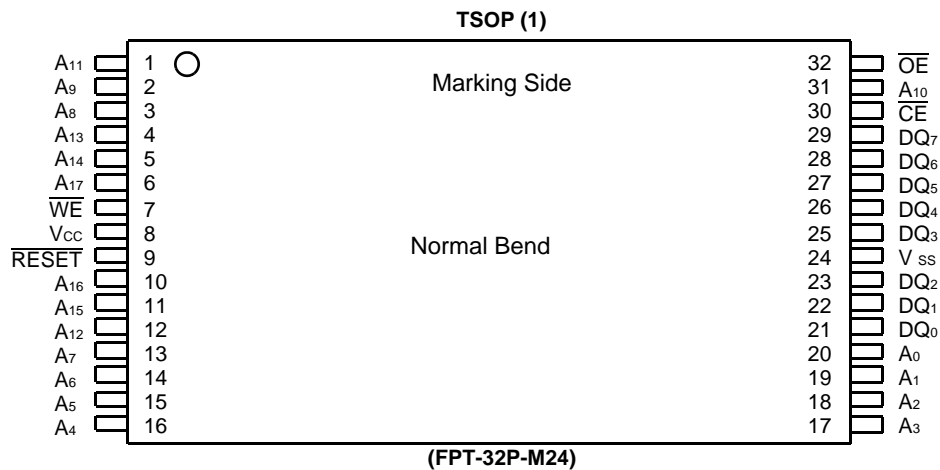


32-pin plastic QFJ (PLCC)



# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

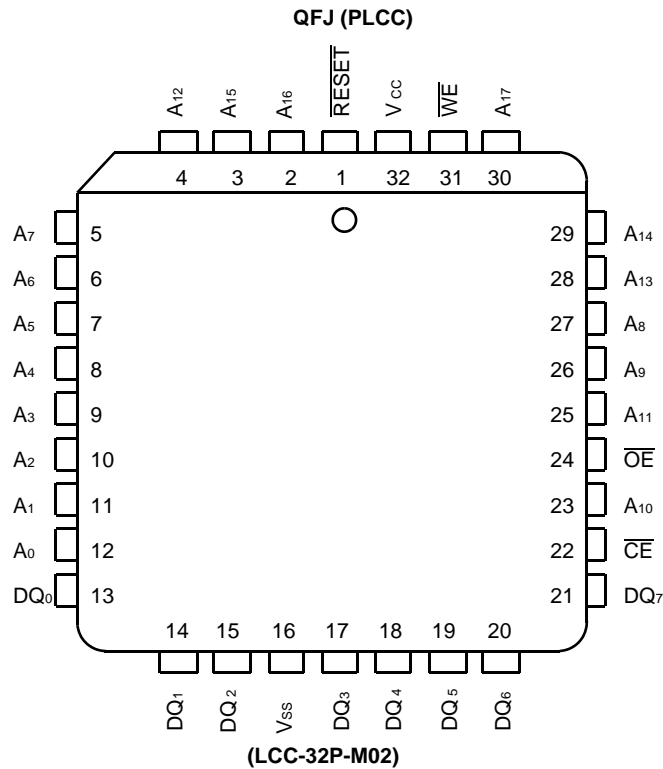
## ■ PIN ASSIGNMENTS



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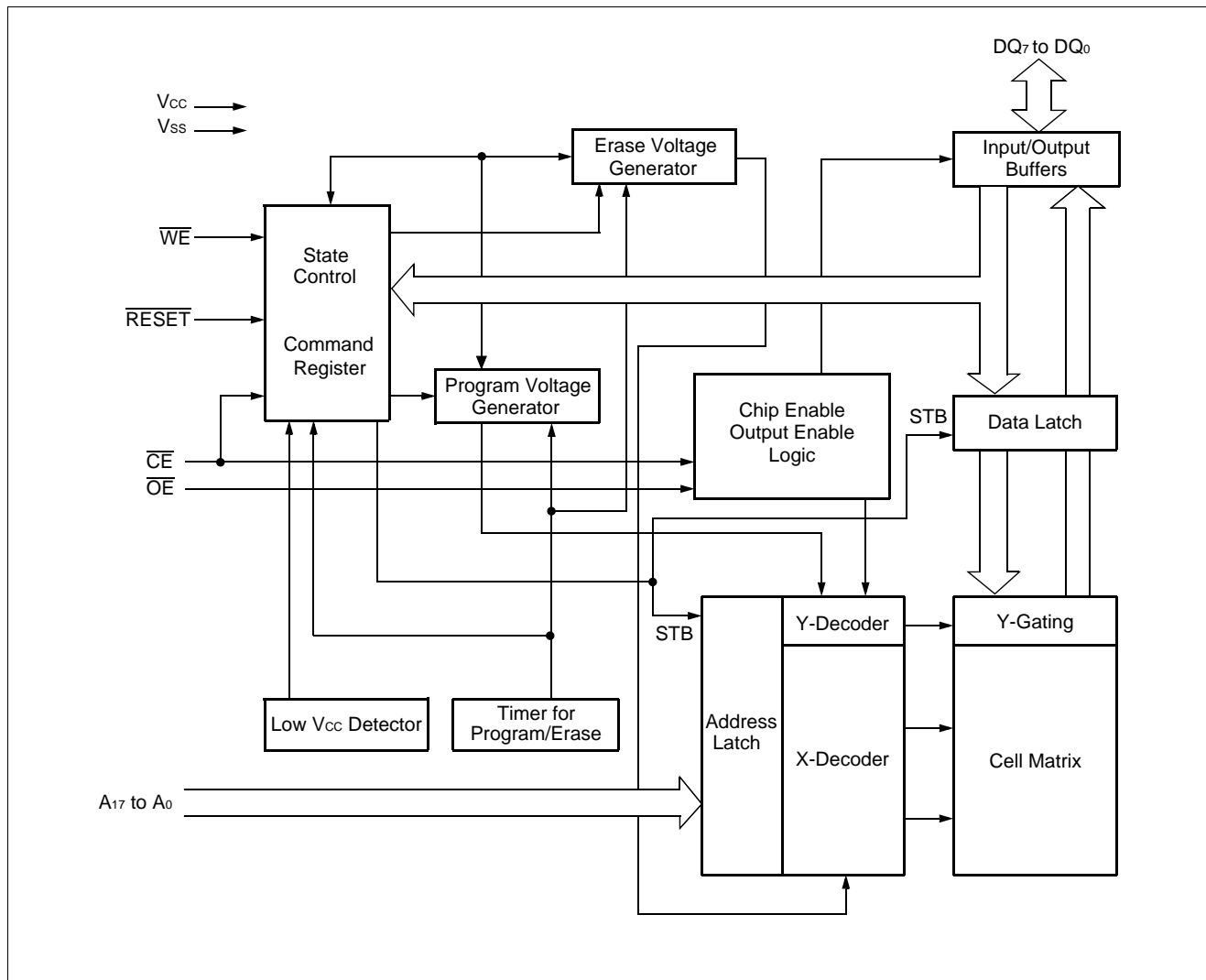
# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

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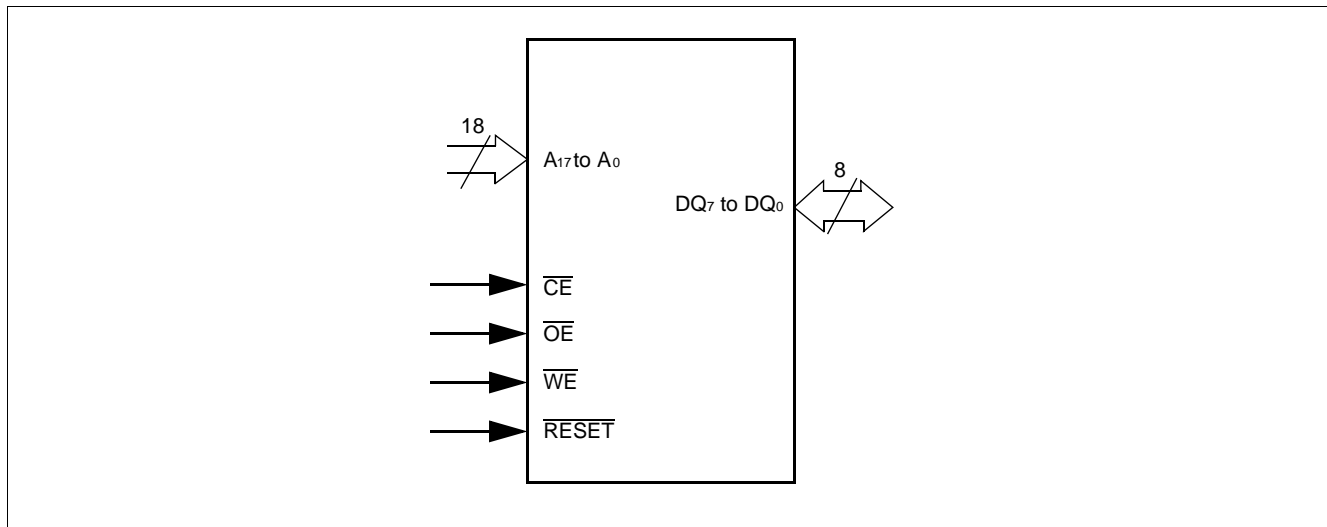


Pin	Function
A <sub>17</sub> to A <sub>0</sub>	Address Inputs
DQ <sub>7</sub> to DQ <sub>0</sub>	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RESET}}$	Hardware Reset Pin/Sector Protection Unlock
N.C.	No Internal Connection
V <sub>SS</sub>	Device Ground
V <sub>CC</sub>	Device Power Supply

## ■ BLOCK DIAGRAM




## ■ LOGIC SYMBOL



## ■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 16K byte, two 8K bytes, one 32K byte, and three 64K bytes
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable

**MBM29F002TC/BC User Bus Operations**

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A <sub>0</sub>	A <sub>1</sub>	A <sub>6</sub>	A <sub>9</sub>	A <sub>10</sub>	DQ <sub>7</sub> to DQ <sub>0</sub>	$\overline{RESET}$
Auto-Select Manufacturer Code* <sup>1</sup>	L	L	H	L	L	L	V <sub>ID</sub>	L	Code	H
Auto-Select Device Code* <sup>1</sup>	L	L	H	H	L	L	V <sub>ID</sub>	L	Code	H
Read* <sup>3</sup>	L	L	H	A <sub>0</sub>	A <sub>1</sub>	A <sub>6</sub>	A <sub>9</sub>	A <sub>10</sub>	D <sub>OUT</sub>	H
Standby	H	X	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	A <sub>0</sub>	A <sub>1</sub>	A <sub>6</sub>	A <sub>9</sub>	A <sub>10</sub>	D <sub>IN</sub>	H
Enable Sector Protection* <sup>2</sup>	L	V <sub>ID</sub>		X	X	X	V <sub>ID</sub>	X	X	H
Verify Sector Protection* <sup>2</sup>	L	L	H	L	H	L	V <sub>ID</sub>	L	Code	H
Temporary Sector Unprotection	X	X	X	X	X	X	X	X	X	V <sub>ID</sub>
Reset (Hardware)	X	X	X	X	X	X	X	X	High-Z	L

**Legend:** L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = V<sub>IL</sub> or V<sub>IH</sub>,  = Pulse Input. See DC Characteristics for voltage levels.

\*1 : Manufacturer and device codes may also be accessed via a command register write sequence. Refer to “MBM29F002TC/BC Command Definitions Table” in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE”.

\*2 : Refer to the section on Sector Protection.

\*3 :  $\overline{WE}$  can be V<sub>IL</sub> if  $\overline{OE}$  is V<sub>IL</sub>,  $\overline{OE}$  at V<sub>IH</sub> initiates the write operations.



# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

**MBM29F002TC/BC Command Definitions**

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset*1	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Reset/Read*1	3	555h	AAh	2AAh	55h	555h	F0h	RA*2	RD*2	—	—	—	—
Manufacture Code	3	555h	AAh	2AAh	55h	555h	90h	00h*2	04h*2	—	—	—	—
Device Code	3	555h	AAh	2AAh	55h	555h	90h	01h*2	ID*2	—	—	—	—
Byte Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
Sector Erase Suspend	Erase can be suspended during sector erase with Addr ("H" or "L"), Data (B0h)												
Sector Erase Resume	Erase can be resumed after suspend with Addr ("H" or "L"), Data (30h)												

\*1 : Either of the two reset commands will reset the device.

\*2 : The fourth bus cycle is only for read.

- Notes :
- Address bits A<sub>17</sub> to A<sub>11</sub> = X = "H" or "L" for all address commands except or Program Address (PA) and Sector Address (SA).
  - Bus operations are defined in "MBM29F002TC/BC User Bus Operations Table" in "■ FLEXIBLE SECTOR-ERASE ARCHITECTURE".
  - RA = Address of the memory location to be read.  
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the  $\overline{WE}$  pulse.  
SA = Address of the sector to be erased. The combination of A<sub>17</sub>, A<sub>16</sub>, A<sub>15</sub>, A<sub>14</sub>, and A<sub>13</sub> will uniquely select any sector.
  - RD = Data read from location RA during read operation.  
PD = Data to be programmed at location PA. Data is latched on the rising edge of  $\overline{WE}$ .  
ID = Device Code (Refer to the section on Sector Protection Verify Autoselect Codes.)
  - The command combinations not described in "MBM29F002TC/BC Command Definitions Table" in "■ FLEXIBLE SECTOR-ERASE ARCHITECTURE" are illegal.

**MBM29F002TC/BC Sector Protection Verify Autoselect Codes**

Type		A <sub>17</sub> to A <sub>13</sub>	A <sub>10</sub>	A <sub>6</sub>	A <sub>1</sub>	A <sub>0</sub>	Code (HEX)
Manufacture's Code		X	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	04h
Device Code	MBM29F002TC	X	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	B0h
	MBM29F002BC	X	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	34h
Sector Protection		Sector Addresses	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	01h*

\* : Outputs 01h at protected sector addresses and outputs 00h at unprotected sector addresses.

# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

Extended Autoselect Code Table

Type		Code	DQ <sub>7</sub>	DQ <sub>6</sub>	DQ <sub>5</sub>	DQ <sub>4</sub>	DQ <sub>3</sub>	DQ <sub>2</sub>	DQ <sub>1</sub>	DQ <sub>0</sub>
Manufacture's Code		04h	0	0	0	0	0	1	0	0
Device Code	MBM29F002TC	B0h	1	0	1	1	0	0	0	0
	MBM29F002BC	34h	0	0	1	1	0	1	0	0
Sector Protection		01h	0	0	0	0	0	0	0	1

Sector Address Table (MBM29F002TC)

	A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	Address Range
SA0	0	0	X	X	X	00000h to 0FFFFh
SA1	0	1	X	X	X	10000h to 1FFFFh
SA2	1	0	X	X	X	20000h to 2FFFFh
SA3	1	1	0	X	X	30000h to 37FFFh
SA4	1	1	1	0	0	38000h to 39FFFh
SA5	1	1	1	0	1	3A000h to 3BFFFh
SA6	1	1	1	1	X	3C000h to 3FFFFh

Sector Address Table (MBM29F002BC)

	A <sub>17</sub>	A <sub>16</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	Address Range
SA0	0	0	0	0	X	00000h to 03FFFh
SA1	0	0	0	1	0	04000h to 05FFFh
SA2	0	0	0	1	1	06000h to 07FFFh
SA3	0	0	1	X	X	08000h to 0FFFFh
SA4	0	1	X	X	X	10000h to 1FFFFh
SA5	1	0	X	X	X	20000h to 2FFFFh
SA6	1	1	X	X	X	30000h to 3FFFFh

**Sector Architecture**

16K byte	3FFFFh
8K byte	3BFFFh
8K byte	39FFFh
32K byte	37FFFh
64K byte	2FFFFh
64K byte	1FFFFh
64K byte	0FFFFh
64K byte	00000h

**MBM29F002TC Sector Architecture**

64K byte	3FFFFh
64K byte	2FFFFh
64K byte	1FFFFh
64K byte	0FFFFh
32K byte	07FFFh
8K byte	05FFFh
8K byte	03FFFh
16K byte	00000h

**MBM29F002BC Sector Architecture**

## ■ FUNCTIONAL DESCRIPTION

### Read Mode

The MBM29F002TC/BC has two control functions which must be satisfied in order to obtain data at the outputs.  $\overline{CE}$  is the power control and should be used for a device selection.  $\overline{OE}$  is the output control and should be used to gate data to the output pins if a device is selected.

Address access time ( $t_{ACC}$ ) is equal to the delay from stable addresses to valid output data. The chip enable access time ( $t_{CE}$ ) is the delay from stable addresses and stable  $\overline{CE}$  to valid data at the output pins. The output enable access time is the delay from the falling edge of  $\overline{OE}$  to valid data at the output pins (assuming the addresses have been stable for at least  $t_{ACC-tOE}$  time).

### Standby Mode

There are two ways to implement the standby mode on the MBM29F002TC/BC devices, one using both the  $\overline{CE}$  and  $\overline{RESET}$  pins; the other via the  $\overline{RESET}$  pin only.

When using both pins, a CMOS standby mode is achieved with  $\overline{CE}$  and  $\overline{RESET}$  inputs both held at  $V_{CC} \pm 0.3$  V. Under this condition the current consumed is less than 5  $\mu$ A. A TTL standby mode is achieved with  $\overline{CE}$  and  $\overline{RESET}$  pins held at  $V_{IH}$ . Under this condition the current is reduced to approximately 1 mA. During Embedded Algorithm operation,  $V_{CC}$  Active current ( $I_{CC2}$ ) is required even  $\overline{CE} = V_{IH}$ . The device can be read with standard access time ( $t_{CE}$ ) from either of these standby modes.

When using the  $\overline{RESET}$  pin only, a CMOS standby mode is achieved with  $\overline{RESET}$  input held at  $V_{SS} \pm 0.3$  V ( $\overline{CE} = "H"$  or  $"L"$ ). Under this condition the current consumed is less than 5  $\mu$ A. A TTL standby mode is achieved with  $\overline{RESET}$  pin held at  $V_{IL}$  ( $\overline{CE} = "H"$  or  $"L"$ ). Under this condition the current required is reduced to approximately 1 mA. Once the  $\overline{RESET}$  pin is taken high, the device requires 500 ns of wake up time before outputs are valid for read access.

In the standby mode the outputs are in the high impedance state, independent of the  $\overline{OE}$  input.

### Output Disable

With the  $\overline{OE}$  input at a logic high level ( $V_{IH}$ ), output from the device is disabled. This will cause the output pins to be in a high impedance state.

### Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force  $V_{ID}$  (11.5 V to 12.5 V) on address pin  $A_9$ . Two identifier bytes may then be sequenced from the device outputs by toggling address  $A_0$  from  $V_{IL}$  to  $V_{IH}$ . All addresses are don't cares except  $A_0$ ,  $A_1$ ,  $A_6$  and  $A_{10}$ . (See "MBM29F002TC/BC Sector Protection Verify Autoselect Code Table" and "Extended Autoselect Code Table" in "■ FLEXIBLE SECTOR-ERASE ARCHITECTURE".)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29F002TC/BC is erased or programmed in a system without access to high voltage on the  $A_9$  pin. The command sequence is illustrated in "MBM29F002TC/BC Command Definitions Table" in "■ FLEXIBLE SECTOR-ERASE ARCHITECTURE". (Refer to Autoselect Command section.)

Byte 0 ( $A_0 = V_{IL}$ ) represents the manufacturer's code (Fujitsu = 04h) and byte 1 ( $A_0 = V_{IH}$ ) represents the device identifier code for MBM29F002TC = B0h, MBM29F002BC = 34h. These two bytes are given in the "MBM29F002TC/BC Sector Protection Verify Autoselect Code Table" and "Extended Autoselect Code Table" in "■ FLEXIBLE SECTOR-ERASE ARCHITECTURE". All identifiers for manufactures and device will exhibit odd parity with  $DQ_7$  defined as the parity bit. In order to read the proper device codes when executing the Autoselect,

A<sub>1</sub> must be V<sub>IL</sub>. (See “MBM29F002TC/BC Sector Protection Verify Autoselect Code Table” and “Extended Autoselect Code Table” in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE”.)

The Autoselect mode also facilitates the determination of sector protection in the system. By performing a read operation at the address location XX02h with the higher order address bits A<sub>13</sub>, A<sub>14</sub>, A<sub>15</sub>, A<sub>16</sub> and A<sub>17</sub> set to the desired sector address, the device will return 01h for a protected sector and 00h for a non-protected sector.

## Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing  $\overline{WE}$  to V<sub>IL</sub>, while  $\overline{CE}$  is at V<sub>IL</sub> and  $\overline{OE}$  is at V<sub>IH</sub>. Addresses are latched on the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever happens later; while data is latched on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

## Sector Protection

The MBM29F002TC/BC features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 6). The sector protection feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V<sub>ID</sub> on address pin A<sub>9</sub> and control pin  $\overline{OE}$ , (suggest V<sub>ID</sub> = 11.5 V),  $\overline{CE}$  = V<sub>IL</sub>. The sector addresses (A<sub>13</sub>, A<sub>14</sub>, A<sub>15</sub>, A<sub>16</sub>, and A<sub>17</sub>) should be set to the sector to be protected. “Sector Address Table (MBM29F002TC)” and “Sector Address Table (MBM29F002BC)” in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE”. define the sector address for each of the seven (7) individual sectors. Programming of the protection circuitry begins on the falling edge of the  $\overline{WE}$  pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the  $\overline{WE}$  pulse. See “AC Waveforms for Sector Protection Timing Diagram” in “■ TIMING DIAGRAM” and “Sector Protection Algorithm” in “■ FLOW CHART” for sector protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V<sub>ID</sub> on address pin A<sub>9</sub> with  $\overline{CE}$  and  $\overline{OE}$  at V<sub>IL</sub> and  $\overline{WE}$  at V<sub>IH</sub>. Scanning the sector addresses (A<sub>13</sub>, A<sub>14</sub>, A<sub>15</sub>, A<sub>16</sub>, and A<sub>17</sub>) while (A<sub>10</sub>, A<sub>6</sub>, A<sub>1</sub>, A<sub>0</sub>) = (0, 0, 1, 0) will produce a logical “1” code at device output DQ<sub>0</sub> for a protected sector. Otherwise the device will produce 00h for unprotected sector. In this mode, the lower order addresses, except for A<sub>0</sub>, A<sub>1</sub>, A<sub>6</sub>, and A<sub>10</sub> are DON'T CARES. Address locations with A<sub>1</sub> = V<sub>IL</sub> are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses (A<sub>13</sub>, A<sub>14</sub>, A<sub>15</sub>, A<sub>16</sub>, and A<sub>17</sub>) are the desired sector address will produce a logical “1” at DQ<sub>0</sub> for a protected sector. See “MBM29F002TC/BC Sector Protection Verify Autoselect Code Table” and “Extended Autoselect Code Table” in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE” for Autoselect codes.

## Temporary Sector Unprotection

This feature allows temporary unprotection of previously protected sectors of the MBM29F002TC/BC device in order to change data. The Sector Unprotection mode is activated by setting the  $\overline{RESET}$  pin to high voltage (12 V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the 12 V is taken away from the  $\overline{RESET}$  pin, all the previously protected sectors will be protected again. See “Temporary Sector Unprotection Timing Diagram” in “■ TIMING DIAGRAM” and “Temporary Sector Unprotection Algorithm” in “■ FLOW CHART”.

## Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. “MBM29F002TC/BC Command Definitions Table” in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE” defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover, both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

## Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

## Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising  $A_9$  to a high voltage. However, multiplexing high voltage onto the address lines is not generally desirable system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00h retrieves the manufacture code of 04h. A read cycle from address XX01h returns the device code D5h. (See “MBM29F002TC/BC Sector Protection Verify Autoselect Code Table” and “Extended Autoselect Code Table” in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE”).

All manufacturer and device codes will exhibit odd parity with the  $DQ_7$  defined as the parity bit.

Sector state (protection or unprotection) will be informed by address XX02h.

Scanning the sector addresses ( $A_{17}$ ,  $A_{16}$ ,  $A_{15}$ ,  $A_{14}$ , and  $A_{13}$ ) while ( $A_{10}$ ,  $A_6$ ,  $A_1$ ,  $A_0$ ) = (0, 0, 1, 0) will produce a logical “1” at device output  $DQ_0$  for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register and also to write the Autoselect command during the operation, execute it after writing Read/Reset command sequence.

## Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever happens later and the data is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever happens first. The rising edge of  $\overline{CE}$  or  $\overline{WE}$  (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

This automatic programming operation is completed when the data on  $DQ_7$  is equivalent to data written to this bit at which time the device returns to the read mode and addresses are no longer latched. (See “Hardware Sequence Flags Table” in “■ FUNCTIONAL DESCRIPTION”). Therefore, the device requires that a valid address

to the device be supplied by the system at this particular instance of time.  $\overline{\text{Data}}$  Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored. If a hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

“Embedded Erase™ Algorithm” in “■ FLOW CHART” illustrates the Embedded Programming™ Algorithm using typical command strings and bus operations.

## Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last  $\overline{\text{WE}}$  pulse in the command sequence and terminates when the data on DQ<sub>7</sub> is “1” (see Write Operation Status section) at which time the device returns to read the mode.

“Data Polling Algorithm” in “■ FLOW CHART” illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

## Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of  $\overline{\text{WE}}$ , while the command (Data = 30h) is latched on the rising edge of  $\overline{\text{WE}}$ . After time-out of 50  $\mu\text{s}$  from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on “MBM29F002TC/BC Command Definitions Table” in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE”. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50  $\mu\text{s}$  otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50  $\mu\text{s}$  from the rising edge of the last  $\overline{\text{WE}}$  will initiate the execution of the Sector Erase command(s). If another falling edge of the  $\overline{\text{WE}}$  occurs within the 50  $\mu\text{s}$  time-out window the timer is reset. (Monitor DQ<sub>3</sub> to determine if the sector erase timer window is still open, see section DQ<sub>3</sub>, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun will corrupt the data in that sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for DQ<sub>3</sub>, Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 6).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the



remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 50  $\mu$ s time out from the rising edge of the  $\overline{WE}$  pulse for the last sector erase command pulse and terminates when the data on DQ<sub>7</sub> is “1” (see Write Operation Status section) at which time the device returns to the read mode.  $\overline{Data}$  polling must be performed at an address within any of the sectors being erased.

“ $\overline{Data}$  Polling Algorithm” in “■ FLOW CHART” illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

## Erase Suspend

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during a Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writing the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Any other command written during the Erase Suspend mode will be ignored except the Erase Resume command. Writing the Erase Resume command resumes the erase operation. The addresses are DON'T CARES when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 15  $\mu$ s to suspend the erase operation. When the device has entered the erase-suspended mode, the DQ<sub>7</sub> bit will be at logic “1”, and DQ<sub>6</sub> will stop toggling. The user must use the address of the erasing sector for reading DQ<sub>6</sub> and DQ<sub>7</sub> to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ<sub>2</sub> to toggle. (See the section on DQ<sub>2</sub>.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Byte Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Byte Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode will cause DQ<sub>2</sub> to toggle. The end of the erase-suspended program operation is detected by  $\overline{Data}$  polling of DQ<sub>7</sub>, or by the Toggle Bit I (DQ<sub>6</sub>) which is the same as the regular Byte Program operation. Note that DQ<sub>7</sub> must be read from the Byte Program address while DQ<sub>6</sub> can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



## Write Operation Status

Status			DQ <sub>7</sub>	DQ <sub>6</sub>	DQ <sub>5</sub>	DQ <sub>3</sub>	DQ <sub>2</sub>
In Progress	Embedded Program Algorithm		$\overline{\text{DQ}}_7$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle* <sup>1</sup>
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{\text{DQ}}_7$	Toggle* <sup>2</sup>	0	0	1* <sup>3</sup>
Exceeded Time Limits	Embedded Program Algorithm		$\overline{\text{DQ}}_7$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{\text{DQ}}_7$	Toggle	1	0	N/A

\*1 : Performing successive read operations from the erase-suspended sector will cause DQ<sub>2</sub> to toggle.

\*2 : Performing successive read operations from any address will cause DQ<sub>6</sub> to toggle.

\*3 : Reading the byte address being programmed while in the erase-suspend program mode will indicate logic “1” at the DQ<sub>2</sub> bit. However, successive reads from the erase-suspended sector will cause DQ<sub>2</sub> to toggle.

## DQ<sub>7</sub>

### Data Polling

The MBM29F002TC/BC device features  $\overline{\text{Data}}$  Polling as a method to indicate to the host that the embedded algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DQ<sub>7</sub>. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ<sub>7</sub>. During the Embedded Erase™ Algorithm, an attempt to read the device will produce a “0” at the DQ<sub>7</sub> output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a “1” at the DQ<sub>7</sub> output. The flowchart for  $\overline{\text{Data}}$  Polling (DQ<sub>7</sub>) is shown in “Toggle Bit I Algorithm” in “■ FLOW CHART”.

$\overline{\text{Data}}$  polling will also flag the entry into Erase Suspend. DQ<sub>7</sub> will switch “0” to “1” at the start of the Erase Suspend mode. Please note that the address of an erasing sector must be applied in order to observe DQ<sub>7</sub> in the Erase Suspend Mode.

During Program in Erase Suspend,  $\overline{\text{Data}}$  polling will perform the same as in regular program execution outside of the suspend mode.

For chip erase, the  $\overline{\text{Data}}$  Polling is valid after the rising edge of the sixth  $\overline{\text{WE}}$  pulse in the six write pulse sequence. For sector erase, the  $\overline{\text{Data}}$  Polling is valid after the last rising edge of the sector erase  $\overline{\text{WE}}$  pulse.  $\overline{\text{Data}}$  Polling must be performed at sector address within any of the sectors being erased and not a sector that is within a protected sector. Otherwise, the status may not be valid.

Just prior to the completion of Embedded Algorithm operation DQ<sub>7</sub> may change asynchronously while the output enable ( $\overline{\text{OE}}$ ) is asserted low. This means that the device is driving status information on DQ<sub>7</sub> at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ<sub>7</sub> output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ<sub>7</sub> has a valid data, the data outputs on DQ<sub>6</sub> to DQ<sub>0</sub> may be still invalid. The valid data on DQ<sub>7</sub> to DQ<sub>0</sub> will be read on the successive read attempts.

The  $\overline{\text{Data}}$  Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspend, erase-suspend-program mode, or sector erase time-out. (See “Hardware Sequence Flags Table” in “■ FUNCTIONAL DESCRIPTION”.)

See “AC waveforms for  $\overline{\text{Data}}$  Polling during Embedded Algorithm Operations” in “■ TIMING DIAGRAM” for the  $\overline{\text{Data}}$  Polling timing specifications and diagrams.

## DQ<sub>6</sub>

### Toggle Bit I

The MBM29F002TC/BC also features the “Toggle Bit I” as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ( $\overline{\text{OE}}$  toggling) data from the device *at any address* will result in DQ<sub>6</sub> toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ<sub>6</sub> will stop toggling and valid data will be read on *the next* successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth  $\overline{\text{WE}}$  pulse in the four write pulse sequence. For chip erase, and sector erase the Toggle Bit I is valid after the rising edge of the sixth  $\overline{\text{WE}}$  pulse in the six write pulse sequence. For Sector Erase, the Toggle Bit I is valid after the last rising edge of the sector erase  $\overline{\text{WE}}$  pulse. The Toggle Bit I is active during the sector erase time out.

In programming, if the sector being written to is protected, the Toggle Bit I will toggle for about 2  $\mu\text{s}$  and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the Toggle Bit I for about 100  $\mu\text{s}$  and then drop back into read mode, having changed none of the data.

Either  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  toggling will cause the DQ<sub>6</sub> to toggle. In addition, an Erase Suspend/Resume command will cause DQ<sub>6</sub> to toggle.

See “AC waveforms for Toggle Bit I during Embedded Algorithm Operations” in “■ TIMING DIAGRAM” for the Toggle Bit I timing specifications and diagrams.

## DQ<sub>5</sub>

### Exceeded Timing Limits

DQ<sub>5</sub> will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ<sub>5</sub> will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed.  $\overline{\text{Data}}$  Polling DQ<sub>7</sub>, DQ<sub>6</sub> is the only operating function of the device under this condition. The  $\overline{\text{CE}}$  circuit will partially power down the device under these conditions (to approximately 2 mA). The  $\overline{\text{OE}}$  and  $\overline{\text{WE}}$  pins will control the output disable functions as described in “MBM29F002TC/BC User Bus Operations Table” in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE”.

The DQ<sub>5</sub> failure condition may also appear if a user tries to program a 1 to a location that is previously programmed to 0. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ<sub>7</sub> bit and DQ<sub>6</sub> never stops toggling. Once the device has exceeded timing limits, the DQ<sub>5</sub> bit will indicate a “1.” Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device.

## DQ<sub>3</sub>

### Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ<sub>3</sub> will remain low until the time-out is complete.  $\overline{\text{Data}}$  Polling and Toggle Bit I are valid after the initial sector erase command sequence.

If  $\overline{\text{Data}}$  Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ<sub>3</sub> may be used to determine if the sector erase timer window is still open. If DQ<sub>3</sub> is high (“1”) the internally controlled

erase cycle has begun; attempts to write subsequent commands (other than Erase Suspend) to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit I. If DQ<sub>3</sub> is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ<sub>3</sub> prior to and following each subsequent sector erase command. If DQ<sub>3</sub> were high on the second status check, the command may not have been accepted.

Refer to "Hardware Sequence Flags Table" in "■ FUNCTIONAL DESCRIPTION".

## DQ<sub>2</sub>

### Toggle Bit II

This toggle bit II, along with DQ<sub>6</sub>, can be used to determine whether the device is in the Embedded Erase™ Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ<sub>2</sub> to toggle during the Embedded Erase™ Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ<sub>2</sub> to toggle. When the device is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic "1" at the DQ<sub>2</sub> bit.

Mode	DQ <sub>7</sub>	DQ <sub>6</sub>	DQ <sub>2</sub>
Program	$\overline{\text{DQ}}_7$	Toggle	1
Erase	0	Toggle	Toggle
Erase Suspend Read *1 (Erase-Suspended Sector)	1	1	Toggle
Erase Suspend Program	$\overline{\text{DQ}}_7$ *2	Toggle	1*2

\*1 : These status flags apply when outputs are read from a sector that has been erase-suspended.

\*2 : These status flags apply when outputs are read from the byte address of the non-erase suspended sector.

DQ<sub>6</sub> is different from DQ<sub>2</sub> in that DQ<sub>6</sub> toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ<sub>7</sub>, is summarized as follows:

For example, DQ<sub>2</sub> and DQ<sub>6</sub> can be used together to determine the erase-suspend-read mode (DQ<sub>2</sub> toggles while DQ<sub>6</sub> does not). See also "Hardware Sequence Flags Table" in "■ FUNCTIONAL DESCRIPTION" and "Embedded Program™ Algorithm" in "■ FLOW CHART".

Furthermore, DQ<sub>2</sub> can also be used to determine which sector is being erased. When the device is in the erase mode, DQ<sub>2</sub> toggles if this bit is read from the erasing sector.

## RESET

### Hardware Reset

The MBM29F002TC/BC device may be reset by driving the  $\overline{\text{RESET}}$  pin to V<sub>IL</sub>. The  $\overline{\text{RESET}}$  pin must be kept low (V<sub>IL</sub>) for at least 500 ns. Any operation in progress will be terminated and the internal state machine will be reset to the read mode 20 μs after the  $\overline{\text{RESET}}$  pin is driven low. If a hardware reset occurs during a program operation, the data at that particular location will be indeterminate.

When the  $\overline{\text{RESET}}$  pin is low and the internal reset is complete, the device goes to standby mode and cannot be accessed. Also, note that all the data output pins are tri-stated for the duration of the  $\overline{\text{RESET}}$  pulse. Once the  $\overline{\text{RESET}}$  pin is taken high, the device requires t<sub>RH</sub> of wake up time until outputs are valid for read access.

The  $\overline{\text{RESET}}$  pin may be tied to the system reset input. Therefore, if a system reset occurs during the Embedded Program or Erase Algorithm, the device will be automatically reset to read mode and this will enable the system's microprocessor to read the boot-up firmware from the Flash memory.

## Data Protection

The MBM29F002TC/BC is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completions of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from  $V_{CC}$  power-up and power-down transitions or system noise.

## Low $V_{CC}$ Write Inhibit

To avoid initiation of a write cycle during  $V_{CC}$  power-up and power-down, a write cycle is locked out for  $V_{CC}$  less than 3.2 V (typically 3.7 V). If  $V_{CC} < V_{LKO}$ , the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the  $V_{CC}$  level is greater than  $V_{LKO}$ . It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when  $V_{CC}$  is above 3.2 V.

## Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$ , or  $\overline{\text{WE}}$  will not initiate a write cycle.

## Logical Inhibit

Writing is inhibited by holding any one of  $\overline{\text{OE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IH}$  or  $\overline{\text{WE}} = V_{IH}$ . To initiate a write cycle  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be a logical zero while  $\overline{\text{OE}}$  is a logical one.

## Power-Up Write Inhibit

Power-up of the device with  $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$  and  $\overline{\text{OE}} = V_{IH}$  will not accept commands on the rising edge of  $\overline{\text{WE}}$ . The internal state machine is automatically reset to the read mode on power-up.

# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	T <sub>stg</sub>	−55	+125	°C
Ambient Temperature with Power Applied	T <sub>A</sub>	−40	+85	°C
Voltage with Respect to Ground All pins except A <sub>9</sub> , $\overline{\text{OE}}$ , and $\overline{\text{RESET}}$ *1, *2	V <sub>IN</sub> , V <sub>OUT</sub>	−2.0	+7.0	V
Power Supply Voltage *1, *3	V <sub>CC</sub>	−2.0	+7.0	V
A <sub>9</sub> , $\overline{\text{OE}}$ , and $\overline{\text{RESET}}$ *2	V <sub>IN</sub>	−2.0	+13.5	V

\*1 : Voltage is defined on the basis of V<sub>SS</sub> = GND = 0 V.

\*2 : Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, input or I/O pins may undershoot V<sub>SS</sub> to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V<sub>CC</sub> +0.5 V. During voltage transitions, input or I/O pins may overshoot to V<sub>CC</sub> +2.0 V for periods up to 20 ns.

\*3 : Minimum DC input voltage on A<sub>9</sub>,  $\overline{\text{OE}}$ , and  $\overline{\text{RESET}}$  pins is −0.5 V. During voltage transitions, A<sub>9</sub>,  $\overline{\text{OE}}$ , and  $\overline{\text{RESET}}$  pins may undershoot V<sub>SS</sub> to −2.0 V for periods of up to 20 ns. Voltage difference between input and power supply (V<sub>IN</sub> − V<sub>CC</sub>) does not exceed +9.0 V. Maximum DC input voltage on A<sub>9</sub>,  $\overline{\text{OE}}$ , and  $\overline{\text{RESET}}$  is +13.0 V which may overshoot to +14.0 V for periods up to 20 ns.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value		Unit
			Min	Max	
Ambient Temperature		T <sub>A</sub>	−40	+85	°C
V <sub>CC</sub> Supply Voltages*	MBM29F002TC/BC-55	V <sub>CC</sub>	+4.75	+5.25	V
	MBM29F002TC/BC-70/-90		+4.50	+5.50	V

\* : Voltage is defined on the basis of V<sub>SS</sub> = GND = 0 V.

Note : Operating ranges define those limits between which the functionality of the device is guaranteed.

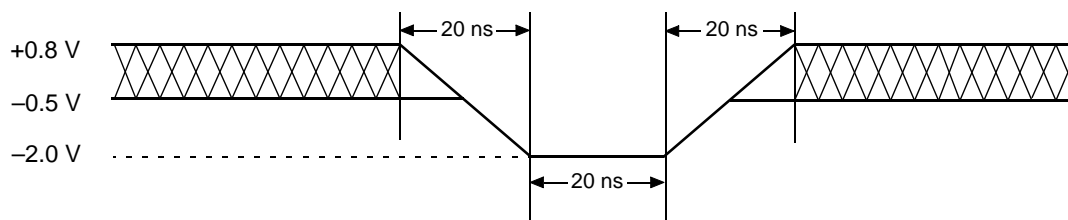
**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

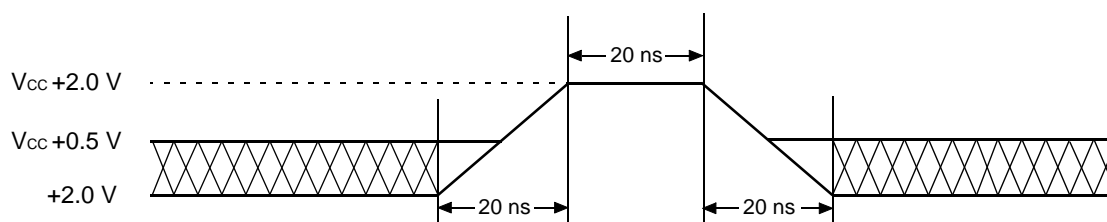
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT

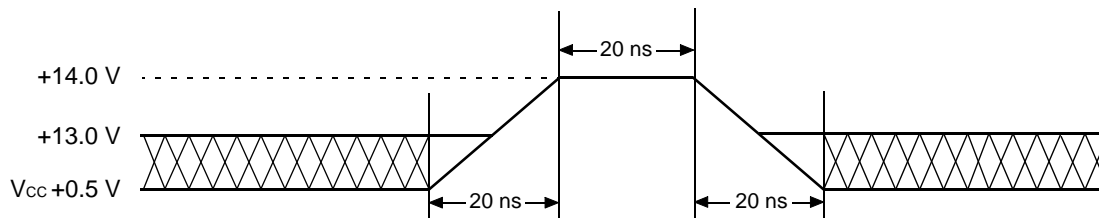
### 1. Maximum Overshoot Waveform



### 2. Maximum Overshoot Waveform 1



### 3. Maximum Overshoot Waveform 2



Note : This waveform is applied for  $A_9$ ,  $\overline{OE}$  and  $\overline{RESET}$ .

## ■ DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Value		Unit
			Min	Max	
Input Leakage Current	$I_{LI}$	$V_{IN} = V_{SS} \text{ to } V_{CC}, V_{CC} = V_{CC} \text{ Max}$	—	$\pm 1.0$	$\mu A$
Output Leakage Current	$I_{LO}$	$V_{OUT} = V_{SS} \text{ to } V_{CC}, V_{CC} = V_{CC} \text{ Max}$	—	$\pm 1.0$	$\mu A$
$A_9, \overline{OE}, \overline{RESET}$ Inputs Leakage Current	$I_{LIT}$	$V_{CC} = V_{CC} \text{ Max}, A_9, \overline{OE}, \overline{RESET} = 12.5 \text{ V}$	—	50	$\mu A$
$V_{CC}$ Active Current *1	$I_{CC1}$	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$	—	35	mA
$V_{CC}$ Active Current *2	$I_{CC2}$	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$	—	50	mA
$V_{CC}$ Current (Standby)	$I_{CC3}$	$V_{CC} = V_{CC} \text{ Max}, \overline{CE} = V_{IH}, \overline{RESET} = V_{IH}$	—	1	mA
		$V_{CC} = V_{CC} \text{ Max}, \overline{CE} = V_{CC} \pm 0.3 \text{ V}, \overline{RESET} = V_{CC} \pm 0.3 \text{ V}$	—	5	$\mu A$
$V_{CC}$ Current (Standby, Reset)	$I_{CC4}$	$V_{CC} = V_{CC} \text{ Max}, \overline{RESET} = V_{IL}$	—	1	mA
		$V_{CC} = V_{CC} \text{ Max}, \overline{RESET} = V_{SS} \pm 0.3 \text{ V}$	—	5	$\mu A$
Input Low Level	$V_{IL}$	—	-0.5	0.8	V
Input High Level	$V_{IH}$	—	2.0	$V_{CC} + 0.5$	V
Voltage for Autoselect and Sector Protection ( $A_9, \overline{OE}, \overline{RESET}$ ) *3, *4	$V_{ID}$	—	11.5	12.5	V
Output Low Voltage Level	$V_{OL}$	$I_{OL} = 12.0 \text{ mA}, V_{CC} = V_{CC} \text{ Min}$	—	0.45	V
Output High Voltage Level	$V_{OH1}$	$I_{OH} = -2.5 \text{ mA}, V_{CC} = V_{CC} \text{ Min}$	2.4	—	V
	$V_{OH2}$	$I_{OH} = -100 \mu A$	$V_{CC} - 0.4$	—	V
Low $V_{CC}$ Lock-Out Voltage	$V_{LKO}$	—	3.2	4.2	V

\*1 : The  $I_{CC}$  current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is 2 mA/MHz, with  $\overline{OE}$  at  $V_{IH}$ .

\*2 :  $I_{CC}$  active while Embedded Algorithm (program or erase) is in progress.

\*3 : Applicable to sector protection function.

\*4 : ( $V_{ID} - V_{CC}$ ) do not exceed 9 V.

## ■ AC CHARACTERISTICS

### • Read Only Operations Characteristics

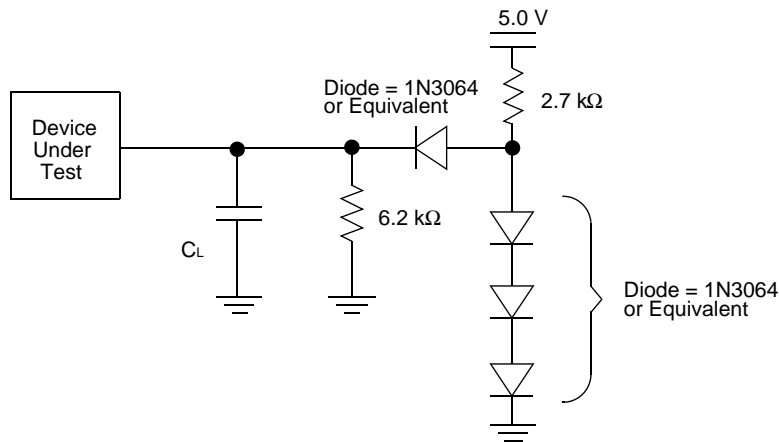
Parameter	Symbol		Test Setup	Value						Unit
				-55*1		-70*2		-90*2		
	JEDEC	Standard		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	—	55	—	70	—	90	—	ns
Address to Output Delay	t <sub>AVQV</sub>	t <sub>ACC</sub>	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	55	—	70	—	90	ns
Chip Enable to Output Delay	t <sub>ELQV</sub>	t <sub>CE</sub>	$\overline{OE} = V_{IL}$	—	55	—	70	—	90	ns
Output Enable to Output Delay	t <sub>GLQV</sub>	t <sub>OE</sub>	—	—	30	—	30	—	35	ns
Chip Enable to Output High-Z	t <sub>EHQZ</sub>	t <sub>DF</sub>	—	—	20	—	20	—	20	ns
Output Enable to Output High-Z	t <sub>GHQZ</sub>	t <sub>DF</sub>	—	—	20	—	20	—	20	ns
Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$ , Whichever Occurs First	t <sub>AXQX</sub>	t <sub>OH</sub>	—	0	—	0	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t <sub>READY</sub>	—	—	20	—	20	—	20	μs

\*1 : Test Conditions:

Output Load: 1 TTL gate and 30 pF  
 Input rise and fall times: 5 ns  
 Input pulse levels: 0.0 V or 3.0 V  
 Timing measurement reference level  
 Input: 1.5 V  
 Output: 1.5 V

\*2 : Test Conditions:

Output Load: 1 TTL gate and 100 pF  
 Input rise and fall times: 5 ns  
 Input pulse levels: 0.45 V or 2.4 V  
 Timing measurement reference level  
 Input: 0.8 V and 2.0 V  
 Output: 0.8 V and 2.0 V



Notes : •  $C_L = 30$  pF including jig capacitance  
 •  $C_L = 100$  pF including jig capacitance

**Figure 4 Test Conditions**



# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

## • Write/Erase/Program Operations

Parameter		Symbol		MBM29F002TC/BC									Unit
				-55			-70			-90			
		JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Write Cycle Time		t <sub>AVAV</sub>	t <sub>WC</sub>	55	—	—	70	—	—	90	—	—	ns
Address Setup Time		t <sub>AVWL</sub>	t <sub>AS</sub>	0	—	—	0	—	—	0	—	—	ns
Address Hold Time		t <sub>WLAX</sub>	t <sub>AH</sub>	40	—	—	45	—	—	45	—	—	ns
Data Setup Time		t <sub>DVWH</sub>	t <sub>DS</sub>	25	—	—	30	—	—	45	—	—	ns
Data Hold Time		t <sub>WHDx</sub>	t <sub>DH</sub>	0	—	—	0	—	—	0	—	—	ns
Output Enable Setup Time		—	t <sub>OES</sub>	0	—	—	0	—	—	0	—	—	ns
Output Enable Hold Time	Read	—	t <sub>OEh</sub>	0	—	—	0	—	—	0	—	—	ns
	Toggle Bit I and Data Polling			10	—	—	10	—	—	10	—	—	ns
Read Recover Time Before Write		t <sub>GHWL</sub>	t <sub>GHWL</sub>	0	—	—	0	—	—	0	—	—	ns
Read Recover Time Before Write		t <sub>GHEL</sub>	t <sub>GHEL</sub>	0	—	—	0	—	—	0	—	—	ns
$\overline{\text{CE}}$ Setup Time		t <sub>ELWL</sub>	t <sub>CS</sub>	0	—	—	0	—	—	0	—	—	ns
$\overline{\text{WE}}$ Setup Time		t <sub>WLLEL</sub>	t <sub>WS</sub>	0	—	—	0	—	—	0	—	—	ns
$\overline{\text{CE}}$ Hold Time		t <sub>WHEH</sub>	t <sub>CH</sub>	0	—	—	0	—	—	0	—	—	ns
$\overline{\text{WE}}$ Hold Time		t <sub>EHWH</sub>	t <sub>WH</sub>	0	—	—	0	—	—	0	—	—	ns
Write Pulse Width		t <sub>WLWH</sub>	t <sub>WP</sub>	30	—	—	35	—	—	45	—	—	ns
Write Pulse Width		t <sub>ELEH</sub>	t <sub>CP</sub>	30	—	—	35	—	—	45	—	—	ns
Write Pulse Width High		t <sub>WHWL</sub>	t <sub>WPH</sub>	20	—	—	20	—	—	20	—	—	ns
Write Pulse Width High		t <sub>EHEL</sub>	t <sub>CPH</sub>	20	—	—	20	—	—	20	—	—	ns
Byte Programming Operation		t <sub>WHWH1</sub>	t <sub>WHWH1</sub>	—	8	—	—	8	—	—	8	—	μs
Sector Erase Operation *1		t <sub>WHWH2</sub>	t <sub>WHWH2</sub>	—	1	—	—	1	—	—	1	—	s
				—	—	8	—	—	8	—	—	8	s
V <sub>CC</sub> Setup Time		—	t <sub>VCS</sub>	50	—	—	50	—	—	50	—	—	μs
Rise Time to V <sub>ID</sub>		—	t <sub>VIDR</sub>	500	—	—	500	—	—	500	—	—	ns
Voltage Transition Time *2		—	t <sub>VLHT</sub>	4	—	—	4	—	—	4	—	—	μs
Write Pulse Width *2		—	t <sub>WPP</sub>	100	—	—	100	—	—	100	—	—	μs
$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active *2		—	t <sub>OESP</sub>	4	—	—	4	—	—	4	—	—	μs
$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active *2		—	t <sub>CSP</sub>	4	—	—	4	—	—	4	—	—	μs

(Continued)

# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

(Continued)

Continued

Parameter	Symbol		MBM29F002TC/BC									Unit
			-55			-70			-90			
	JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESET Pulse Width	—	t <sub>RP</sub>	500	—	—	500	—	—	500	—	—	ns
RESET Hold Time Before Read	—	t <sub>RH</sub>	50	—	—	50	—	—	50	—	—	ns
Delay Time from Embedded Output Enable	—	t <sub>EOE</sub>	—	—	30	—	—	30	—	—	35	ns

\*1 : This does not include the preprogramming time.

\*2 : This timing is for Sector Protection operation.

## ■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	1	8	s	Excludes 00h programming prior to erasure
Byte Programming Time	—	8	150	μs	Excludes system-level overhead
Chip Programming Time	—	2.1	5	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	

## ■ TSOP(1) PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0	7	8	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0	8	10	pF
Control Pin Capacitance	C <sub>IN2</sub>	V <sub>IN</sub> = 0	8	10	pF

Note : Test conditions T<sub>A</sub> = +25°C, f = 1.0 MHz

## ■ PLCC PIN CAPACITANCE




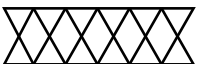

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0	7	8	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0	8	10	pF
Control Pin Capacitance	C <sub>IN2</sub>	V <sub>IN</sub> = 0	8	10	pF

Notes : • Sampled, not 100% tested.

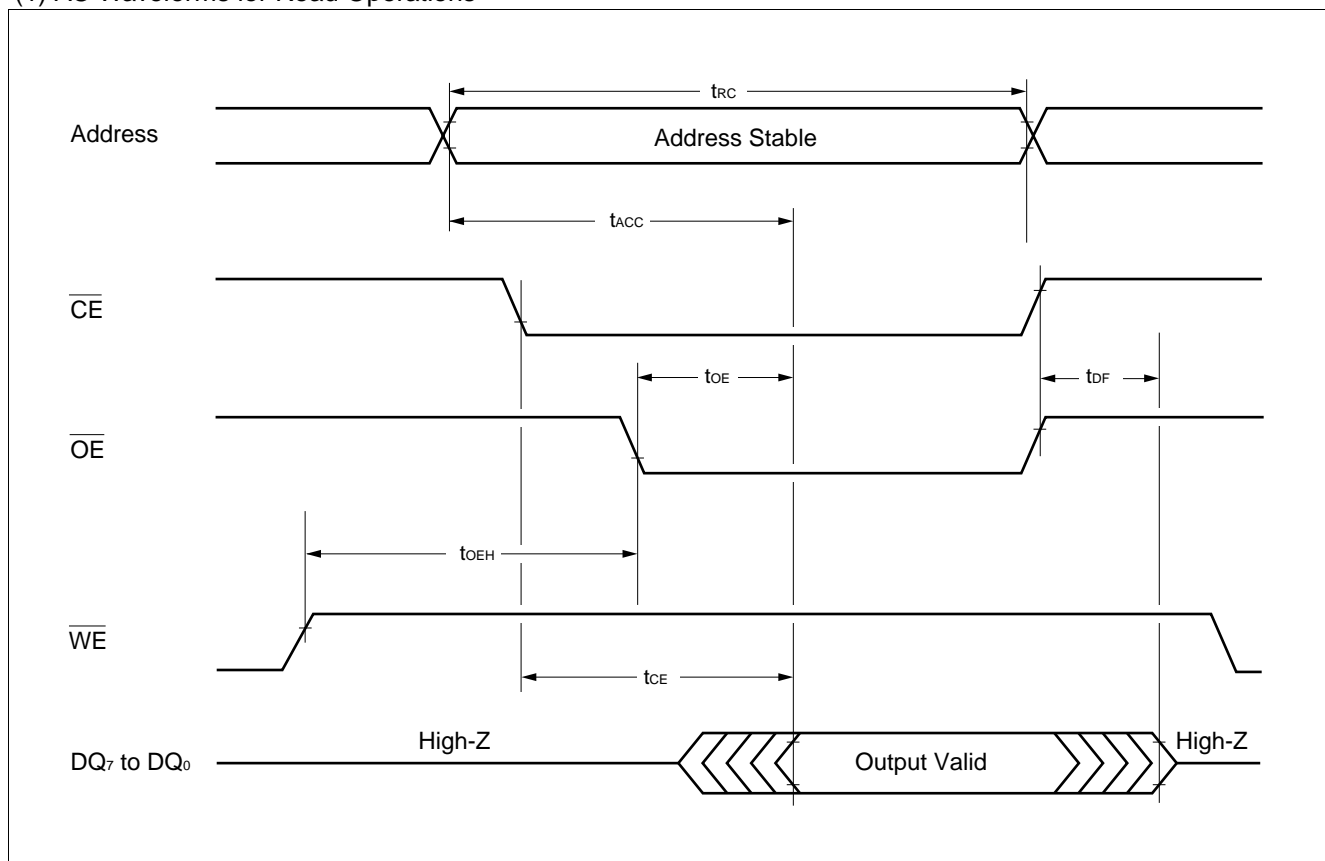
• Test conditions T<sub>A</sub> = +25°C, f = 1.0 MHz

## ■ SWITCHING WAVEFORMS

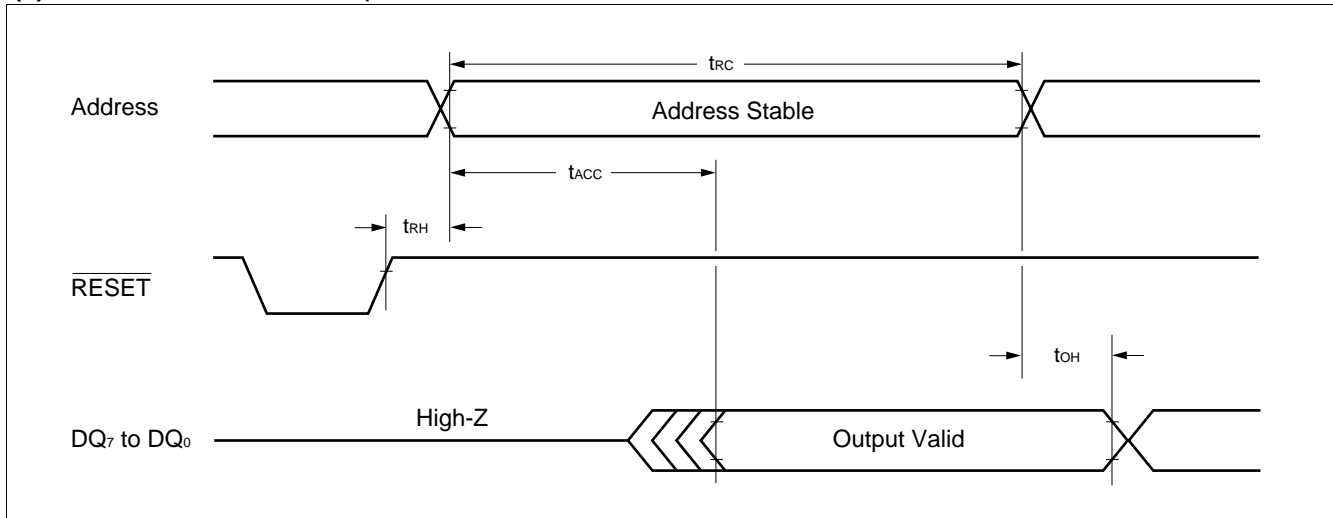
### • Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	"H" or "L" Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

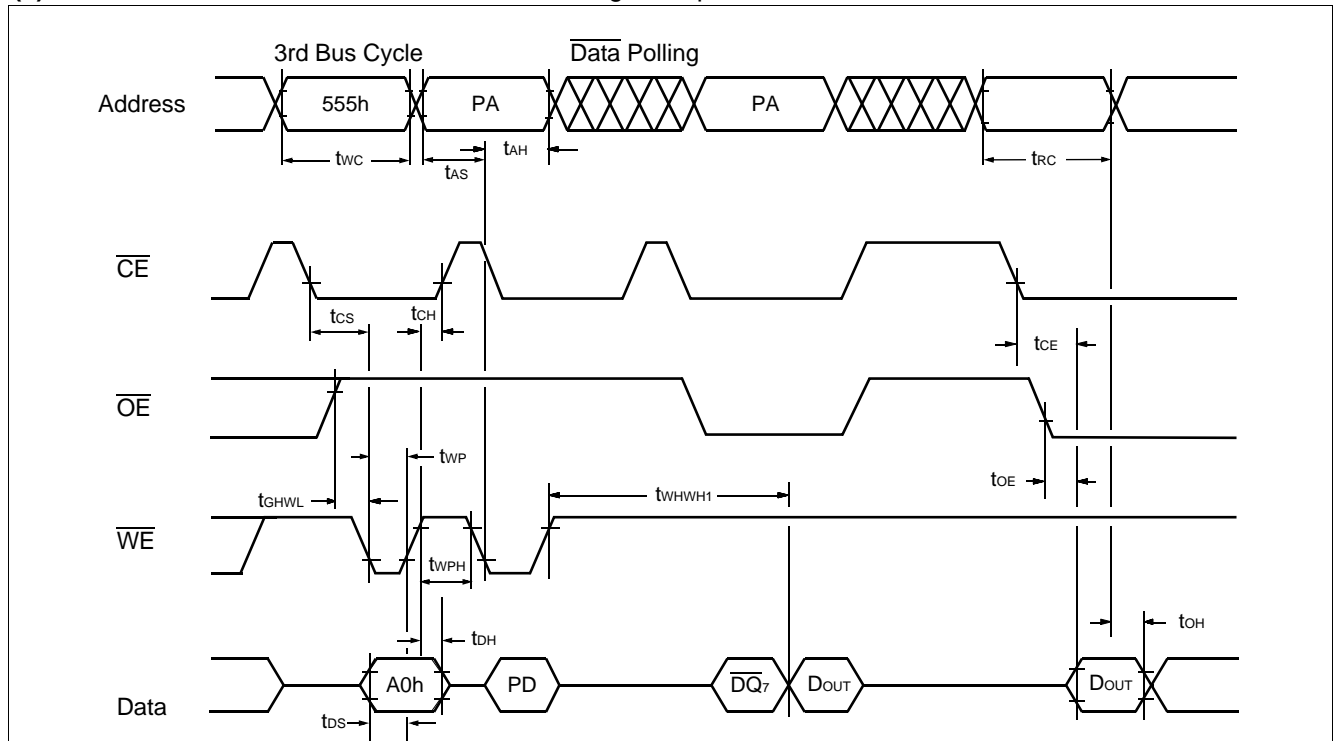
### (1) AC Waveforms for Read Operations



## (2) AC Waveforms for Read Operations

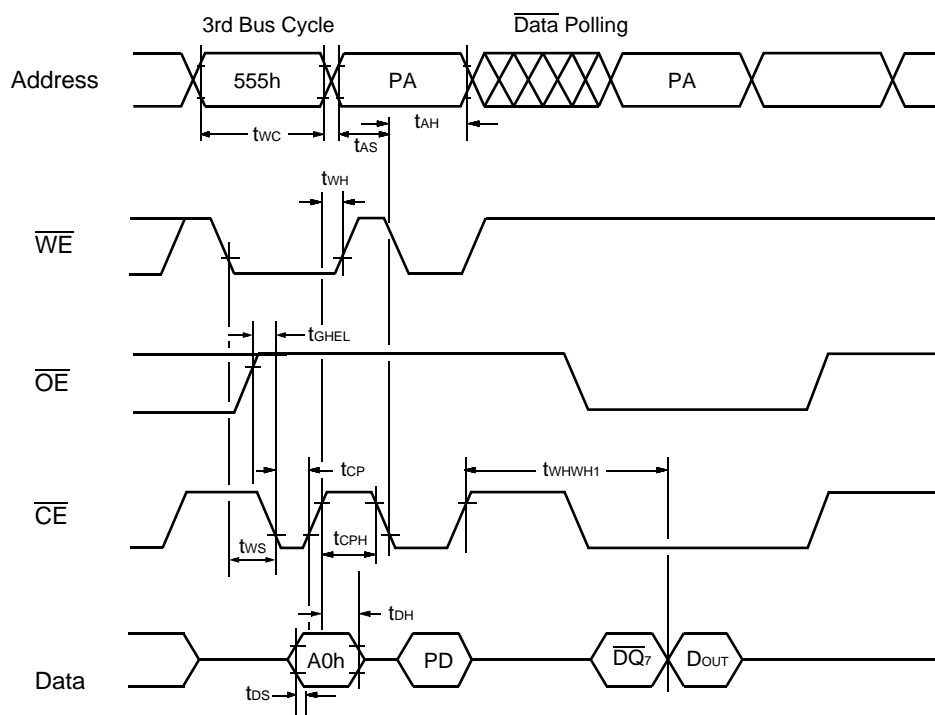


## (3) AC Waveforms for Alternate $\overline{WE}$ Controlled Program Operations



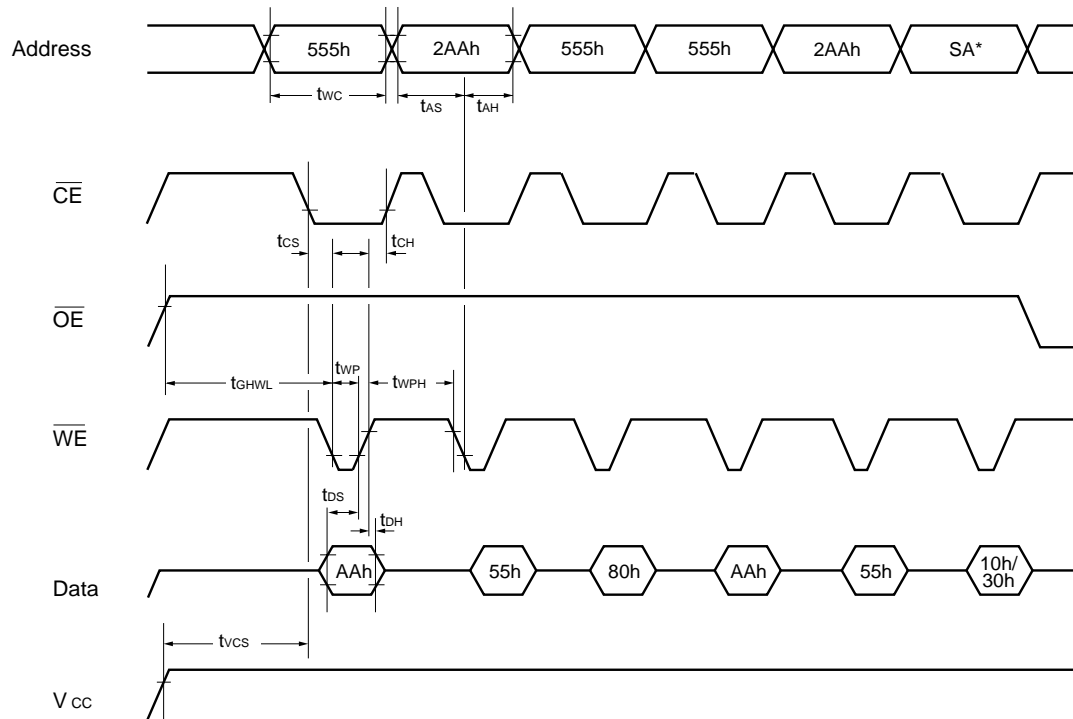
- Notes :
- PA is address of the memory location to be programmed.
  - PD is data to be programmed at byte address.
  - $\overline{DQ_7}$  is the output of the complement of the data written to the device.
  - D<sub>OUT</sub> is the output of the data written to the device.
  - Figure indicates last two bus cycles of four bus cycle sequence.

## (4) AC Waveforms for Alternate $\overline{\text{CE}}$ Controlled Program Operations



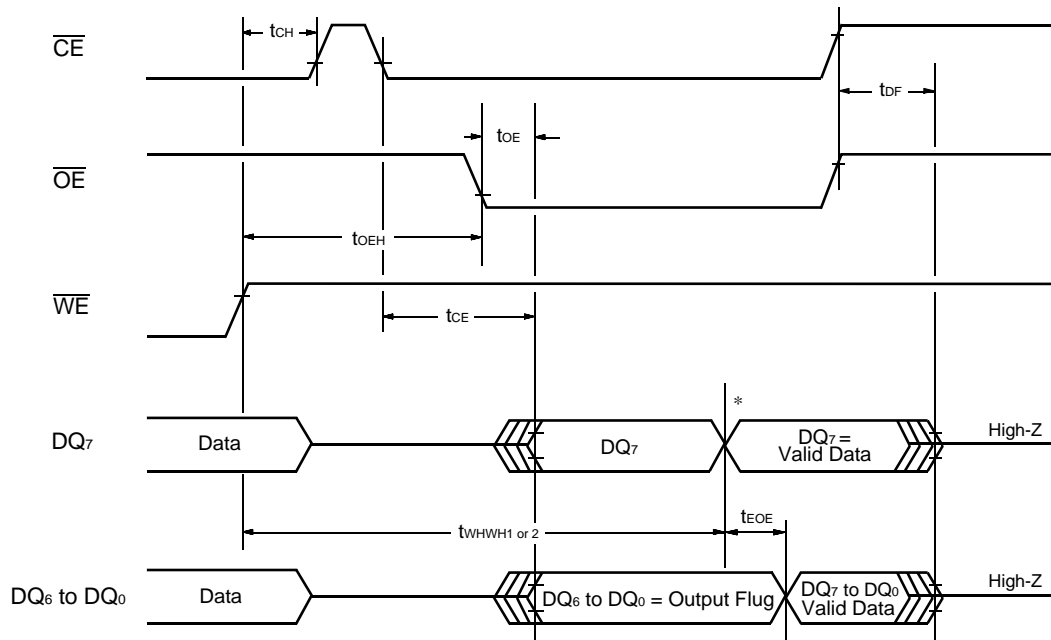
- Notes :
- PA is address of the memory location to be programmed.
  - PD is data to be programmed at byte address.
  - $\overline{\text{DQ}}_7$  is the output of the complement of the data written to the device.
  - D<sub>OUT</sub> is the output of the data written to the device.
  - Figure indicates last two bus cycles of four bus cycle sequence.

## (5) AC Waveforms Chip/Sector Erase Operations



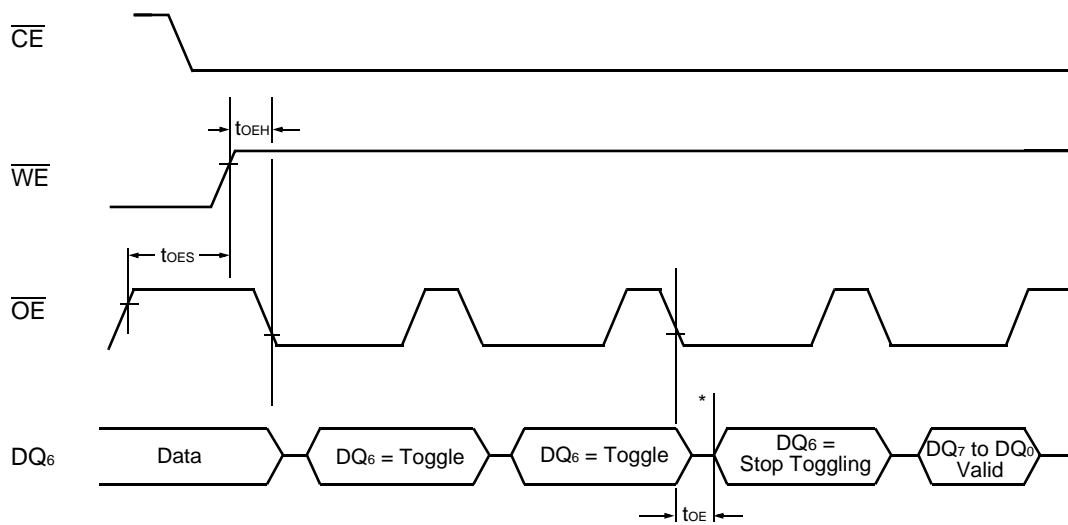
\*: SA is the sector address for Sector Erase. Addresses = 555h for Chip Erase.

## (6) AC Waveforms for Data Polling During Embedded Algorithm Operations

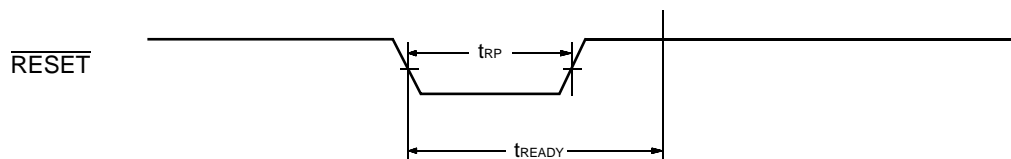


\*: DQ7 = Valid Data (The device has completed the Embedded operation.)

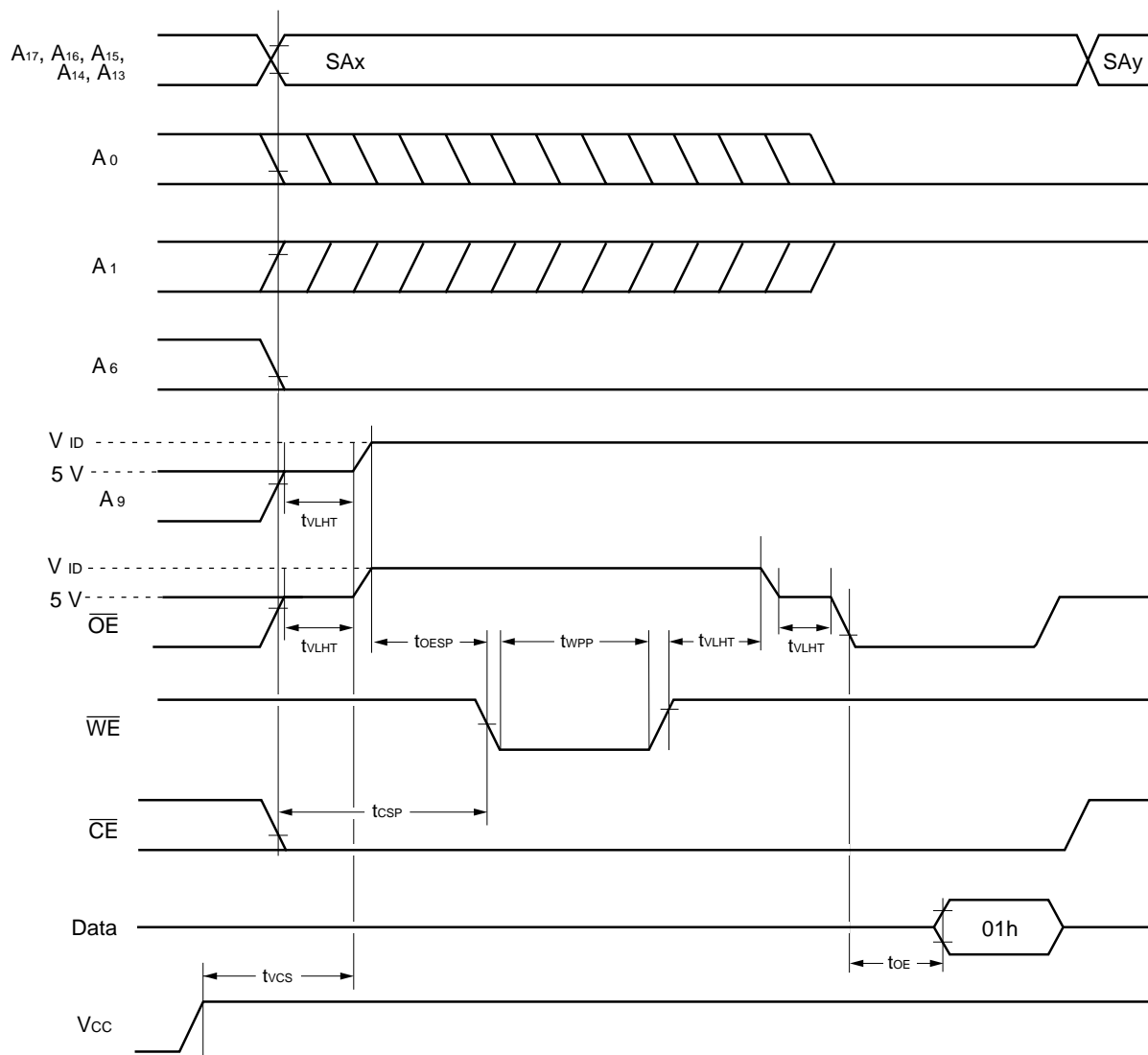
(7) AC Waveforms for Toggle Bit I during Embedded Algorithm Operations



(8)  $\overline{RESET}$  Timing Diagram



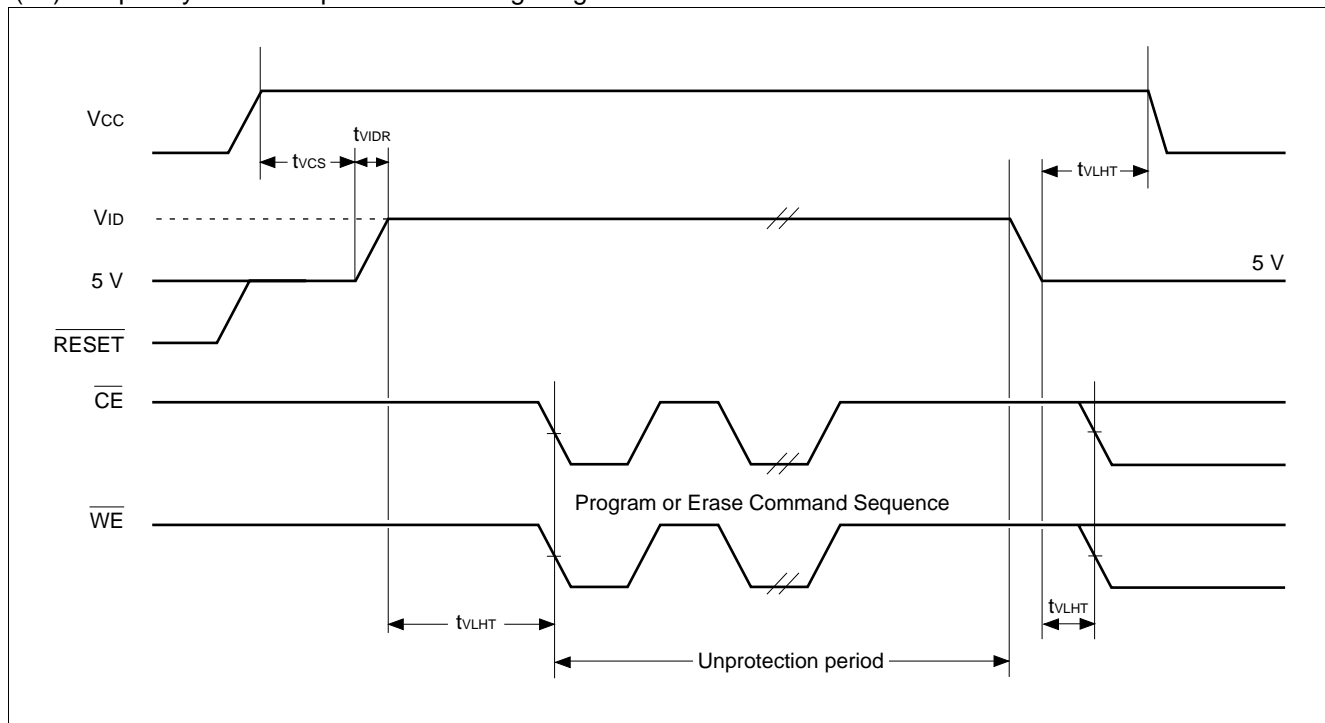
(9) AC Waveforms for Sector Protection Timing Diagram



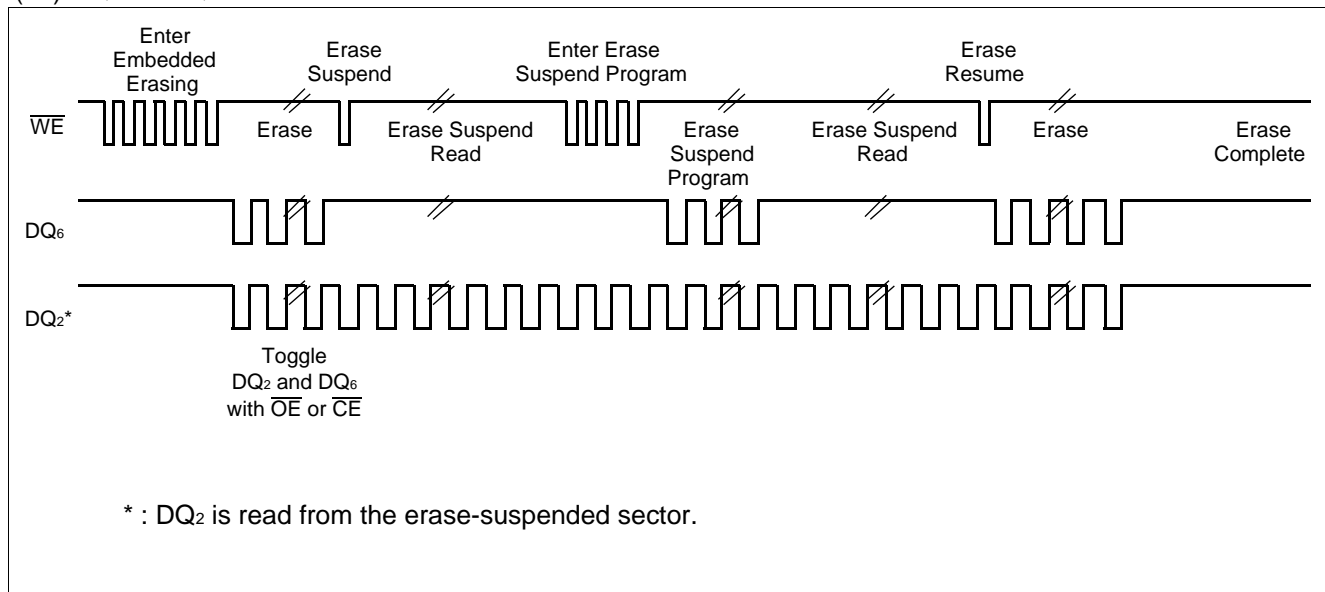
SGAx = Sector Address for initial sector  
 SGAy = Sector Address for initial sector



(10) Temporary Sector Unprotection Timing Diagram



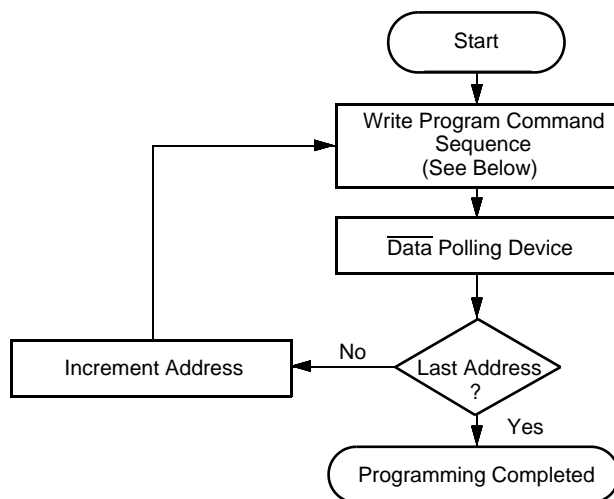
(11) DQ<sub>2</sub> vs. DQ<sub>6</sub>



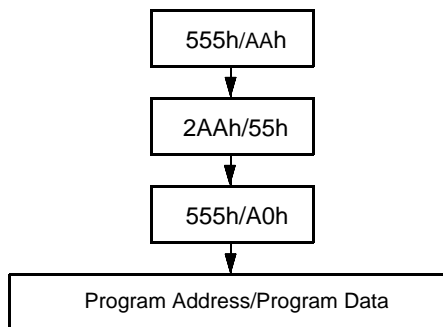
## ■ FLOW CHART

### (1) Embedded Program™ Algorithm

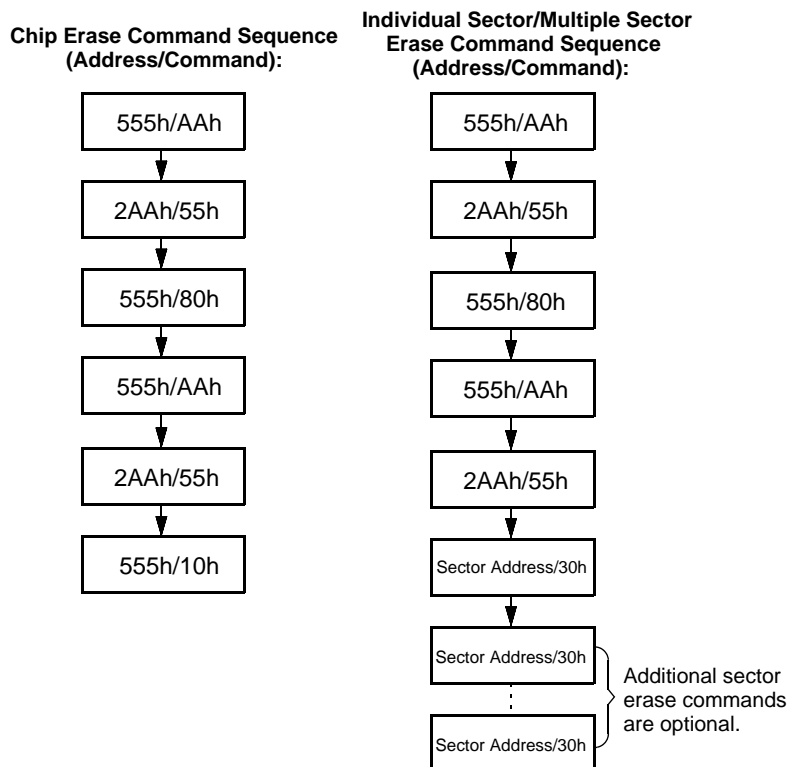
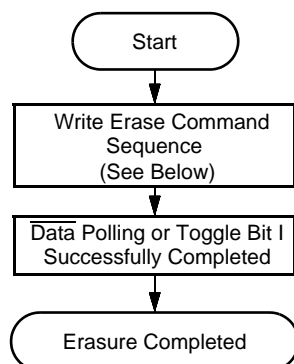
#### EMBEDDED ALGORITHMS



#### Program Command Sequence (Address/Command):

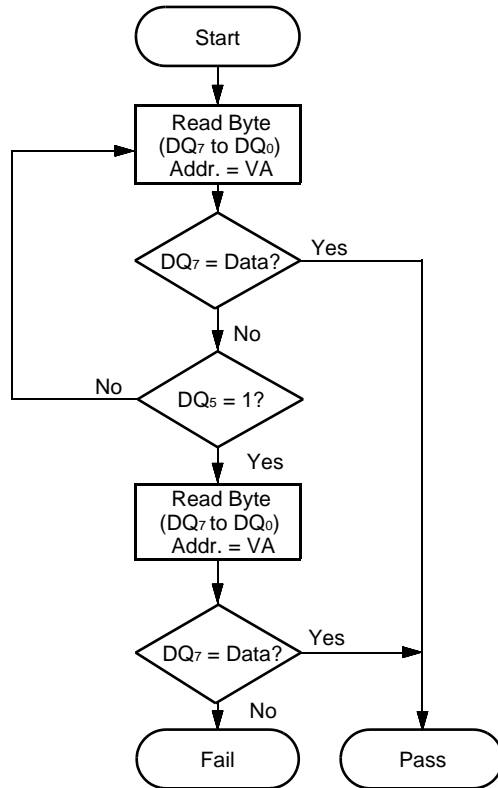


## (2) Embedded Erase™ Algorithm



Note : To insure the command has been accepted, the system software should check the status of DQ<sub>3</sub> prior to and following each subsequent sector erase command. If DQ<sub>3</sub> were high on the second status check, the command may not have been accepted.

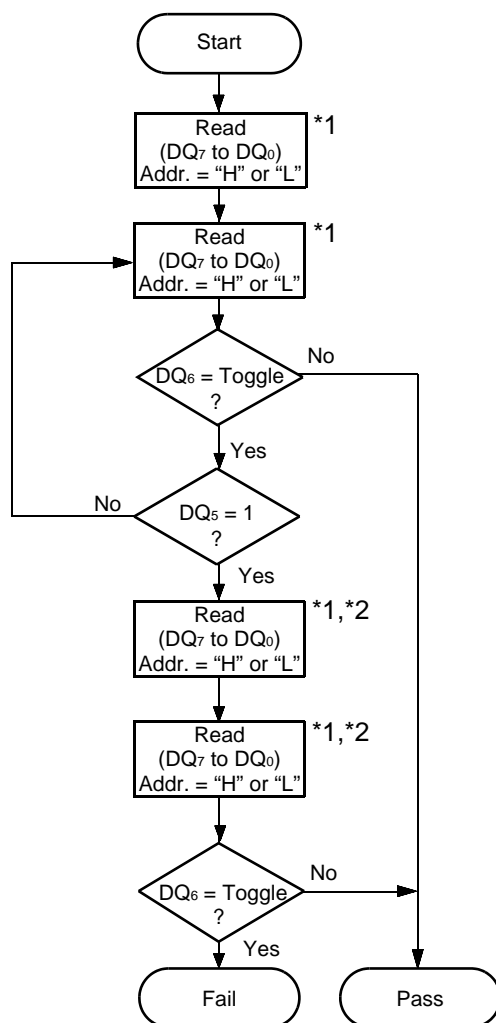
## (3) Data Polling Algorithm



VA = Address for programming  
 = Any of the sector addresses within the sector being erased during sector erase or multiple erases operation.  
 = Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.

Note : DQ<sub>7</sub> is rechecked even if DQ<sub>5</sub> = "1" because DQ<sub>7</sub> may change simultaneously with DQ<sub>5</sub>.

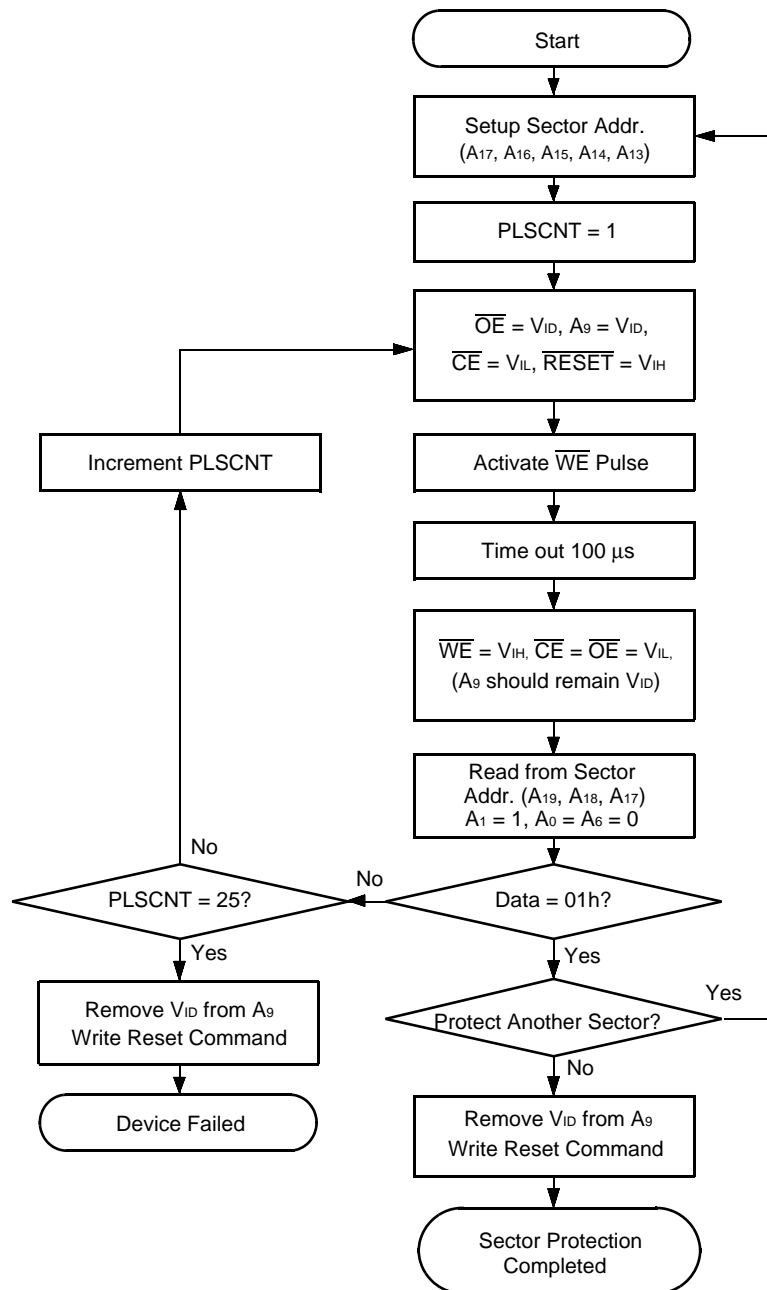
## (4) Toggle Bit I Algorithm



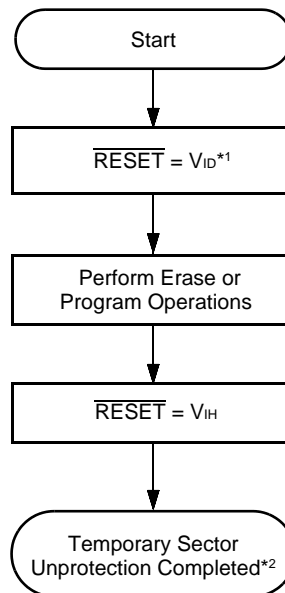
\*1 : Read toggle bit twice to determin whether it is toggling.

\*2 : DQ<sub>6</sub> is rechecked even if DQ<sub>5</sub> = "1" because DQ<sub>6</sub> may stop toggling at the same time as DQ<sub>5</sub> changing to "1".

(5) Sector Protection Algorithm



## (6) Temporary Sector Unprotection Algorithm



\*1 : All Protected sectors unprotected.

\*2 : All previously protected sectors are protected once again.

# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

## ■ ORDERING INFORMATION

Part No.	Package	Access Time (ns)	Remarks
MBM29F002TC-55PFTN	32-pin plastic TSOP (1) (FPT-32P-M24) (Normal Bend)	55	Top Sector
MBM29F002TC-70PFTN		70	
MBM29F002TC-90PFTN		90	
MBM29F002TC-55PFTR	32-pin plastic TSOP (1) (FPT-32P-M25) (Reverse Bend)	55	
MBM29F002TC-70PFTR		70	
MBM29F002TC-90PFTR		90	
MBM29F002TC-55PD	32-pin plastic QFJ (PLCC) (LCC-32P-M02)	55	Bottom Sector
MBM29F002TC-70PD		70	
MBM29F002TC-90PD		90	
MBM29F002BC-55PFTN	32-pin plastic TSOP (1) (FPT-32P-M24) (Normal Bend)	55	
MBM29F002BC-70PFTN		70	
MBM29F002BC-90PFTN		90	
MBM29F002BC-55PFTR	32-pin plastic TSOP (1) (FPT-32P-M25) (Reverse Bend)	55	
MBM29F002BC-70PFTR		70	
MBM29F002BC-90PFTR		90	
MBM29F002BC-55PD	32-pin plastic QFJ (PLCC) (LCC-32P-M02)	55	
MBM29F002BC-70PD		70	
MBM29F002BC-90PD		90	

MBM29F002    T    C    -70    PFTN

### PACKAGE TYPE

PFTN = 32-Pin Thin Small Outline Package  
(TSOP (1) ) Normal Bend  
PFTR = 32-Pin Thin Small Outline Package  
(TSOP (1) ) Reverse Bend  
PD = 32-Pin Rectangular Plastic Leaded  
Chip Carrier (QFJ (PLCC) )

### SPEED OPTION

See Product Selector Guide

C = Device Revision

### BOOT CODE SECTOR ARCHITECTURE

T = Top sector  
B = Bottom sector

### DEVICE NUMBER/DESCRIPTION

MBM29F002

2 Mega-bit (256K × 8-Bit) CMOS Flash Memory  
5.0 V-only Read, Write, and Erase

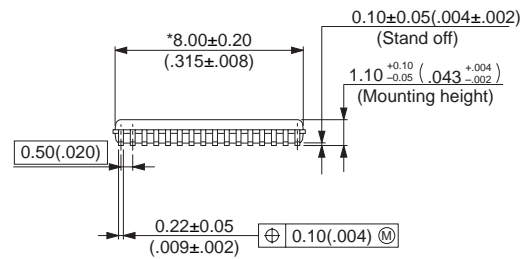
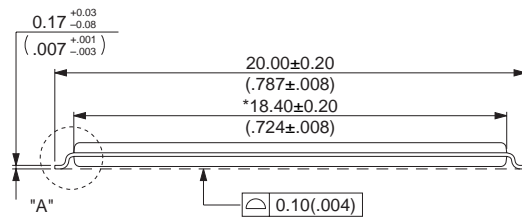
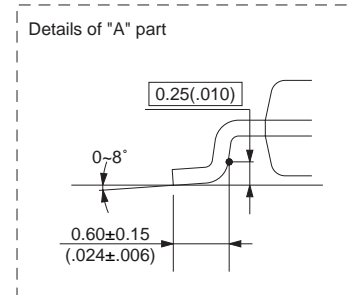
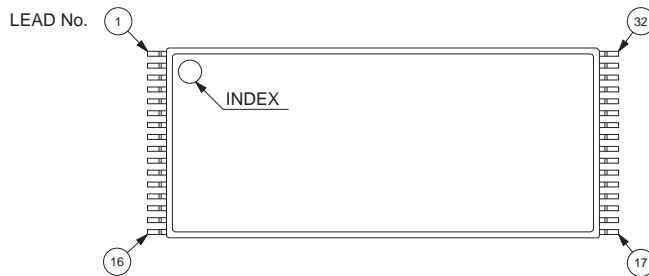


# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

## ■ PACKAGE DIMENSIONS

32-pin plastic TSOP(1)  
(FPT-32P-M24)

Note 1) \* : Resin protrusion. (Each side : +0.15 (.006) Max)  
Note 2) Pins width and pins thickness include plating thickness.  
Note 3) Pins width do not include tie bar cutting remainder.



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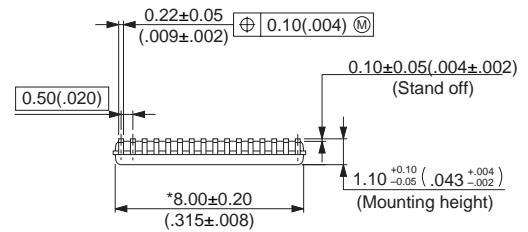
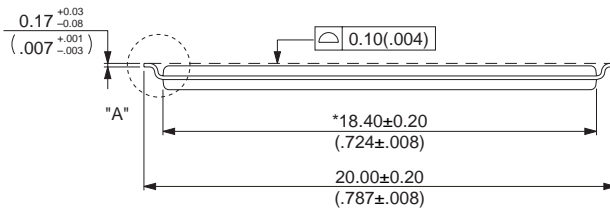
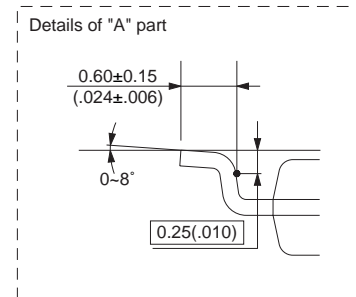
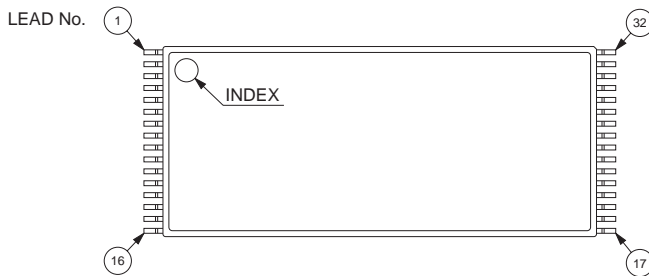
Dimensions in mm (inches) .  
Note : The values in parentheses are reference values.

(Continued)

# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

32-pin plastic TSOP(1)  
(FPT-32P-M25)

Note 1) \* : Resin protrusion. (Each side : +0.15 (.006) Max)  
Note 2) Pins width and pins thickness include plating thickness.  
Note 3) Pins width do not include tie bar cutting remainder.



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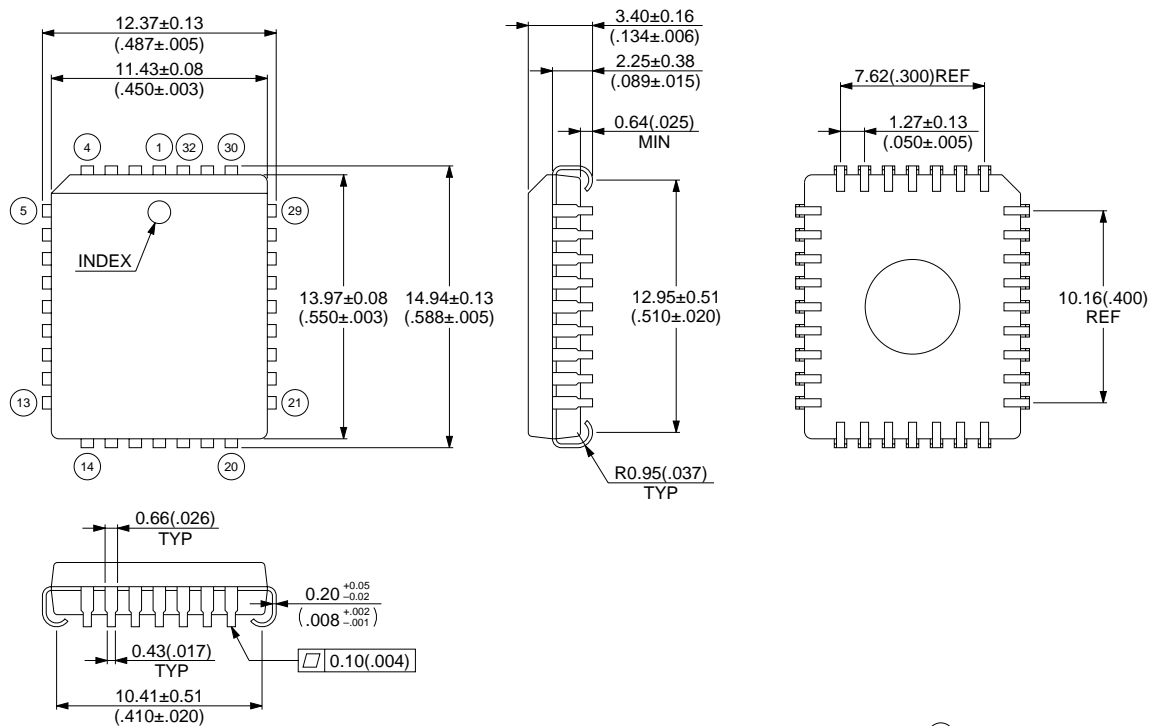
Dimensions in mm (inches) .  
Note : The values in parentheses are reference values.

(Continued)

# MBM29F002TC-55/-70/-90/MBM29F002BC-55/-70/-90

(Continued)

32-pin plastic QFJ(PLCC)  
(LCC-32P-M02)



(No) : LEAD No.

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Dimensions in mm (inches) .

Note : The values in parentheses are reference values.

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