SIEMENS

ICs for Communications

Multichannel Network Interface Controller for HDLC MUNICH32

PEB 20320 Version 3.4
PEF 20320 Version 3.4

Delta Sheet 12.97

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Multichannel Network Interface Controller for HDLC
MUNICH32

PEB 20320
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Delta Sheet for the Version 3.4

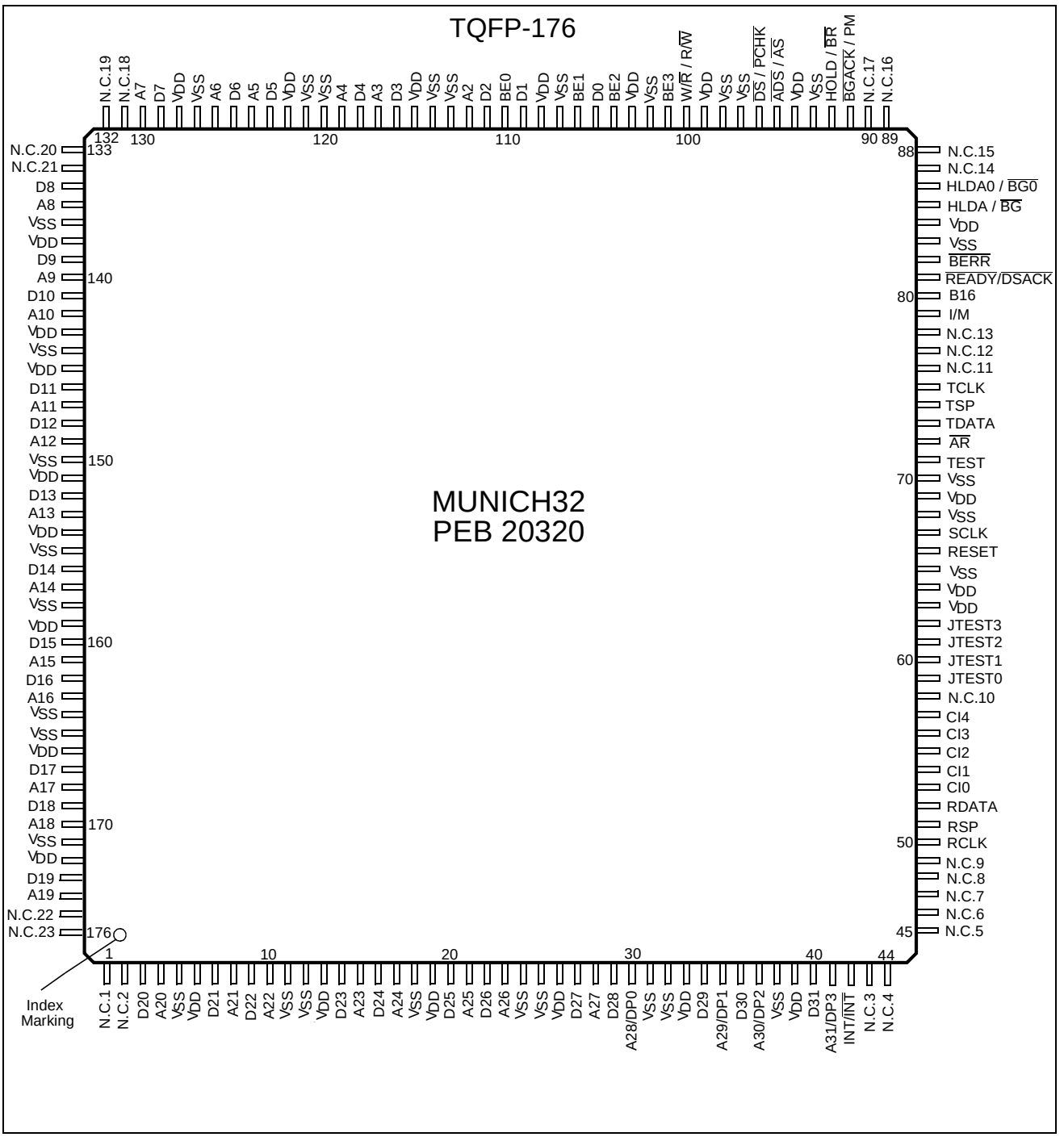
This document describes the latest MUNICH32 (Version 3.4) in relation to the Version 3.2 and hence is a “Delta Sheet“ which references the MUNICH32 User’s Manual 01.96 (V 3.2).

1 Upgrades of MUNICH32 V3.4

1.1 Package

MUNICH32 V3.4 is provided in both packages: P-MQFP-160-1 and P-TQFP-176.

1.2 Pin Configuration (top view)



1.3 Functional Upgrades

1.3.1 Capability of minimum one byte reception in HDLC CS=1 mode

The MUNICH32 V3.4 is able to receive frames with 1 Byte length. This capability is available in HDLC CS=1 mode only. In order to use this new functionality bit #9 of the channel specification, which is called NSF (=no short frame indication), has to be set to a logical ’1’.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Interrupt Mask								NITBS	RI	TI	TO	TA	TH	RO	RA
FRDA															
FTDA															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFLAG						TFLAG/ NSF	TFLAG/ CS	INV	CRC	TRV		FA	Mode		IFTF
FRDA															
FTDA															
0	0	0	0	0	0	0	0	0	0	ITBS					

When this bit is set to ’1’ with CS=0 aborted frames (> 2 byte) are written into the shared memory, last 2 bytes are invalid, ERR / CRC interrupt is generated, status RA bit is set.

In all other modes (HDLC protocol) this bit has to be set to logical ’0’!

The new mode has all features of the HDLC mode with the following changes:

- In case of 1 Byte (or greater) frame received, the data is copied to the RAM
- The short frame interrupt is not generated!
- The short frame status bit is not set the same way as described in HDLC case
- The FI interrupt is generated the same way as described in HDLC case

Note: CRC is still calculated and checked and e.g. a frame of 1 or 2 Byte length (in CRC16 Mode) will always cause an FI+ERR interrupt.

Examples:

a)	0x7E, data1, 0x7E...	• data1 in RAM • status SF-Bit set • FI indication interrupt generated • No SF interrupt • ERR interrupt due to wrong CRC
b)	0x7E, data=0xFC(or 0xFD, or 0x7F), 0x7E	• no data in RAM • SF, ERR-interrupt

1.3.2 Reset

The RESET behaviour was changed between MUNICH32 V3.3 and MUNICH32 V3.4:

After power up a logical ’1’ at the reset pin of the MUNICH32 V3.4 sets the device into a reset state where the complete microprocessor bus interface is tristated and the internal reset sequence is started.

The trailing edge of the reset starts the last part of the internal reset sequence and takes about 12 SCLK clock cycles. It is not allowed to give an AR during these first 12 SCLK cycles after the trailing edge of RESET.

1.3.3 New version number

The version number is identified in the interrupt information bits VN(3:1):

these bits are ’110’ for version 3.4.

The version number in the boundary scan ID code is set to ’0110’ for version 3.4.

1.4 Electrical Characteristics

The MUNICH32 V3.4 is available for the extended range of temperature:

Ambient temperature ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: PEB	T_A	0 to 70	°C
PEF	T_A	-40 to 85	°C

All other electrical characteristics are as specified in MUNICH32 User’s Manual 01.96.