

SN54F258, SN74F258
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

SDFS067A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- 3-State Outputs Interface Directly With System Bus
- Provides Bus Interface From Multiple Sources in High-Performance Systems
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

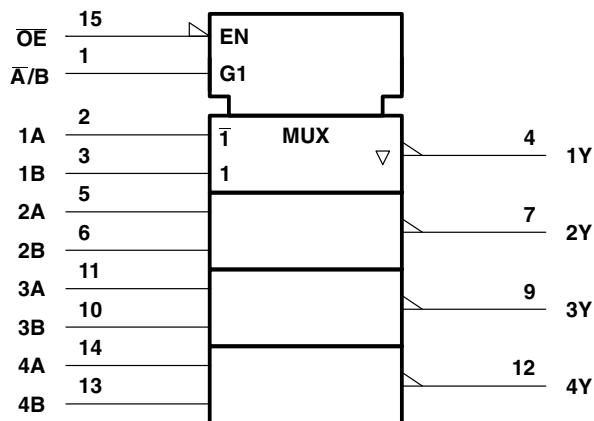
The 'F258 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output-enable (\overline{OE}) input is at a high logic level.

The SN54F258 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74F258 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

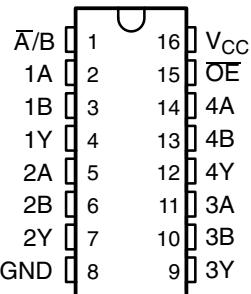
INPUTS				OUTPUT
\overline{OE}	$\overline{A/B}$	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

logic symbol†

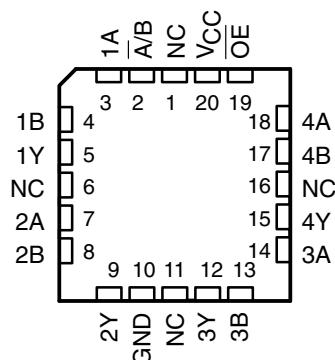


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

SN54F258 . . . J PACKAGE
SN74F258 . . . D OR N PACKAGE
(TOP VIEW)



SN54F258 . . . FK PACKAGE
(TOP VIEW)



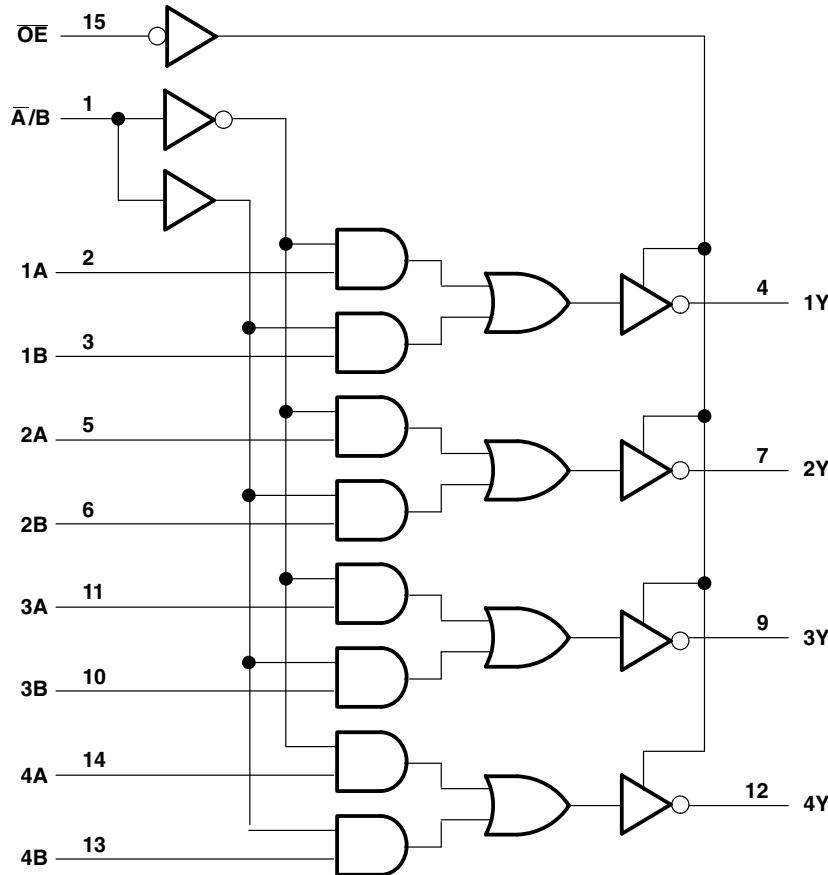
NC – No internal connection

SN54F258, SN74F258

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

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QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES
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recommended operating conditions

		SN54F258			SN74F258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2		2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	High-level output current			-3			-3	mA
I _{OL}	Low-level output current			20			24	mA
T _A	Operating free-air temperature	-55	125		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54F258			SN74F258			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = 4.5 V	I _{OH} = -1 mA	2.5	3.4	2.5	3.4		V
		I _{OH} = -3 mA	2.4	3.3	2.4	3.3		
	V _{CC} = 4.75 V,	I _{OH} = -1 mA to -3 mA			2.7			
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 20 mA	0.3	0.5				V
		I _{OL} = 24 mA			0.35	0.5		
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			50			50	μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			-50			-50	μA
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.5 V			-0.6			-0.6	mA
I _{OS[‡]}	V _{CC} = 5.5 V, V _O = 0	-60	-150		-60	-150		mA
I _{CCH}	V _{CC} = 5.5 V, See Note 2	Condition A	6.2	9.5	6.2	9.5		mA
I _{CCL}		Condition B	15.1	23	15.1	23		
I _{CCZ}		Condition C	11.3	17	11.3	17		

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:

- A. All B inputs at 4.5 V, other inputs grounded
- B. \bar{A}/B and all B inputs at 4.5 V, other inputs grounded
- C. \bar{OE} and all B inputs at 4.5 V, other inputs grounded

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switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $R1 = 500\text{ }\Omega$, $R2 = 500\text{ }\Omega$, $T_A = 25^\circ\text{C}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R1 = 500\text{ }\Omega$, $R2 = 500\text{ }\Omega$, $T_A = \text{MIN to MAX}^\dagger$			UNIT	
			'F258			SN54F258		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	Data (A or B)	Any Y	1	3.6	5.3	1	7.5	1 6
t_{PHL}			1	3.1	4.7	1	6	1 5.5
t_{PLH}	A/B	Any Y	3.2	6.1	8.5	3.2	12	3.2 9.5
t_{PHL}			3.2	6.9	9.5	3.2	11.5	3.2 11
t_{PZH}	G	Any Y	2.2	5.5	7.5	2.2	11	2.2 8.5
t_{PZL}			2.2	5.1	7.5	2.2	9.5	2.2 8.5
t_{PHZ}	G	Any Y	1.2	3.9	6	1	7	1.2 7
t_{PLZ}			1.2	4.1	6	1.2	9	1.2 7

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74F258D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F258
SN74F258D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F258
SN74F258DG4	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F258
SN74F258N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F258N
SN74F258N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F258N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

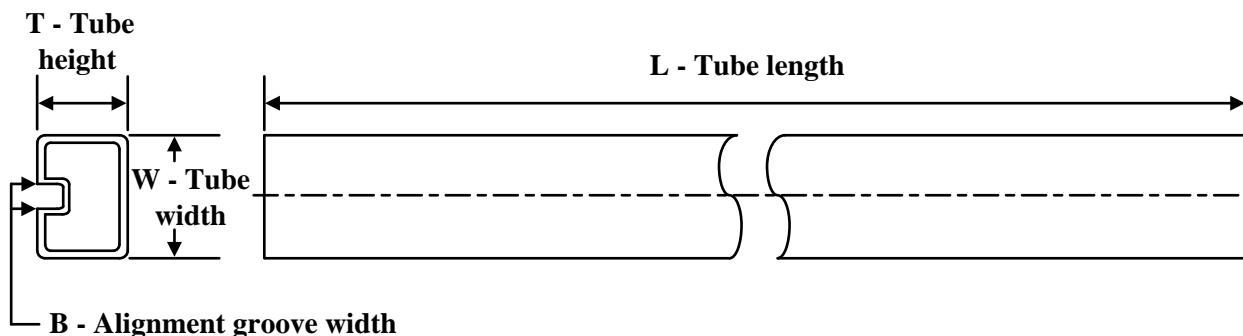
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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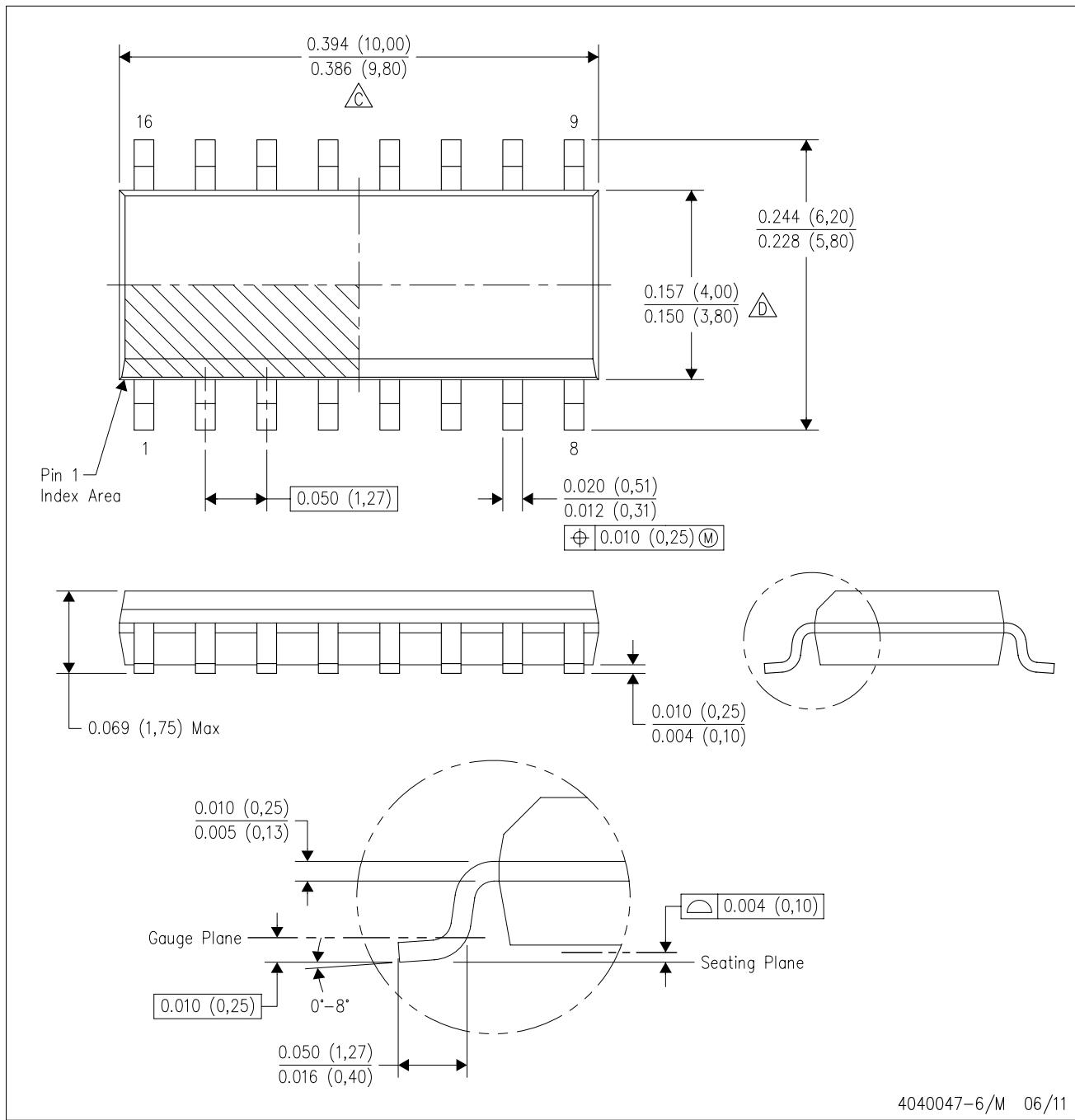
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74F258D	D	SOIC	16	40	507	8	3940	4.32
SN74F258D.A	D	SOIC	16	40	507	8	3940	4.32
SN74F258DG4	D	SOIC	16	40	507	8	3940	4.32
SN74F258N	N	PDIP	16	25	506	13.97	11230	4.32
SN74F258N	N	PDIP	16	25	506	13.97	11230	4.32
SN74F258N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74F258N.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

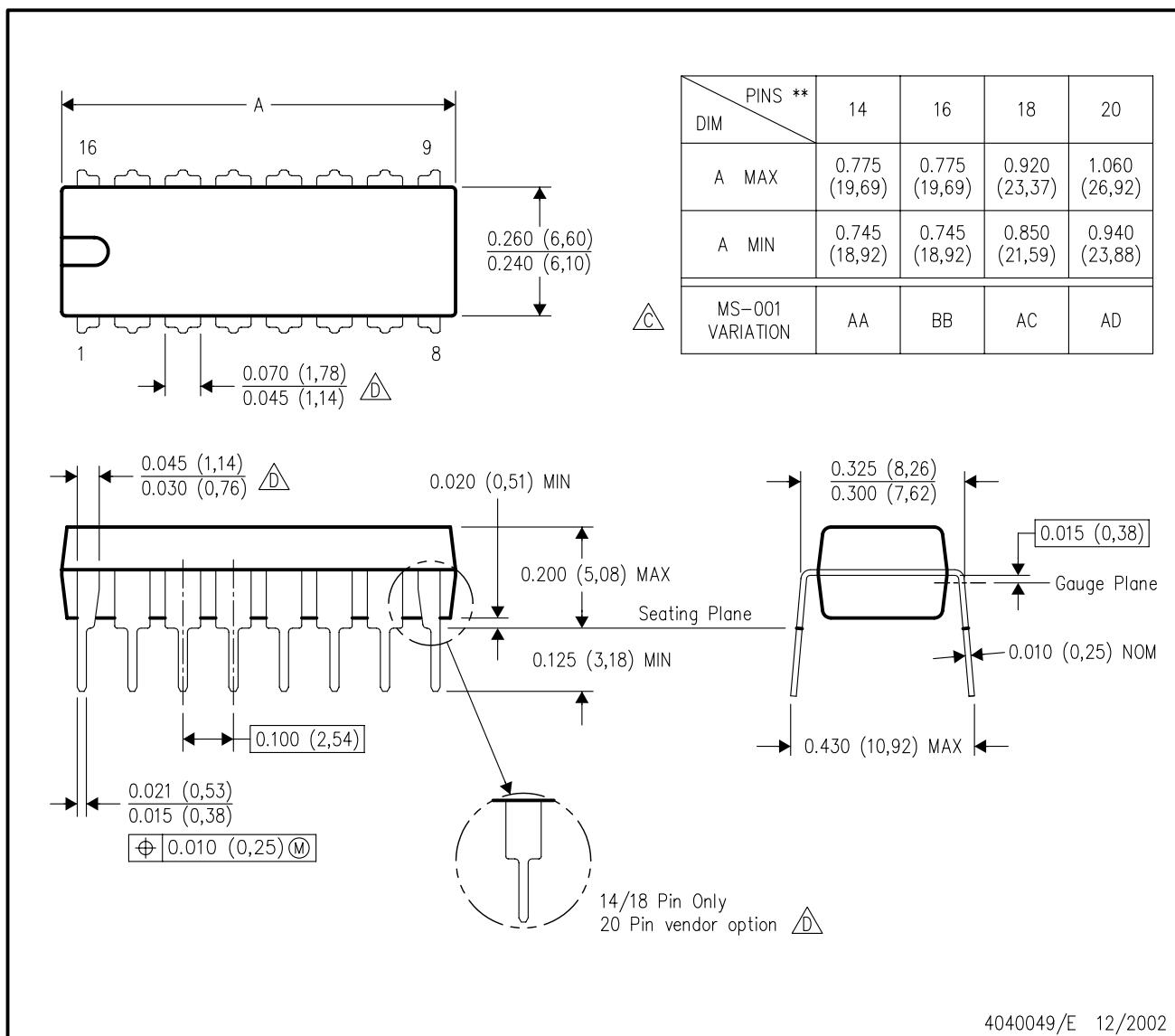
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



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