PROLINX™ GS7032
Digital Video Serializer

DATA SHEET

FEATURES

- **SMPTE 259M-C compliant (270Mb/s)**
- **serializes 8-bit or 10-bit data**
- **minimal external components (no loop filter components required)**
- **isolated, dual-output, adjustable cable driver**
- **3.3V and 5.0V CMOS/TTL compatible inputs**
- **lock detect indication**
- **SMPTE scramble and NRZI coding bypass option**
- **EDH support with GS9001, GS9021**
- **Pb-Free and RoHS Compliant**

APPLICATION

SMPTE 259M-C parallel to serial interfaces for video cameras, VTRs, signal generators; Generic parallel to serial conversion.

DESCRIPTION

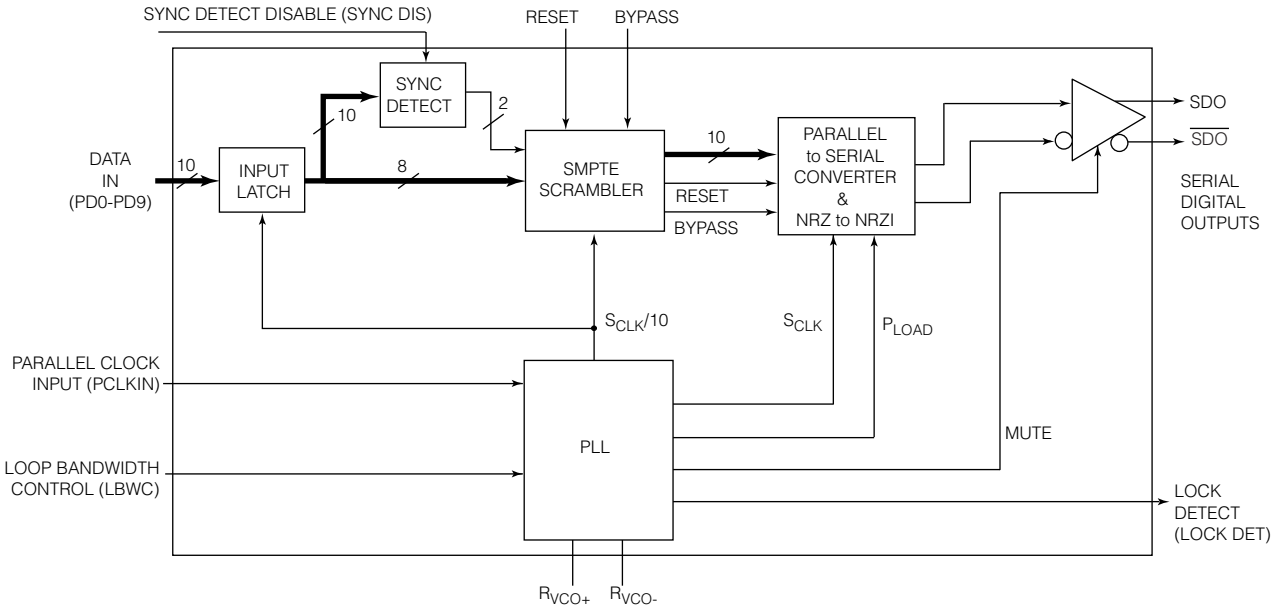
The GS7032 is designed to encode and serialize SMPTE 125M bit parallel digital video signals as well as other 8-bit or 10-bit parallel formats. This device performs the following functions:

- sync detection
- parallel to serial conversion
- data scrambling (using the $X^9 + X^4 + 1$ algorithm)
- 10x parallel clock multiplication
- conversion of NRZ to NRZI serial data

The GS7032 features 270M/bs data rate with a single VCO resistor. Other features include a lock detect output, NRZI encoding and SMPTE scrambler bypass, a sync detect disable, and an isolated dual output cable driver suitable for driving 75Ω loads.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	Pb-FREE AND RoHS COMPLIANT
GS7032 - CVM	44 pin TQFP	0°C to 70°C	No
GS7032 - CVME3	44 pin TQFP	0°C to 70°C	Yes



BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage ($V_S = V_{CC}$-V_{EE})	5.5V
Input Voltage Range (any input)	$V_{EE}<V_{IN}<V_{CC}$
DC Input Current (any one input)	5mA
Power Dissipation (V_{CC} = 5.25V)	1200mW
$\theta_{j\text{-}a}$	42.5°C/W
$\theta_{j\text{-}c}$	6.4°C/W
Maximum Die Temperature	125°C
Operating Temperature Range	$0°C \le T_A \le 70°C$
Storage Temperature Range	$-65°C \le T_S \le 150°C$
Lead Temperature (soldering, 10 sec)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0° – 70°C unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Positive Supply Voltage	V_{CC}	Operating Range	4.75	5.00	5.25	V		3
Power (System Power)	P	V_{CC} = 5.0V, T = 25°C (2 outputs)	-	550	-	mW		5
Supply Current	I_{CC}	V_{CC} = 5.25V (2 outputs)	-	-	160	mA		1
		V_{CC} = 5.0V, T = 25°C (2 outputs)	-	110	-	mA		3
Data & Clock Inputs (PD[9:0] PCLKIN) SYNC DIS	V_{IH}	Logic Input High (wrt V_{EE})	2.4	-	-	V		3
	V_{IL}	Logic Input Low (wrt V_{EE})	-	-	0.8	V		
	I_L	Input Current	-	-	8.0	µA		
Logic Input Levels (Bypass, RESET)	V_{IH}	Logic Input High (wrt to V_{EE})	2.4	-	-	V		3
	V_{IL}	Logic Input Low (wrt to V_{EE})	-	-	0.8	V		
	I_L	Input Current	-	-	5.0	µA		
Lock Detect Output	V_{OL}	Sinking 500µA	-	-	0.4	V		1

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0° – 70°C unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Serial Data Bit Rate	BR_{SDO}	R_{VCO} = 374Ω	-	270Mb/s	-	Mb/s	SMPTE 259M-C	3
Serial Data Outputs Signal Swing	V_{SDO}	R_{LOAD} = 37.5Ω, R_{SET} = 54.9Ω	740	800	860	mVp-p		1
SD Rise/Fall Times	t_r, t_f	20% - 80%	400	-	700	ps		7
SD Overshoot/Undershoot			-	-	7	%	1	7
Output Return Loss	O_{RL}	at 270MHz	15	-	-	dB	1	7
Lock Time	t_{LOCK}	Worst case	-	-	5	ms		6
Min Loop Bandwidth	BW_{MIN}	LBWC = Grounded : BW_{MIN}	-	220	-	kHz		7
Typical Loop Bandwidth	BW_{TYP}	LBWC = Floating : $\sqrt{10}$ BW_{MIN}	-	500	-	kHz		7
Max Loop Bandwidth	BW_{MAX}	LBWC = V_{CC} : 10 BW_{MIN}	-	1.7	-	MHz		7
Intrinsic Jitter (6 σ)		LBWC = V_{CC} (270Mb/s)	-	0.08	-	UI		3
Data & Clock Inputs (PD[9:0] PCLKIN)	t_{SU}	Setup Time at 25°C	2.5	-	-	ns		3
	t_H	Hold Time at 25°C	2.0	-	-	ns		3

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
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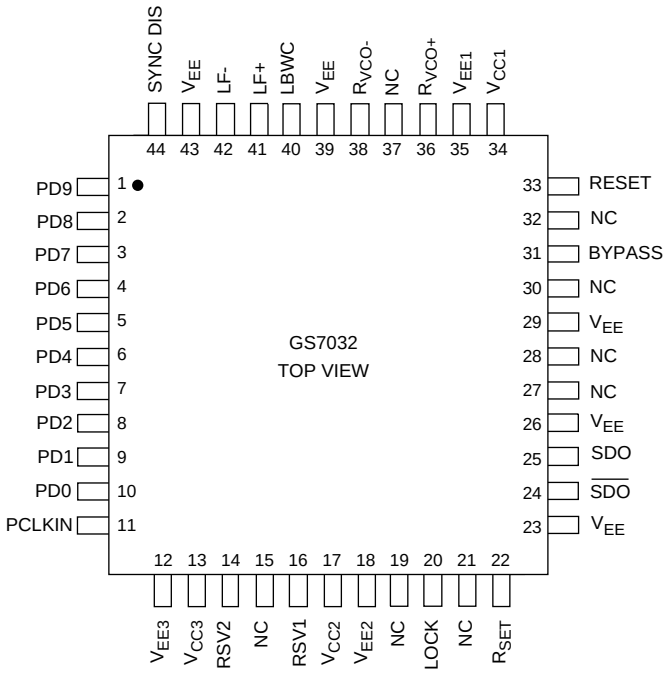
NOTES

1. Depends on PCB layout.

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1-10	PD9 - PD0	I	CMOS or TTL compatible parallel data inputs. PD0 is the LSB and PD9 is the MSB.
11	PCLKIN	I	CMOS or TTL compatible parallel clock input.
12	V_{EE3}	-	Most negative power supply connection for parallel data and clock inputs.
13	V_{CC3}	-	Most positive power supply connection for parallel data and clock inputs.
14	RSV2	I	Reserved pin. Do not connect.
15, 19, 21, 27, 28, 30, 32, 37	NC	I	No connect.
16	RSV1	I	Reserved pin. Always connect to V_{CC}.
17	V_{CC2}	-	Most positive power supply connection for internal logic and digital circuits.
18	V_{EE2}	-	Most negative power supply connection for internal logic and digital circuits.
20	LOCK	O	TTL level which is high when the internal PLL is locked.
22	R_{SET}	I	External resistor used to set the data output amplitude for SDO and $\overline{SDO}$.
23, 26, 29	V_{EE}	-	Most negative power supply connection for shielding (not connected).
24, 25	$\overline{SDO}$, SDO	O	Primary, current mode, 75Ω cable driving output (inverse and true)
31	BYPASS	I	When high, the SMPTE Scrambler and NRZ encoder are bypassed.

PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
33	RESET	I	Resets the scrambler when asserted.
34	V_{CC1}	-	Most positive power supply connection for analog circuits.
35	V_{EE1}	-	Most negative power supply connection for analog circuits.
36, 38	R_{VCO}+, R_{VCO}-	I	Differential VCO current setting resistor that sets the VCO frequency.
39, 43	V_{EE}	-	Most negative power supply connection (substrate).
40	LBWC	I	TTL level loop bandwidth control that adjusts the PLL bandwidth to optimize for lowest jitter. If the pin is set to ground the loop bandwidth is BW_{MIN}. If the pin is left floating, the loop bandwidth is approximately 3 BW_{MIN}, if the pin is tied to V_{CC} the loop bandwidth is approximately10 BW_{MIN}
41, 42	LF+, LF-	I	Differential loop filter pins to optimize loop transfer performance at low loop bandwidths (NC if not used).
44	SYNC DIS	I	Sync detect disable. Logic high disables sync detection. Logic low allows 8 bit operation by mapping 000-003 to 000 and 3FC-3FF to 3FF.

TYPICAL PERFORMANCE CURVES

(V_S = 5V, T_A = 25°C unless otherwise shown. Guard band tested to 70°C only.)

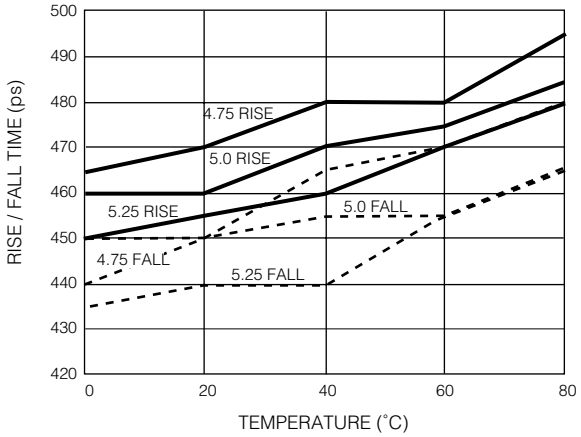


Fig. 1 Rise/Fall Times vs. Temperature

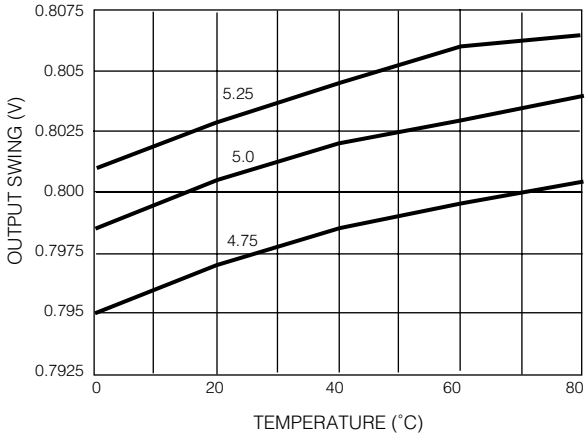


Fig. 3b Output Swing vs. Temperature (800mV)

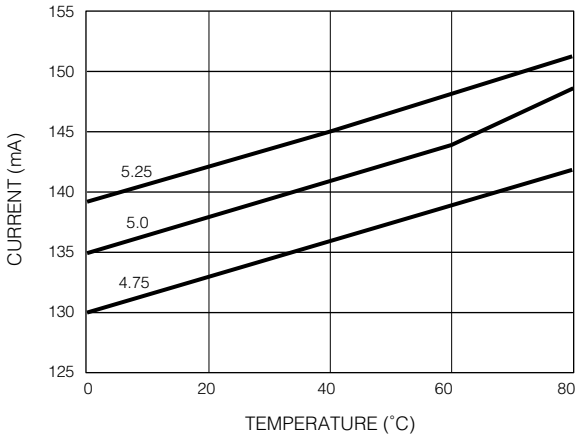


Fig. 2 Supply Current vs. Temperature (SDO ON)

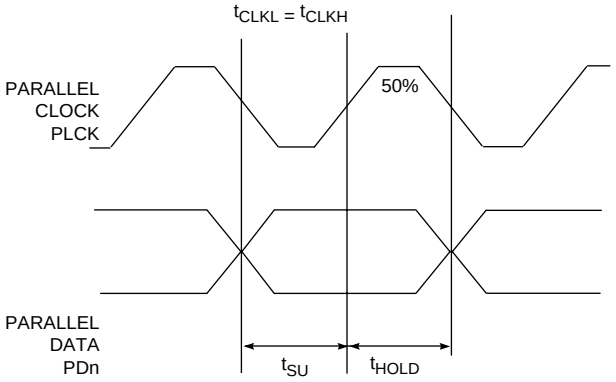


Fig. 4 Waveforms

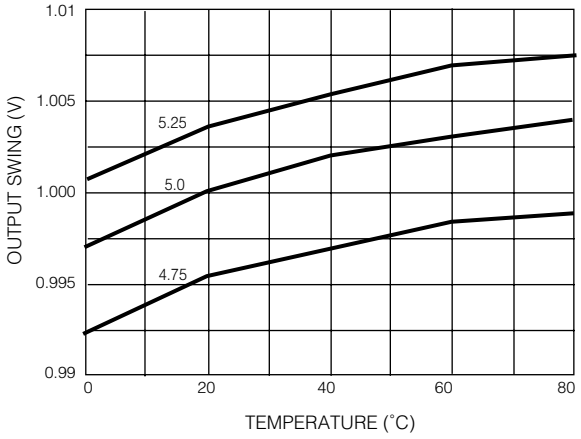


Fig. 3a Output Swing vs. Temperature (1000mV)

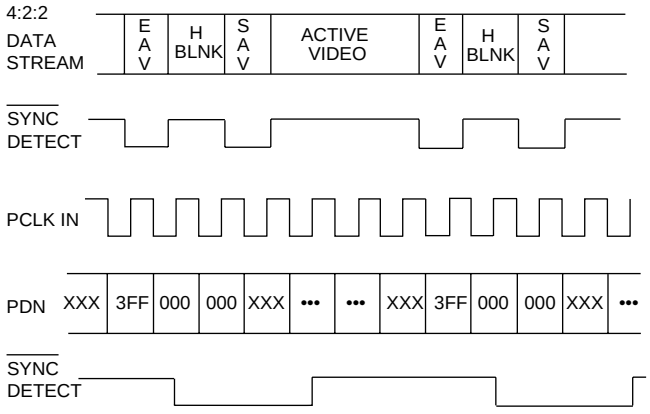


Fig. 5 Timing Diagram

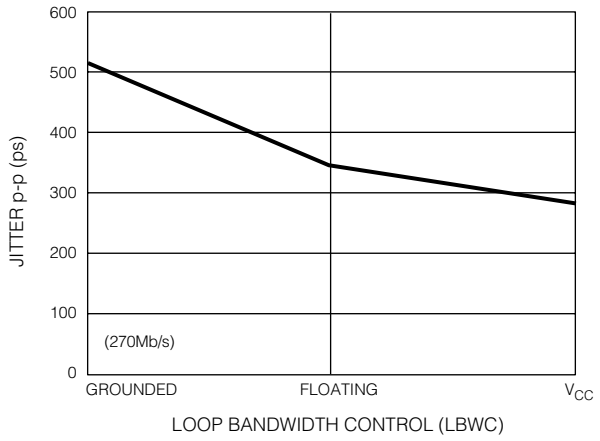


Fig. 6 Output Jitter vs. LBWC

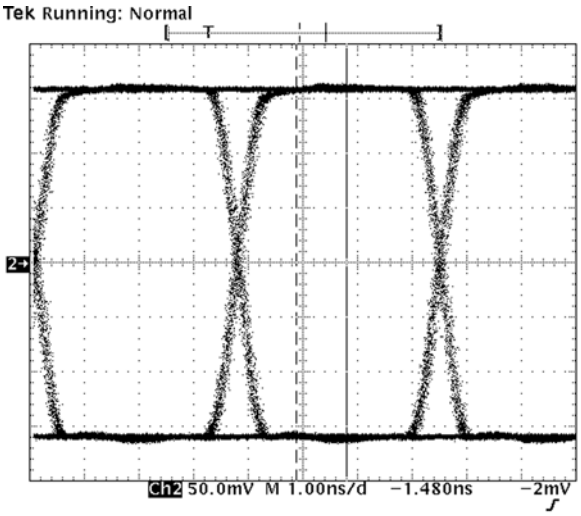


Fig. 7 Output Eye Diagram (270Mb/s)

DETAILED DESCRIPTION

The GS7032 Serializer is a bipolar integrated circuit used to convert parallel data into a serial format according to the SMPTE 259M-C standard. The device encodes both 8-bit and 10-bit TTL-compatible parallel signals producing serial data rates at 270Mb/s. It operates from a single 5V supply and is packaged in a 44 pin TQFP.

Functional blocks within the device include the following:

- input latches
- sync detector
- parallel to serial converter
- SMPTE scrambler
- NRZ to NRZI converter
- internal cable driver
- PLL for 10x parallel clock multiplication
- lock detect

The parallel data (PD0-PD9) and parallel clock (PCLKIN) are applied via pins 1 through 11 respectively.

1. SYNC DETECTOR

The Sync Detector looks for the reserved words used in the TRS-ID sync word. The reserved words are 000-003 and 3FC-3FF in 10-bit hexadecimal, or 00 and FF in 8-bit hexadecimal. When the occurrence of either all zeros or all ones at inputs PD2-PD9 are detected, the lower two bits PD0 and PD1 are forced to zeros or ones, respectively. This makes the system compatible with 8-bit or 10-bit data.

For non-SMPTE standard parallel data, the Sync Detector can be disabled with a logic input, Sync Detect Disable (pin 44).

2. SCRAMBLER

The Scrambler is a linear feedback shift register used to pseudo-randomize the incoming serial data according to the fixed polynomial (X^9+X^4+1). This minimizes the DC component in the output serial data stream. The NRZ to NRZI converter uses another polynomial (X+1) to convert a long sequence of ones to a series of transitions, minimizing polarity effects. These functions can be disabled by setting BYPASS high (pin 31).

3. PHASE LOCKED LOOP

The PLL performs parallel clock multiplication and provides the timing signal for the serializer. It is composed of a phase/frequency detector (with no dead zone), charge pump, VCO, a divide-by-ten counter, and a divide by two counter.

The phase/frequency detector allows a wider capture range and faster lock time than can be achieved with a phase discriminator alone. The discrimination of frequency also eliminates harmonic locking. With this type of discriminator, the PLL can be over-damped for good stability without sacrificing lock time.

The charge pump delivers a 'charge packet' to the loop filter which is proportional to the system phase error. Internal voltage clamps are used to constrain the loop filter voltage between approximately 1.8 and 3.4 volts.

The VCO is a differential low phase noise, factory trimmed design that provides increased immunity to PCB noise and precise control of the VCO centre frequency. The VCO has a pull range of ±15% about the centre frequency. The single external resistor, R_{VCO}, sets the VCO frequency.

4. VCO CENTRE FREQUENCY SELECTION

The recommended R_{VCO} value for auto rate SMPTE 259M-C applications (270Mb/s) is 374Ω *(see the Typical Application Circuit).*

The VCO and an internal divider generate the PLL clock.

5. LOCK DETECT OUTPUT

The Lock Detect output is available from pin 20 and is HIGH when the loop is locked. When the loop is not locked, the lock detect circuit mutes the serial data outputs.

6. SERIAL OUTPUTS

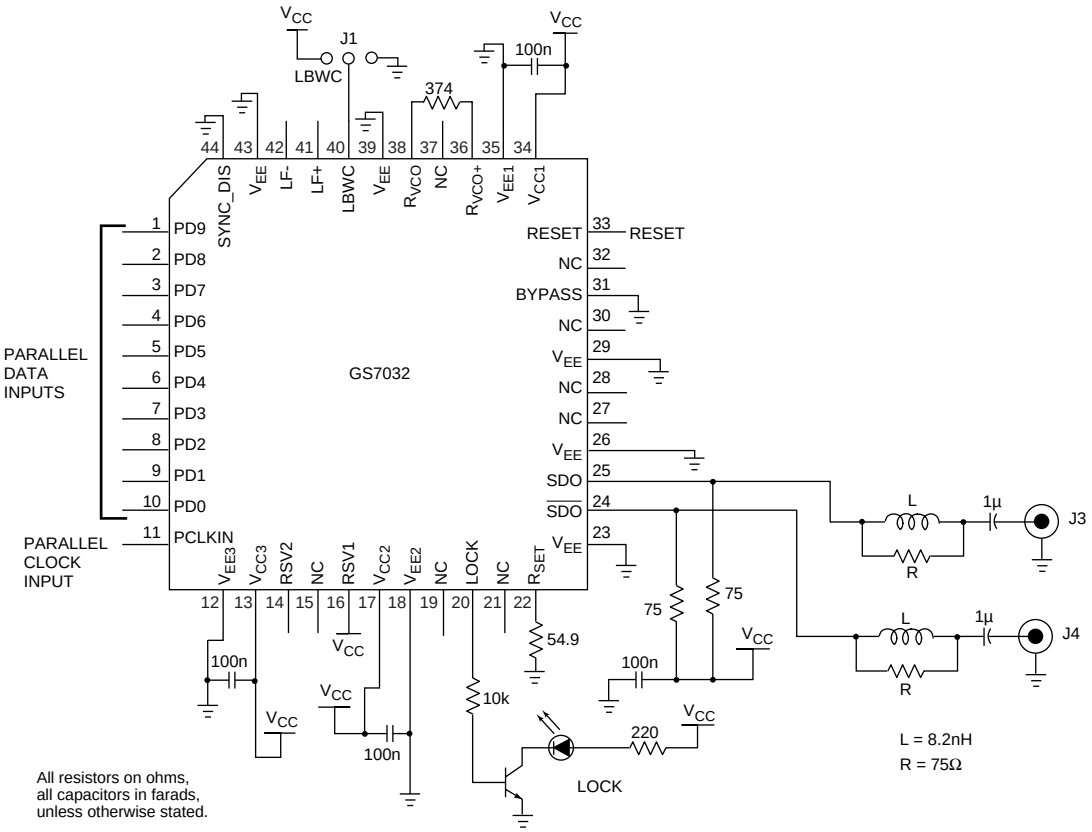
The true and complement serial data, $\overline{SDO}$ and SDO, are available from pins 24 and 25. These outputs will drive two 75Ω co-axial cables with SMPTE level serial digital video signals.

R_{SET} calculation:

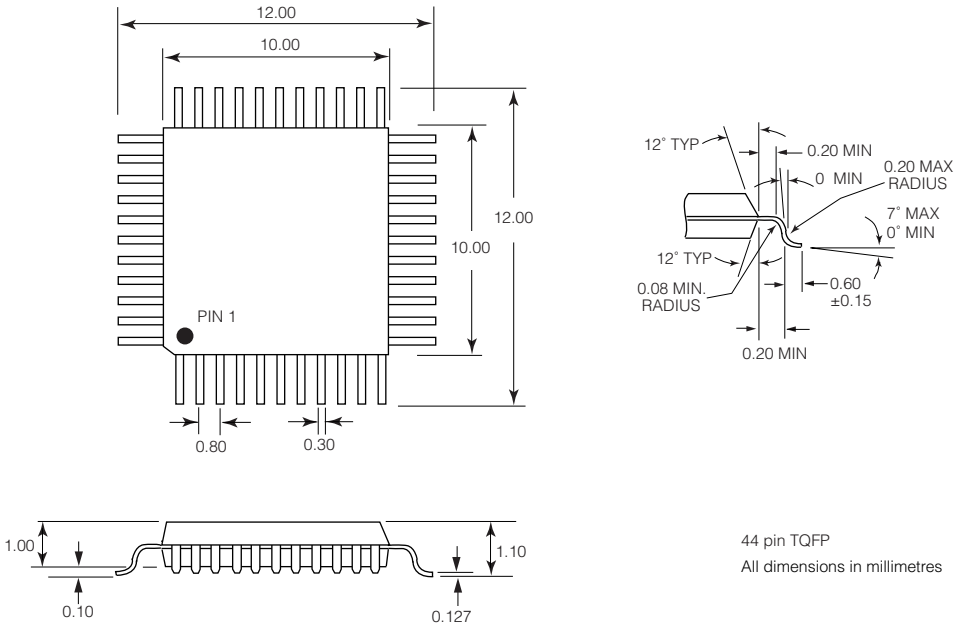
$$R_{SET} = \frac{1.154 \times R_{LOAD}}{V_{SDO}}$$

where $R_{LOAD} = R_{PULL\text{-}UP} \parallel Z_O$

TYPICAL APPLICATION CIRCUIT



PACKAGE DIMENSIONS



44 pin TQFP

All dimensions in millimetres

REVISION HISTORY

VERSION	ECR	DATE	CHANGES AND/OR MODIFICATIONS
4	136659	May 2005	Removed reference to EDH FPGA core. Updated Pb-Free and RoHS Compliant part ordering information.

DOCUMENT IDENTIFICATION

DATA SHEET

The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

CAUTION

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

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