CAT4008

8-Channel Constant Current LED Driver

Description

The CAT4008 is an 8 channel constant current driver for LED billboard and other general display applications. LED channel currents are programmed together via an external RSET resistor. Low output voltage operation on the LED channels as low as 0.4 V (for 2 to 100 mA LED current) allows for more power efficient designs.

A high−speed 4−wire serial interface of up to 25 MHz clock frequency controls each individual channel using a shift register and latch configuration. A serial output data pin (SOUT) allows multiple devices to be cascaded and programmed via one serial interface. The device also includes a blanking control pin (BLANK) that can be used to disable all channels independently of the interface.

Thermal shutdown protection is incorporated in the device to disable the LED outputs if the die temperature exceeds a set limit.

The device is available in the 16−lead SOIC (narrow and wide), and TSSOP packages.

Features

- 8 Constant Current−sink Channels
- Serial Interface up to 25 MHz Clock Frequency
- 3 V to 5.5 V Logic Supply
- LED Current Range from 2 mA to 100 mA
- LED Current set by External RSET Resistor
- 300 mV LED Dropout at 30 mA
- Thermal Shutdown Protection
- Available in 16−lead SOIC (150 and 300 mil wide), and TSSOP Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Billboard Display
- Marquee Display
- Instrument Display
- General Purpose Display

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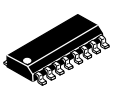
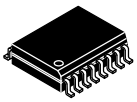


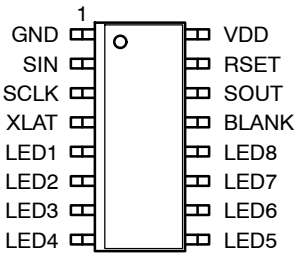
SOIC−16
W SUFFIX
CASE 751BG



SOIC−16
V SUFFIX
CASE 751BH

TSSOP−16
Y SUFFIX
CASE 948AN

PIN CONNECTIONS



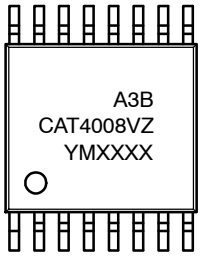
16−Lead SOIC (W, V), TSSOP (Y)
(Top View)

ORDERING INFORMATION

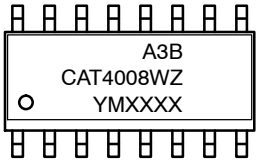
See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

MARKING DIAGRAMS

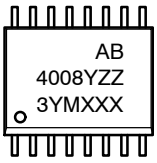
A = Assembly Location
3 = Lead Finish − Matte−Tin
B = Product Revision (Fixed as “B”)
CAT4008W, CAT4008V, 4008Y = Device Code
Z or ZZ = Leave Blank
Y = Production Year (Last Digit)
M = Production Month (1-9, A, B, C)
XXX or XXXX = Last Three of Four Digits of Assembly Lot Number



CAT4008V−T1



CAT4008W−T2



CAT4008Y−T2 or
CAT4008Y−GT2

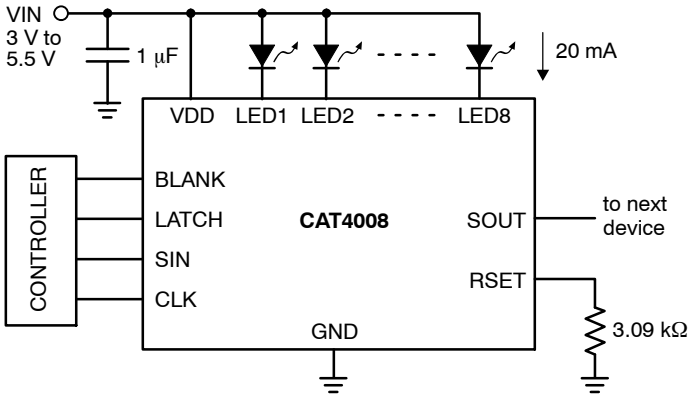


Figure 1. Typical Application Circuit

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
V_{DD} Supply Voltage	6	V
Logic input/output voltage (SIN, SOUT, CLK, BLANK, LATCH)	−0.3 V to V_{DD}+0.3 V	V
LEDn voltage	6	V
DC output current on LED1 to LED8	150	mA
Storage Temperature Range	−55 to +160	°C
Junction Temperature Range	−40 to +150	°C
Lead Soldering Temperature (10 sec.)	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. RECOMMENDED OPERATING CONDITIONS

Parameter	Range	Units
V_{DD}	3.0 to 5.5	V
Voltage applied to LED1 to LED8	0.4 to 5.5	V
LED current RSET control range	up to 100	mA
Ambient Temperature Range	−40 to +85	°C

Table 3. ELECTRICAL OPERATING CHARACTERISTICS
(V_{DD} = 5.0 V, T_{AMB} = 25°C, over recommended operating conditions unless specified otherwise.)

Symbol	Name	Conditions	Min	Typ	Max	Units
DC CHARACTERISTICS						
$I_{LED-ACC}$	LED Current (any channel)	V_{LED} = 1 V, R_{SET} = 3.08 kΩ	18	20	22	mA
		V_{LED} = 1 V, R_{SET} = 1.54 kΩ	36	40	44	
		V_{LED} = 1 V, R_{SET} = 769 Ω		80		
$I_{LED-MAT}$	LED Current Matching (I_{LED} − I_{LEDAVR}) / I_{LEDAVR}	V_{LED} = 1 V, R_{SET} = 3.08 kΩ		±1.5		%
		V_{LED} = 1 V, R_{SET} = 1.54 kΩ	−6.0	±1.5	+6.0	
		V_{LED} = 1 V, R_{SET} = 769 Ω		±2.0		
ΔI_{VDD}	LED current regulation vs. V_{DD}	V_{DD} within 4.5 V and 5.5 V LED current 30 mA		±0.1		% / V
ΔI_{VLED}	LED current regulation vs. V_{LED}	V_{LED} within 1 V and 3 V LED current 30 mA		±0.05		% / V
I_{DDOFF}	Supply Current (all outputs off)	R_{SET} = 3.08 kΩ		2	8	mA
		R_{SET} = 769 Ω		5.5		
I_{DDON}	Supply Current (all outputs on)	R_{SET} = 3.08 kΩ		2.5	9	mA
		R_{SET} = 769 Ω		6.2		
I_{LKG}	LEDn output Leakage	V_{LED} = 5 V, outputs off	−1		1	μA
R_{LATCH}	LATCH Pull−down Resistance		100	180	300	kΩ
R_{BLANK}	BLANK Pull−up Resistance		100	180	300	kΩ
V_{IH} V_{IL}	Logic high input voltage Logic low input voltage		0.7xV_{DD}		 0.3xV_{DD}	V
V_{HYS}	Logic input hysteresis voltage			0.1xV_{DD}		V
I_{IL}	Logic Input leakage current (CLK, SIN)	V_I = V_{DD} or GND	−5	0	5	μA
V_{OH} V_{OL}	SOUT logic high output voltage SOUT logic low output voltage	I_{OH} = −1 mA I_{OL} = 1 mA	V_{CC}−0.3 V		 0.3	V
V_{RSET}	RSET Regulated Voltage	BLANK high, outputs off	1.17	1.20	1.23	V
T_{SD}	Thermal Shutdown			160		°C
T_{HYST}	Thermal Hysteresis			20		°C

Table 4. TIMING CHARACTERISTICS
(For 3.0 V ≤ V_{DD} ≤ 5.5 V, T_{AMB} = 25°C, unless specified otherwise.)

Symbol	Name	Conditions	Min (Note 1)	Typ (Note 2)	Max (Note 1)	Units
CLK						
f_{clk}	CLK Clock Frequency				25	MHz
t_{cwh}	CLK Pulse Width High		20			ns
t_{cwl}	CLK Pulse Width Low		20			ns
SIN						
t_{ssu}	Setup time SIN to CLK		4			ns
t_{sh}	Hold time SIN to CLK		4			ns
LATCH						
t_{lwh}	LATCH Pulse width		20			ns
T_{lh}	Hold time LATCH to CLK		4			ns
T_{lsu}	Setup time LATCH to CLK	Channel Stagger Delay	400			ns
LEDn						
t_{ld}	LED1 Propagation delay	LATCH to LED1 off/on		40	300	ns
t_{ls}	LED Propagation delay stagger	LED(n) to LED(n+1)		17	40	ns
t_{lst}	LED Propagation delay stagger total	LED1 to LED8		120		ns
t_{bd}	BLANK Propagation delay	BLANK to LED(n) off/on		60	300	ns
t_{lr}	LED rise time (10% to 90%)	Pull−up resistor = 50 Ω to 3.0 V		40	200	ns
t_{lf}	LED fall time (90% to 10%)	Pull−up resistor = 50 Ω to 3.0 V		30	250	ns
SOUT						
t_{or}	SOUT rise time (10% to 90%)	C_L = 15 pF		5		ns
t_{of}	SOUT fall time (90% to 10%)	C_L = 15 pF		5		ns
t_{od}	Propagation delay time SOUT	CLK to SOUT	8	15	25	ns

1. All min and max values are guaranteed by design.
2. V_{DD} = 5 V, LED current 30 mA.

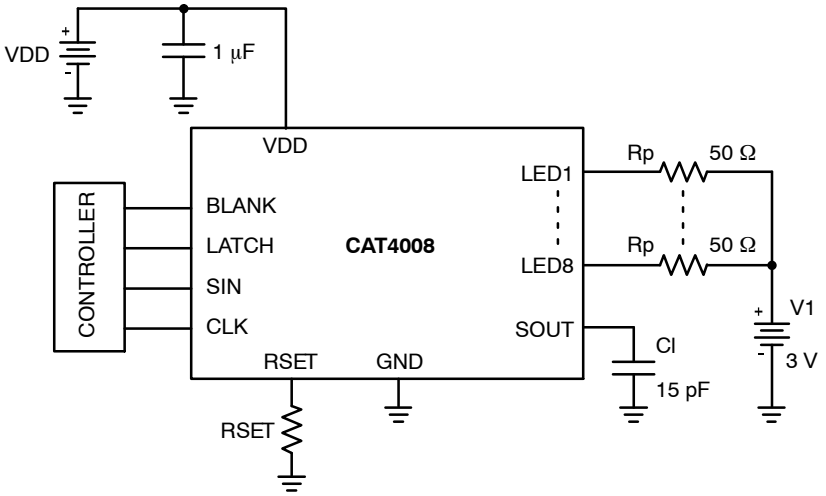


Figure 2. Test Circuit for AC Characteristics

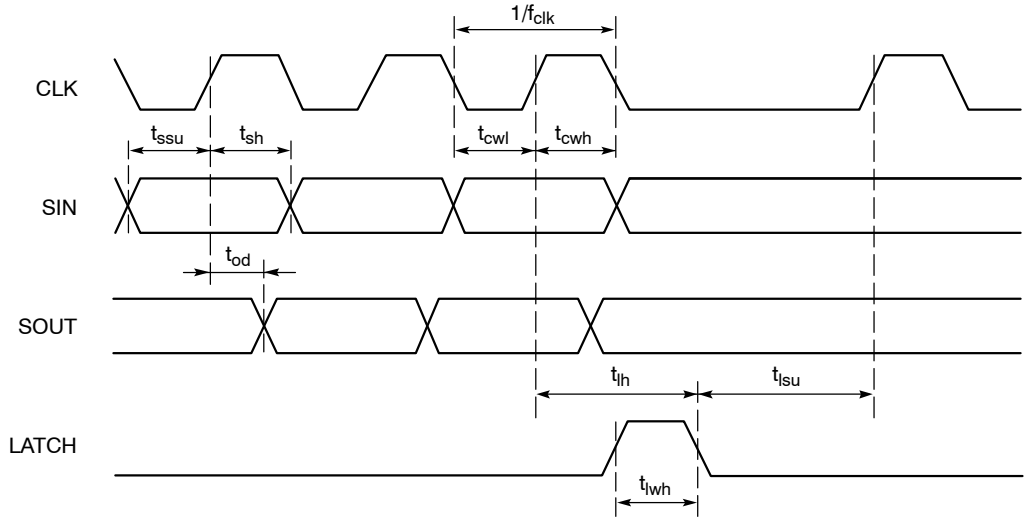


Figure 3. Serial Input Timing Diagram

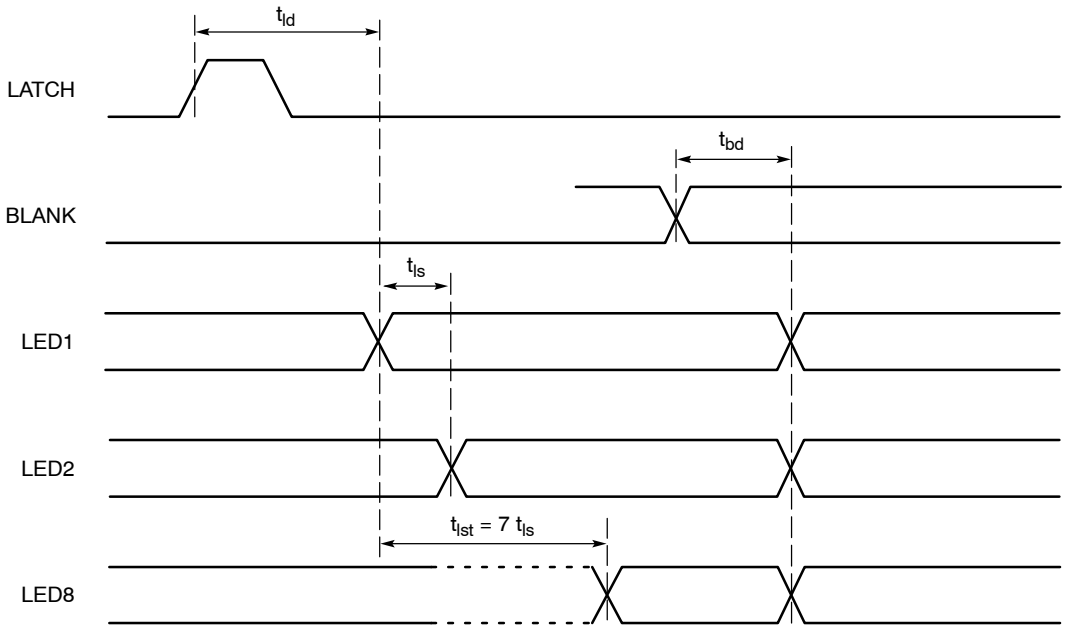


Figure 4. LED Output Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{DD} = 5.0 V, LED current 30 mA, all LEDs On, T_{AMB} = 25°C unless otherwise specified.)

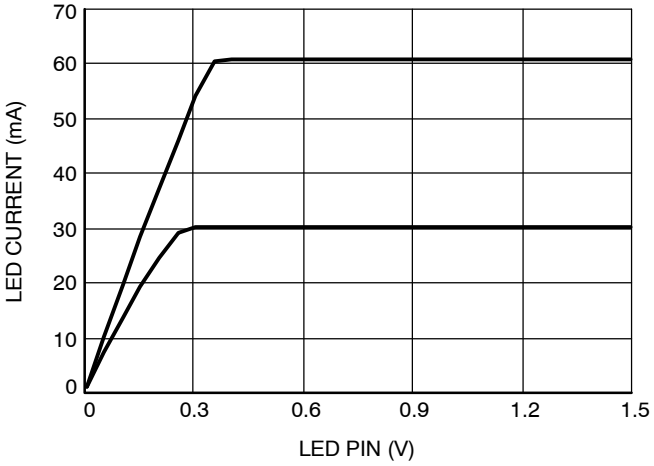


Figure 5. LED Current vs. LED Pin Voltage

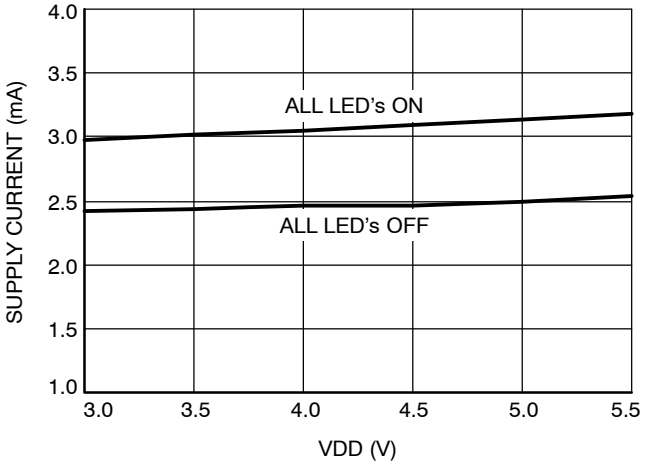


Figure 6. Supply Current vs. VDD Pin Voltage

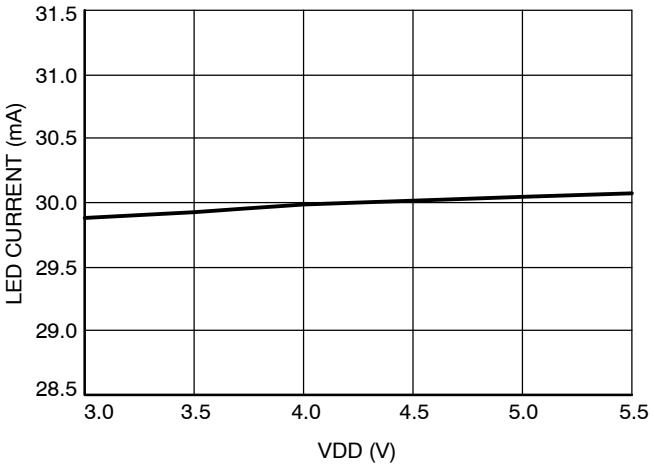


Figure 7. LED Current vs. VDD Pin Voltage

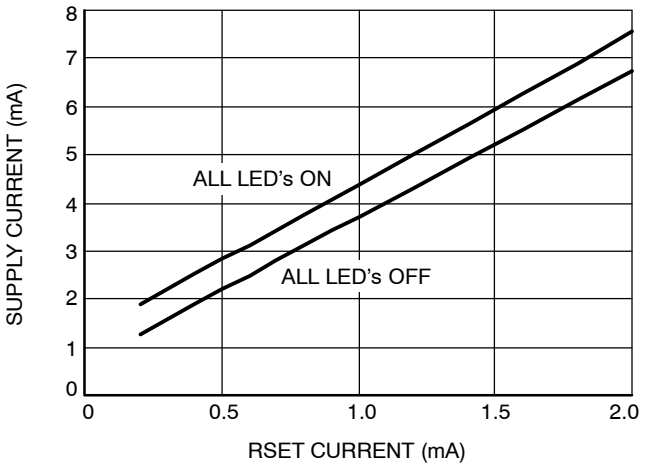


Figure 8. Supply Current vs. RSET Current

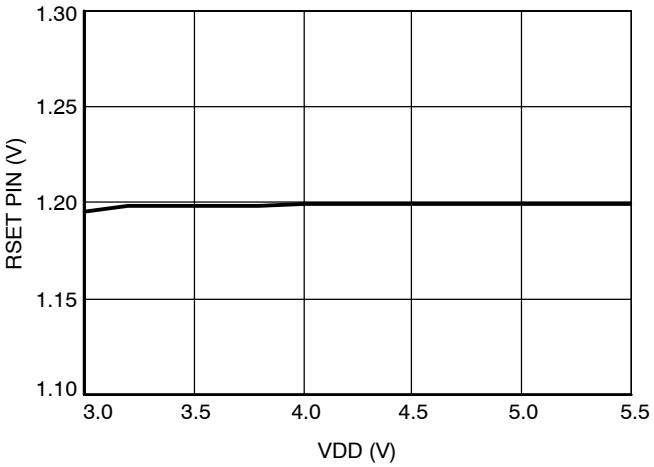


Figure 9. RSET Voltage vs. VDD Pin Voltage

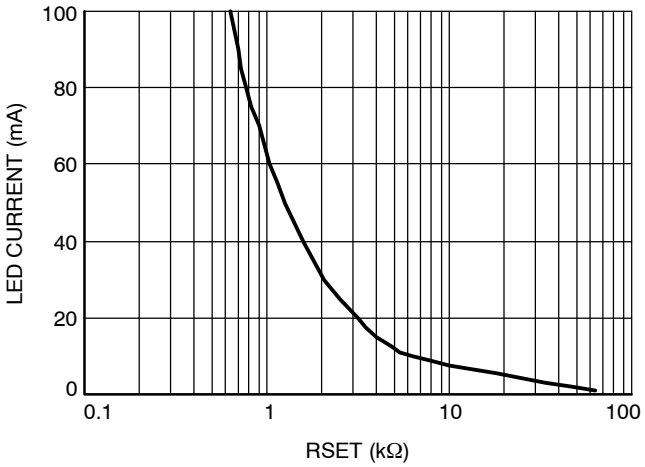


Figure 10. LED Current vs. RSET Resistor

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{DD} = 5.0 V, LED current 30 mA, all LEDs On, T_{AMB} = 25°C unless otherwise specified.)

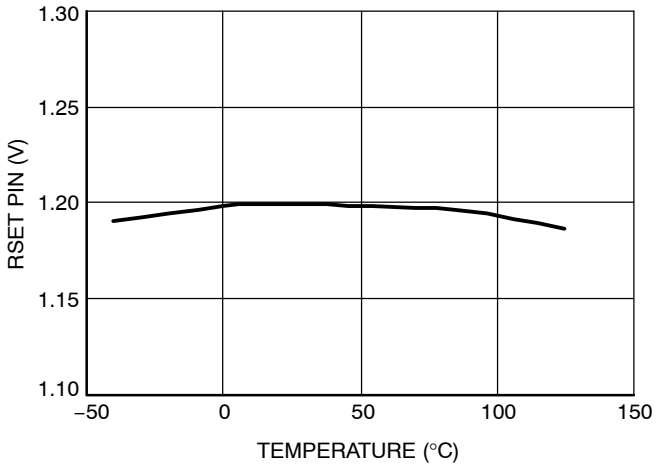


Figure 11. RSET Voltage vs. Temperature

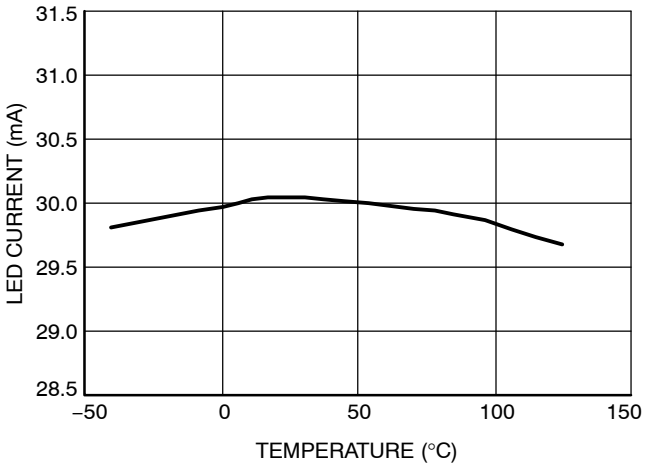


Figure 12. LED Current vs. Temperature

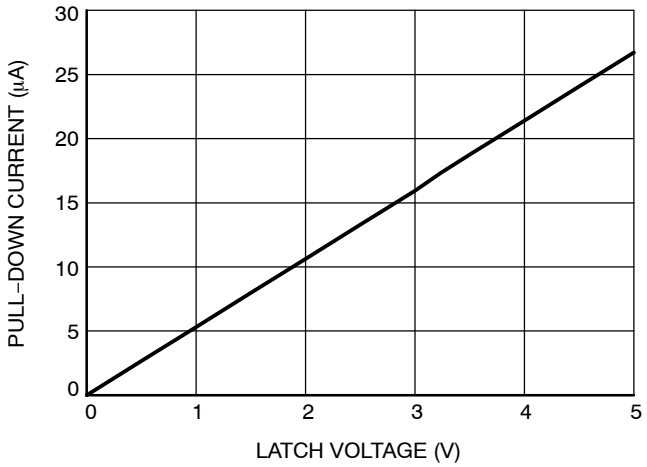


Figure 13. Internal Pull−Down Current (LATCH Pin)

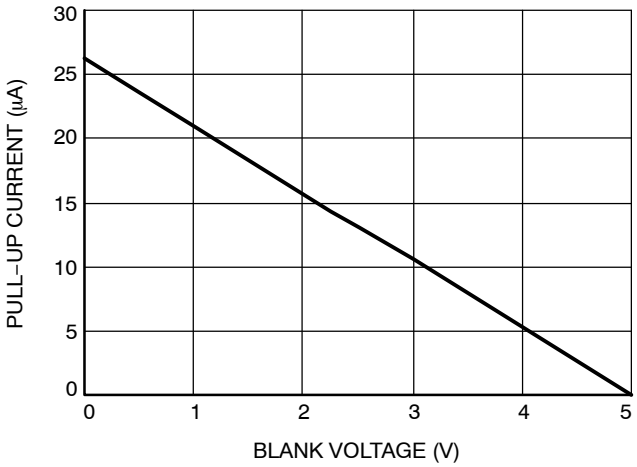


Figure 14. Internal Pull−Up Current (BLANK Pin)

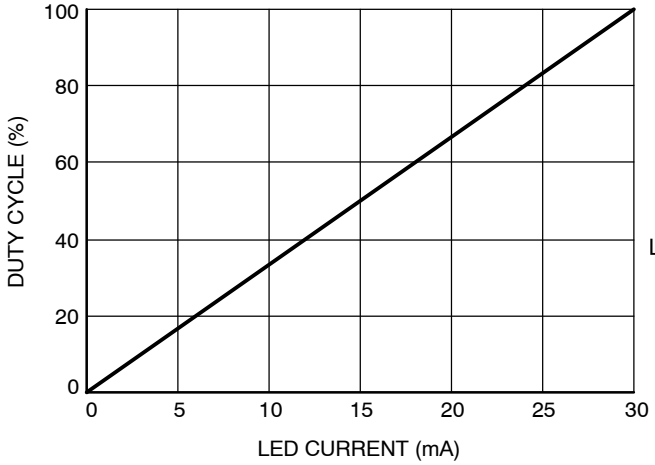


Figure 15. PWM Dimming on BLANK Pin (f = 10 kHz)

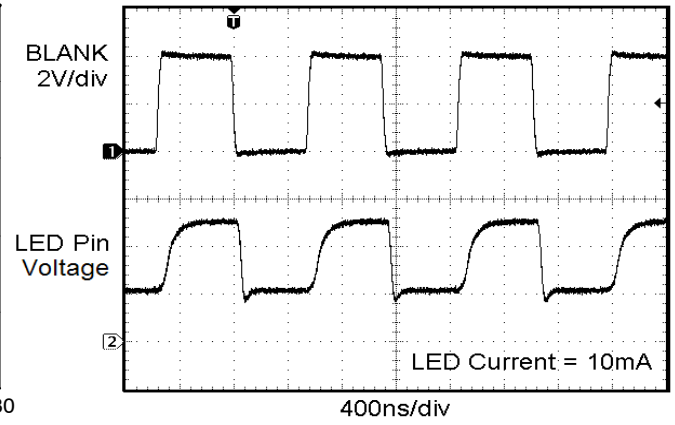


Figure 16. BLANK Transient Response

Table 5. PIN DESCRIPTION

Name	Function
GND	Ground
SIN	Serial data input pin
CLK	Serial clock input pin
LATCH	Latch serial data to output registers
LED1−LED8	LED channel 1 to 8 cathode terminals
BLANK	Enable / disable all channels
SOUT	Serial data output pin.
RSET	LED current set pin
VDD	Positive supply Voltage

Pin Function

GND is the ground reference pin for the device. This pin must be connected to the ground plane on the PCB.

SIN is the serial data input. Data is loaded into the internal register on each rising edge of CLK.

CLK is the serial clock input. On each rising CLK edge, data is transferred from SIN to the internal 8−bit serial shift register.

LATCH is the latch data input. On the rising edge of LATCH, data is loaded from the 8−bit serial shift register into the output register latch. On the falling edge, this data is latched in the output register and isolated from the state of the serial shift register.

LED1 – LED8 are the LED current sink channels. These pins are connected to the LED cathodes. The current sinks drive the LEDs with a current equal to about 51 times RSET pin current. For the LED sink to operate correctly, the voltage on the LED pin must be above 0.4 V.

BLANK is the LED channel enable and disable input pin. When low, LEDs are enabled according to the output latch register content. When high, all LEDs are off, while preserving the data in the output latch register.

SOUT is the serial data output of the 8−bit serial shift register. This pin is used to cascade several devices on the serial bus. The SOUT pin is then connected to the SIN input of the next device on the serial bus to cascade.

RSET is the LED current setting pin. A resistor is connected between this pin and ground. Each LED channel current is set to about 51 times the current pulled out of the pin. The RSET pin voltage is regulated to 1.2 V.

VDD is the positive supply pin voltage for the entire device. A small 1 μF ceramic is recommended close to pin.

Current Setting Resistor

Table 6 lists standard resistor values for various LED current settings.

Table 6. LED CURRENT AND RSET RESISTOR VALUES

LED Current [mA]	R_{SET} [kΩ]
10	6.19
20	3.09
30	2.05
40	1.54
60	1.02
80	0.768

Block Diagram

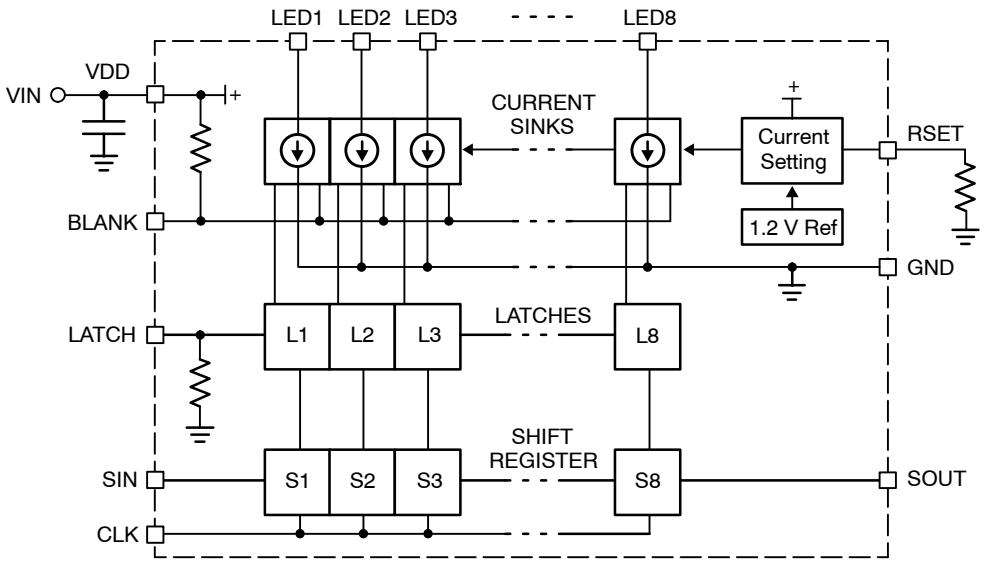


Figure 17. CAT4008 Functional Block Diagram

Basic Operation

The CAT4008 uses 8 tightly matched current sinks to accurately regulate the LED current in each channel. The external resistor, R_{SET}, is used to set the LED channel current to about 51 times the current in R_{SET}.

$$\text{LED current} \cong 51 \times \frac{1.2}{R_{SET}}$$

Tight current regulation for all channels is possible over a wide range of input and LED voltages due to independent current sensing circuitry on each channel. The LED channels have a maximum dropout of 0.4 V for most current and supply voltage conditions. This helps improve the heat dissipation and efficiency of the LED driver.

Upon power−up, an under−voltage lockout circuit clears all latches and shift registers and sets all outputs to off. Once the under−voltage lockout threshold has been reached the device can be programmed.

The driver delays the activation of each consecutive LED output channel by 17 ns (typical). Relative to LED1, LED2 is delayed by 17 ns, LED3 by 34 ns and LED8 by 120 ns typical. The delay is introduced when LATCH is activated. The delay minimizes the inrush current on the LED supply by staggering the turn on and off current spikes over a period of time and therefore allowing usage of smaller bypass capacitors.

Pull−up and pull−down resistors are internally provided to set the state of the BLANK and LATCH pins to the off−state when not externally driven.

Serial Interface

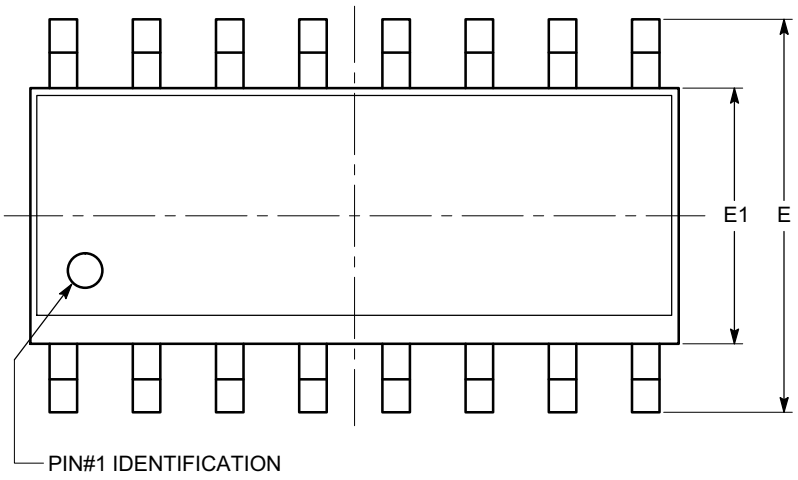
A high−speed serial 4−wire interface is provided to program the state of each LED on or off. The interface contains an 8−bit serial to parallel shift register (S1−S8) and an 8−bit latch (L1−L8). Programming the serial to parallel register is accomplished via SIN and CLK input pins. On each rising edge of the CLK signal, the data from SIN is moved through the shift register serially. Data is also moved out of SOUT which can be connected to a next device if programming more than one device on the same interface.

On the rising edge of LATCH, the data contents of the serial to parallel shift register is reflected in the latches. On the falling edge of LATCH, the state of the serial to parallel register at that particular time is saved in the latches and does not change irrespective of the contents of the serial to parallel register.

BLANK is used to disable all LEDs (turn off) simultaneously while maintaining the same data in the latch register. When low, the LED outputs reflect the data in the latches. When high, all outputs are high impedance (zero current).

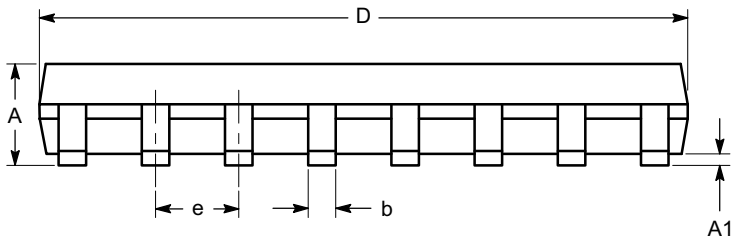
PACKAGE DIMENSIONS

SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

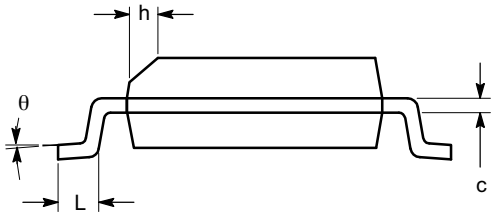


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

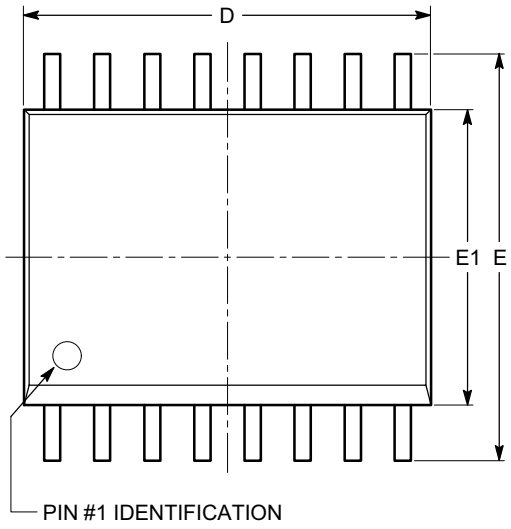


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

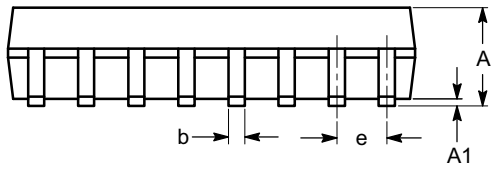
PACKAGE DIMENSIONS

SOIC−16, 300 mils
CASE 751BH−01
ISSUE A

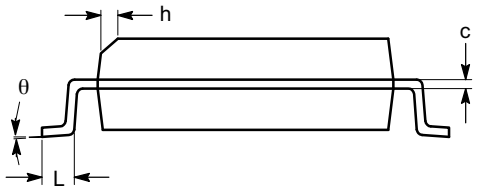


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
b	0.33	0.41	0.51
c	0.18	0.23	0.28
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e	1.27 BSC		
h	0.25		0.75
L	0.38	0.81	1.27
θ	0°		8°



SIDE VIEW

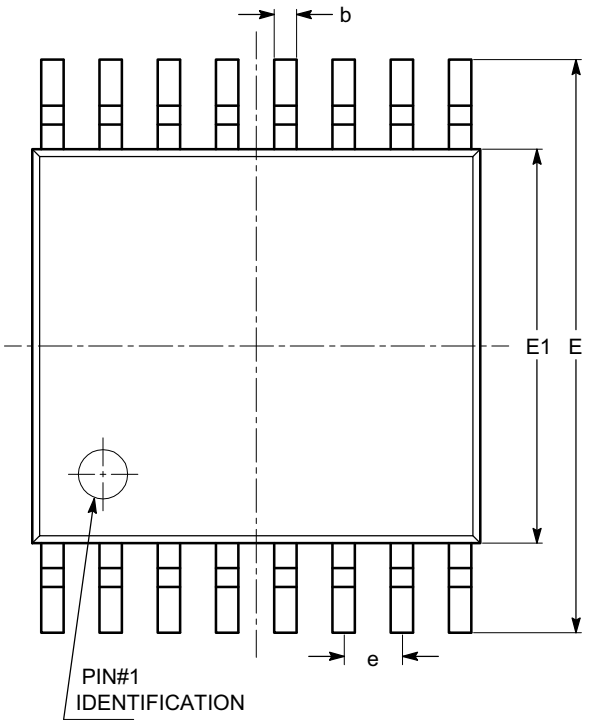


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

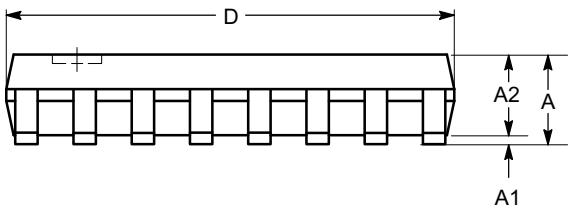
PACKAGE DIMENSIONS

TSSOP16, 4.4x5
CASE 948AN−01
ISSUE O

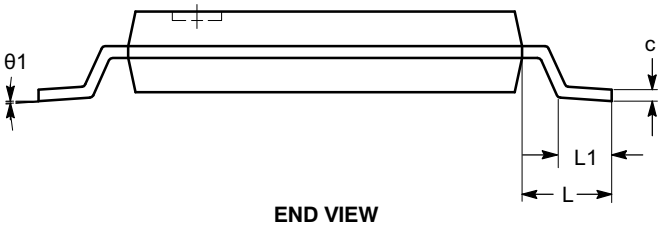


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Example of Ordering Information (Note 5)

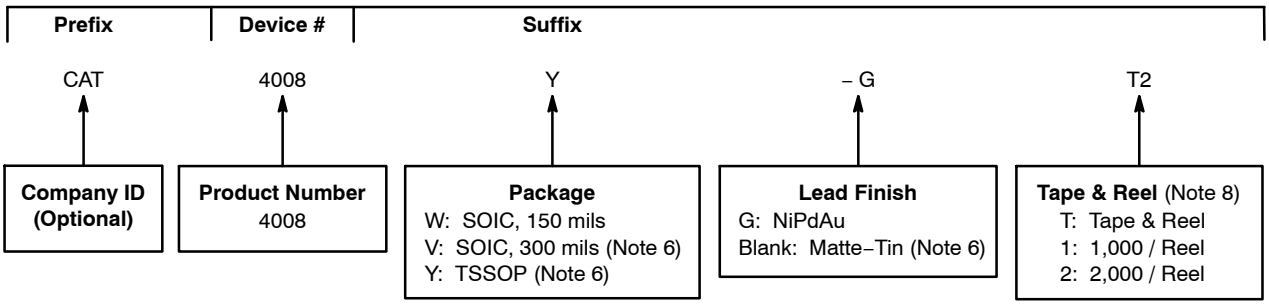


Table 7. ORDERING INFORMATION

Part Number	Package	Quantity per Reel	Package Marking
CAT4008W-T2	SOIC16 (N) (Note 9)	2,000	CAT4008W
CAT4008V-T1	SOIC16 (W) (Notes 6, 9)	1,000	CAT4008V
CAT4008Y-T2	TSSOP16 (Notes 6, 9)	2,000	CAT4008Y
CAT4008Y-GT2	TSSOP16 (Note 10)	2,000	CAT4008Y

3. All packages are RoHS−compliant (Lead−free, Halogen−free).
4. The standard lead finish is Matte−Tin.
5. The device used in the above example is a CAT4008Y−GT2 (TSSOP, NiPdAu, Tape & Reel, 2,000/Reel).
6. Contact factory for package availability.
7. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
8. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
9. Matte−Tin Plated Finish (RoHS−compliant).
10. NiPdAu Plated Finish (RoHS−compliant).

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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