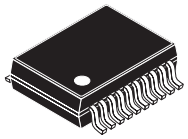
Document Number: MPC17529
Rev 2.0, 12/2013

# 0.7 A Dual H-Bridge Motor Driver with 3.0V/5.0V Compatible Logic I/O

**17529**

**DUAL H-BRIDGE**



**EV SUFFIX (PB-FREE)**
**98ASA10616D**
**20-PIN VMFP**

The 17529 is a monolithic dual H-Bridge power IC ideal for portable electronic applications containing bipolar step motors and/or brush DC-motors (e.g., cameras and disk drive head positioners).

The 17529 operates from 2.0 V to 6.8 V, with independent control of each H-Bridge via parallel MCU interface (3.0 V and 5.0 V compatible logic). The device features an on-board charge pump, as well as built-in shoot-through current protection and an undervoltage shutdown function.

The 17529 has four operating modes: forward, reverse, brake, and tri-stated (high-impedance). The 17529 has a low total $R_{DS(ON)}$ of 1.2 Ω (max at 25 °C).

The 17529's low output resistance and high slew rate provides efficient drive for many types of micromotors.

**ORDERING INFORMATION**

| Device (For Tape and Reel, add an R2 Suffix) | Temperature Range ($T_A$) | Package |
|---|---|---|
| MPC17529EV/EL | -20 °C to 65 °C | 20 VMFP |

### Features

- Low total $R_{DS(ON)}$ 0.7 Ω (typ), 1.2 Ω (max) at 25 °C
- Output current 0.7 A (DC), 1.4 A (peak)
- Shoot-through current protection circuit
- 3.0 V/5.0 V CMOS-compatible inputs
- PWM control input frequency up to 200 kHz
- Built-in charge pump circuit
- Low power consumption
- Undervoltage detection and shutdown circuit

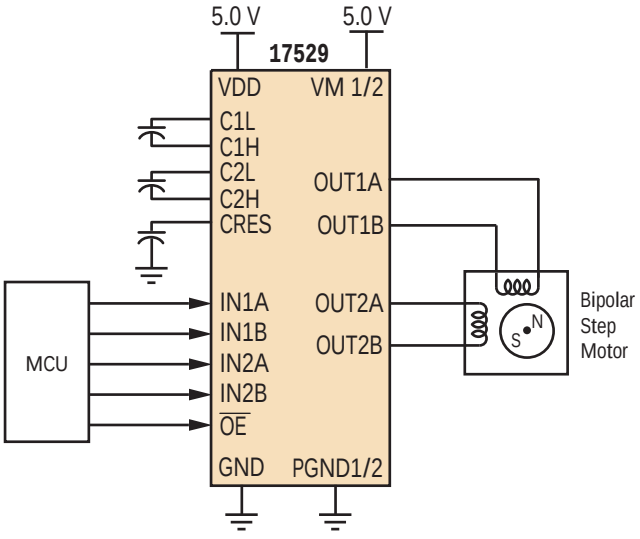



**Figure 1. 17529 Simplified Application Diagram**

## INTERNAL BLOCK DIAGRAM

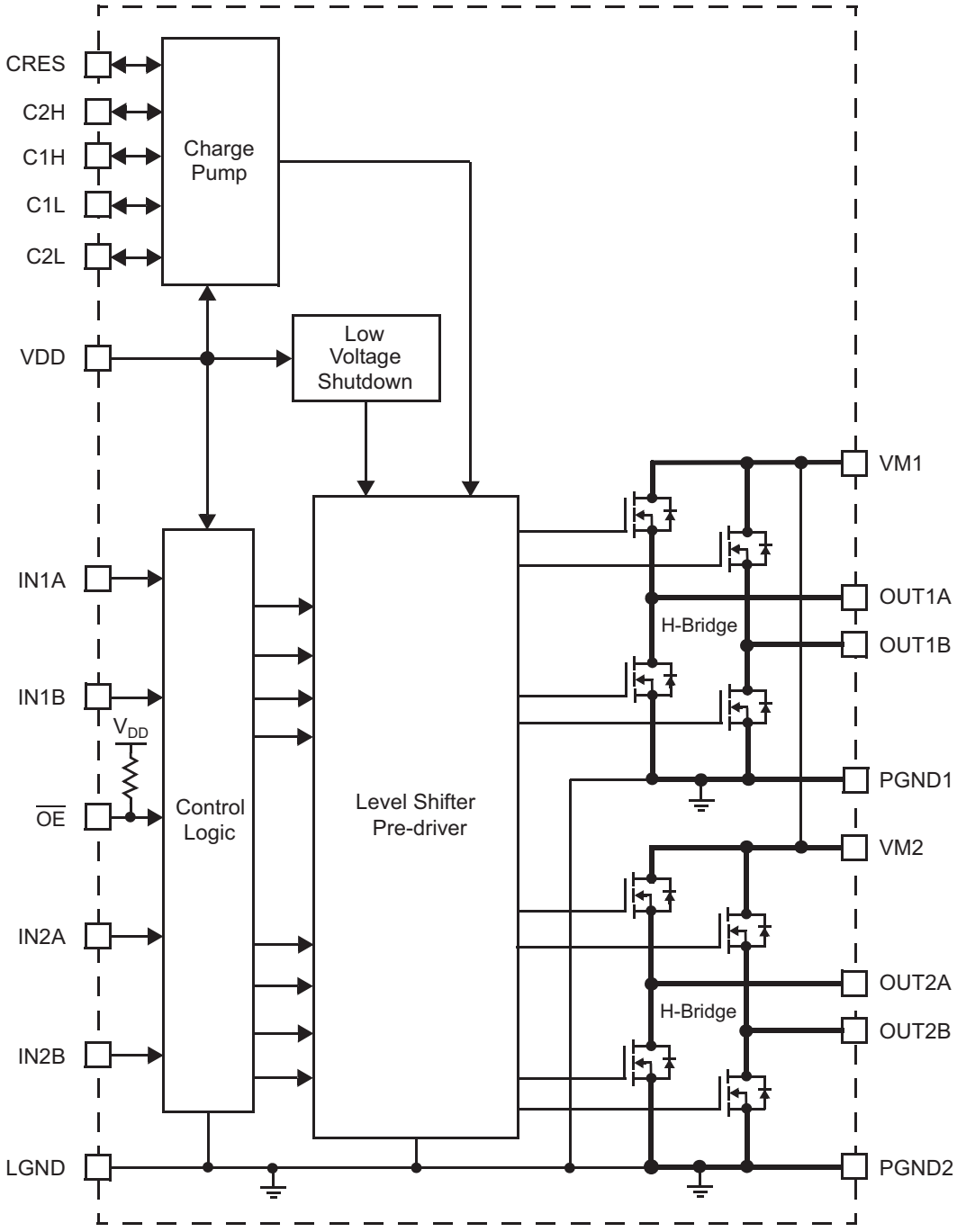



**Figure 2. 17529 Simplified Internal Block Diagram**

# PIN CONNECTIONS

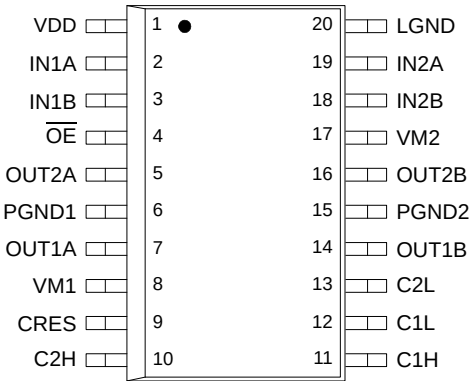



**Figure 3. 17529 Pin Connections**

**Table 1. Pin Function Description**

| Pin | PinName | Formal Name | Definition |
|---|---|---|---|
| 1 | VDD | Control Circuit Power Supply | Positive power source connection for control circuit. |
| 2 | IN1A | Logic Input Control 1A | Logic input control of OUT1A (refer to Table 5, Truth Table, page 7). |
| 3 | IN1B | Logic Input Control 1B | Logic input control of OUT1B (refer to Table 5, Truth Table, page 7). |
| 4 | $\overline{OE}$ | Output Enable | Logic output Enable control of H-Bridges (Low = True). |
| 5 | OUT2A | H-Bridge Output 2A | Output A of H-Bridge channel 2. |
| 6 | PGND1 | Power Ground 1 | High-current power ground 1. |
| 7 | OUT1A | H-Bridge Output 1A | Output A of H-Bridge channel 1. |
| 8 | VM1 | Motor Drive Power Supply 1 | Positive power source connection for H-Bridge 1 (Motor Drive Power Supply). |
| 9 | CRES | Pre-driver Power Supply | Internal triple charge pump output as pre-driver power supply. |
| 10 | C2H | Charge Pump 2H | Charge pump bucket capacitor 2 (positive pole). |
| 11 | C1H | Charge Pump 1H | Charge pump bucket capacitor 1 (positive pole). |
| 12 | C1L | Charge Pump 1L | Charge pump bucket capacitor 1 (negative pole). |
| 13 | C2L | Charge Pump 2L | Charge pump bucket capacitor 2 (negative pole). |
| 14 | OUT1B | H-Bridge Output 1B | Output B of H-Bridge channel 1. |
| 15 | PGND2 | Power Ground 2 | High-current power ground 2. |
| 16 | OUT2B | H-Bridge Output 2B | Output B of H-Bridge channel 2. |
| 17 | VM2 | Motor Drive Power Supply 2 | Positive power source connection for H-Bridge 2 (Motor Drive Power Supply). |
| 18 | IN2B | Logic Input Control 2B | Logic input control of OUT2B (refer to Table 5, Truth Table, page 7). |
| 19 | IN2A | Logic Input Control 2A | Logic input control of OUT2A (refer to Table 5, Truth Table, page 7). |
| 20 | LGND | Logic Ground | Low-current logic signal ground. |

# MAXIMUM RATINGS

**Table 2. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Motor Supply Voltage | $V_M$ | -0.5 to 8.0 | V |
| Charge Pump Output Voltage | $V_{CRES}$ | -0.5 to 14 | V |
| Logic Supply Voltage | $V_{DD}$ | -0.5 to 7.0 | V |
| Signal Input Voltage | $V_{IN}$ | -0.5 to $V_{DD}$+0.5 | V |
| Driver Output Current<br>Continuous<br>Peak (1) | <br>$I_O$<br>$I_{OPK}$ | <br>0.7<br>1.4 | A |
| ESD Voltage<br>Human Body Model (2)<br>Machine Model (3) | <br>$V_{ESD1}$<br>$V_{ESD2}$ | <br>±1500<br>±200 | V |
| Operating Junction Temperature | $T_J$ | -20 to 150 | °C |
| Operating Ambient Temperature | $T_A$ | -20 to 65 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 to 150 | °C |
| Thermal Resistance (4) | $R_{\theta JA}$ | 120 | °C/W |
| Power Dissipation (5) | $P_D$ | 1040 | mW |
| Peak Package Reflow Temperature During Reflow (6), (7) | $T_{PPRT}$ | Note 7 | °C |

Notes

1. $T_A$ = 25 °C, 10 ms pulse at 200 ms interval.
2. ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω).
4. Mounted on 37 x 50 Cu area (1.6 mm FR-4 PCB).
5. $T_A$ = 25 °C.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

# STATIC ELECTRICAL CHARACTERISTICS

**Table 3. Static Electrical Characteristics**

Characteristics noted under conditions $T_A$ = 25 °C, $V_{DD}$ = $V_M$ = 5.0 V, GND = 0 V, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER (VM1, VM2, VDD)** | | | | | |
| Motor Supply Voltage | $V_M$ | 2.0 | 5.0 | 6.8 | V |
| Logic Supply Voltage | $V_{DD}$ | 2.7 | 5.0 | 5.6 | V |
| Driver Quiescent Supply Current (No Signal Input) | $I_{QM}$ | – | – | 1.0 | μA |
| Logic Quiescent Supply Current (No Signal Input) (8) | $I_{QVDD}$ | – | – | 1.0 | mA |
| Operating Power Supply Current | | | | | mA |
| Logic Supply Current (9) | $I_{DVDD}$ | – | – | 3.0 | |
| Charge Pump Circuit Supply Current (10) | $I_{CRES}$ | – | – | 0.7 | |
| Low $V_{DD}$ Detection Voltage (11) | $V_{DDDET}$ | 1.5 | 2.0 | 2.5 | V |
| Driver Output ON Resistance (12) | $R_{DS(ON)}$ | – | 0.7 | 1.2 | Ohms |
| **GATE DRIVE** (C1L–C1H, C2L–C2H, CRES) | | | | | |
| Gate Drive Voltage | $V_{CRES}$ | 12 | 13 | 13.5 | V |
| Recommended External Capacitance (C1L–C1H, C2L–C2H, $C_{RES}$–GND) | $C_{CP}$ | 0.01 | 0.1 | 1.0 | μF |
| **CONTROL LOGIC ($\overline{OE}$, N1A, N1B, N2A, N2B)** | | | | | |
| Logic Input Voltage | $V_{IN}$ | 0.0 | – | $V_{DD}$ | V |
| Logic Inputs (2.7 V < $V_{DD}$ < 5.7 V) | | | | | |
| High-Level Input Voltage | $V_{IH}$ | $V_{DD}$ x 0.7 | – | – | V |
| Low-Level Input Voltage | $V_{IL}$ | – | – | $V_{DD}$ x 0.3 | V |
| High-Level Input Current | $I_{IH}$ | – | – | 1.0 | μA |
| Low-Level Input Current | $I_{IL}$ | -1.0 | – | – | μA |
| $\overline{OE}$ Pin Input Current Low | $I_{OIL\overline{OE}}$ | – | 50 | 100 | μA |

Notes

8. $I_{QVDD}$ includes the current to pre-driver circuit.
9. $I_{VDD}$ includes the current to pre-driver circuit at $f_{IN}$ = 100 kHz.
10. At $f_{IN}$ = 20 kHz.
11. Detection voltage is defined as when the output becomes high-impedance after $V_{DD}$ drops below the detection threshold. When the gate voltage $V_{CRES}$ is applied from an external source, $V_{CRES}$ = 7.5 V.
12. Source + sink at $I_O$ = 0.7 A.

**17529**

# DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 4. Dynamic Electrical Characteristics**

Characteristics noted under conditions $T_A$ = 25 °C, $V_{DD}$ = $V_M$ = 5.0 V, GND = 0 V, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **INPUT (IN1A, IN1B, OE, IN2A, IN2B)** | | | | | |
| Pulse Input Frequency | $f_{IN}$ | – | – | 200 | kHz |
| Input Pulse Rise Time (13) | $t_R$ | – | – | (14) 1.0 | μs |
| Input Pulse Fall Time (15) | $t_F$ | – | – | (14) 1.0 | μs |
| **OUTPUT (OUT1A, OUT1B, OUT2A, OUT2B)** | | | | | |
| Propagation Delay Time (16) | | | | | μs |
| Turn-ON Time | $t_{PLH}$ | – | 0.1 | 0.5 | |
| Turn-OFF Time | $t_{PHL}$ | – | 0.1 | 0.5 | |
| Charge Pump Wake-Up Time (17) | $t_{VGON}$ | – | 1.0 | 3.0 | ms |
| Low-Voltage Detection Time | $t_{VDDDET}$ | – | – | 10 | ms |

Notes

13. Time is defined between 10% and 90%.
14. That is, the input waveform slope must be steeper than this.
15. Time is defined between 90% and 10%.
16. Load of Output is 8.0 Ω resistance.
17. $C_{CP}$ = 0.1 μF.

# TIMING DIAGRAMS

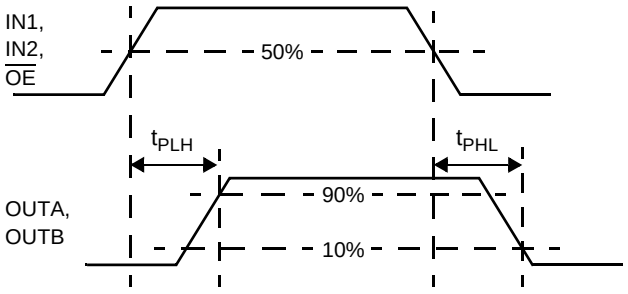



**Figure 4. $t_{PLH}$, $t_{PHL}$, and $t_{PZH}$ Timing**

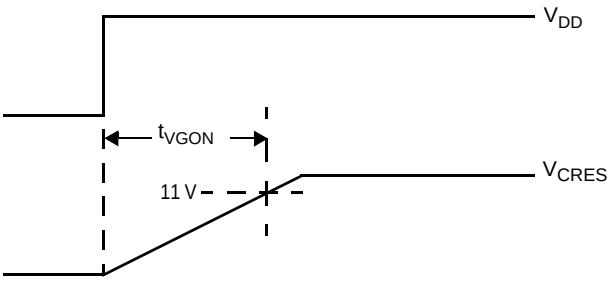



**Figure 6. Charge Pump Timing Diagram**

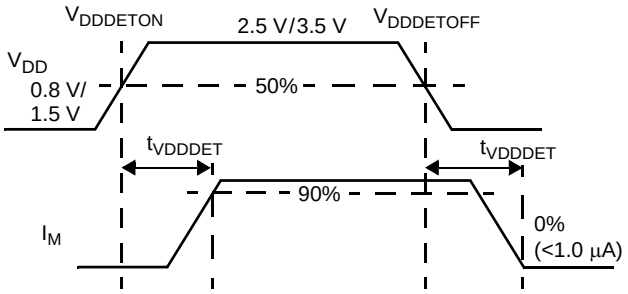



**Figure 5. Low-Voltage Detection Timing Diagram**

**Table 5. Truth Table**

| INPUT | | | OUTPUT | |
|---|---|---|---|---|
| $\overline{OE}$ | IN1A<br>IN2A | IN1B<br>IN2B | OUT1A<br>OUT2A | OUT1B<br>OUT2B |
| L | L | L | L | L |
| L | H | L | H | L |
| L | L | H | L | H |
| L | H | H | Z | Z |
| H | X | X | Z | Z |

H = High.
L = Low.
Z = High-impedance.
X = Don't care.
$\overline{OE}$ Pin is pulled up to $V_{DD}$ with internal resistance.

**17529**

# SYSTEM/APPLICATION INFORMATION

## *INTRODUCTION*

The 17529 is a monolithic dual H-Bridge ideal for portable electronic applications to control bipolar step motors and brush DC motors, such as those found in camera lens assemblies, camera shutters, optical disk drives, etc. The 17529 operates from 2.0 V to 6.8 V, providing dual H-bridge motor drivers with parallel 3.0 V or 5.0 V compatible I/O. The device features an on-board charge pump, as well as built-in shoot-through current protection and undervoltage shutdown.

The 17529 has four operating modes: forward, reverse, brake, and tri-stated (high-impedance). The MOSFETs comprising the output bridge have a total source + sink $R_{DS(ON)} \leq 1.2\ \Omega$.

The 17529 can simultaneously drive two brush DC motors or, as shown in Figure 1, 17529 Simplified Application Diagram on page 1, one bipolar step motor. The drivers are designed to be PWM'ed at frequencies up to 200 kHz.

## *FUNCTIONAL PIN DESCRIPTION*

### CONTROL CIRCUIT POWER SUPPLY (VDD)

The VDD pin carries the logic supply voltage and current into the logic sections of the IC. VDD has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

### LOGIC INPUT CONTROL (IN1A, IN1B, IN2A, AND IN2B)

These logic input pins control each H-Bridge output. IN1A logic HIGH = OUT1A HIGH. However, if all inputs are taken HIGH, the outputs bridges are both tri-stated (refer to Table 5, Truth Table, page 7).

### OUTPUT ENABLE ($\overline{OE}$)

The $\overline{OE}$ pin is a LOW = TRUE enable input. When $\overline{OE}$ = HIGH, all H-Bridge outputs (OUT1A, OUT1B, OUT2A, and OUT2B) are tri-stated (high-impedance), regardless of logic input (IN1A, IN1B, IN2A, and IN2B) states.

### H-BRIDGE OUTPUT (OUT1A, OUT1B, OUT2A, AND OUT2B)

These pins provide connection to the outputs of each of the internal H-Bridges (see Figure 2, 17529 Simplified Internal Block Diagram, page 2).

### MOTOR DRIVE POWER SUPPLY (VM1 AND VM2)

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the output pins. All VM pins must be connected together on the printed circuit board.

### CHARGE PUMP (C1L AND C1H, C2L AND C2H)

These two pairs of pins, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

### PRE-DRIVER POWER SUPPLY (CRES)

The CRES pin is the output of the internal charge pump. Its output voltage is approximately three times the $V_{DD}$ voltage. The $V_{CRES}$ voltage is power supply for internal pre-driver circuit of H-Bridges.

### POWER GROUND (PGND)

Power ground pins. They must be tied together on the PCB.

### LOGIC GROUND (LGND)

Logic ground pin.

# APPLICATIONS

## TYPICAL APPLICATION

Figure 7 shows a typical application for the 17529. When applying the gate voltage to the CRES pin from an external source, be sure to connect it via a resistor equal to, or greater than, $R_G = V_{CRES}/0.02\ \Omega$.

The internal charge pump of this device is generated from the VDD supply; therefore, care must be taken to provide sufficient gate-source voltage for the high side MOSFETs when $V_M >> V_{DD}$ (e.g., $V_M$ = 5.0 V, $V_{DD}$ = 3.0 V), in order to ensure full enhancement of the high-side MOSFET channels.

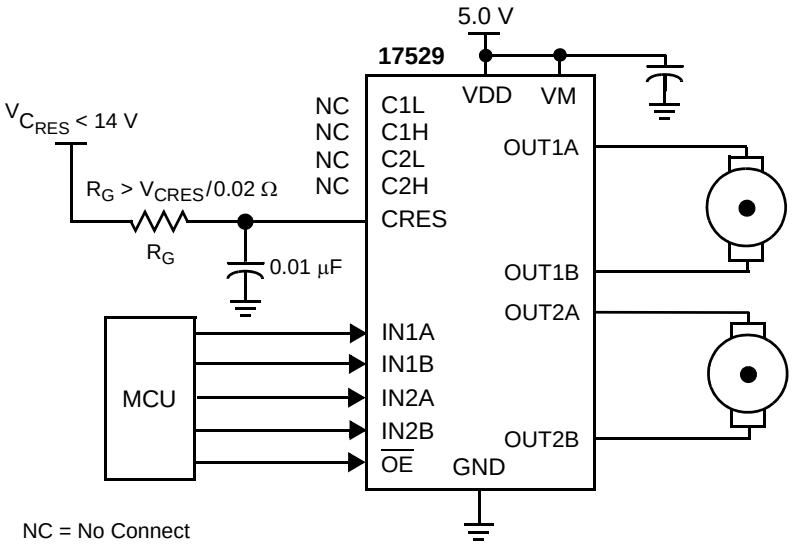



**Figure 7. 17529 Typical Application Diagram**

## CONDUCTED ELECTROMOTIVE FORCE (CEMF) SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a capacitor or zener at the supply pin (VM) (see Figure 8).

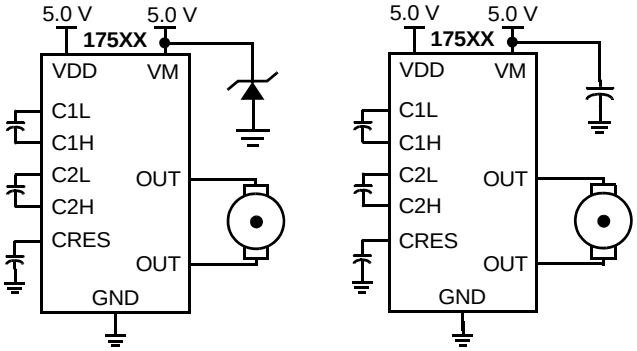



**Figure 8. CEMF Snubbing Techniques**

## PCB LAYOUT

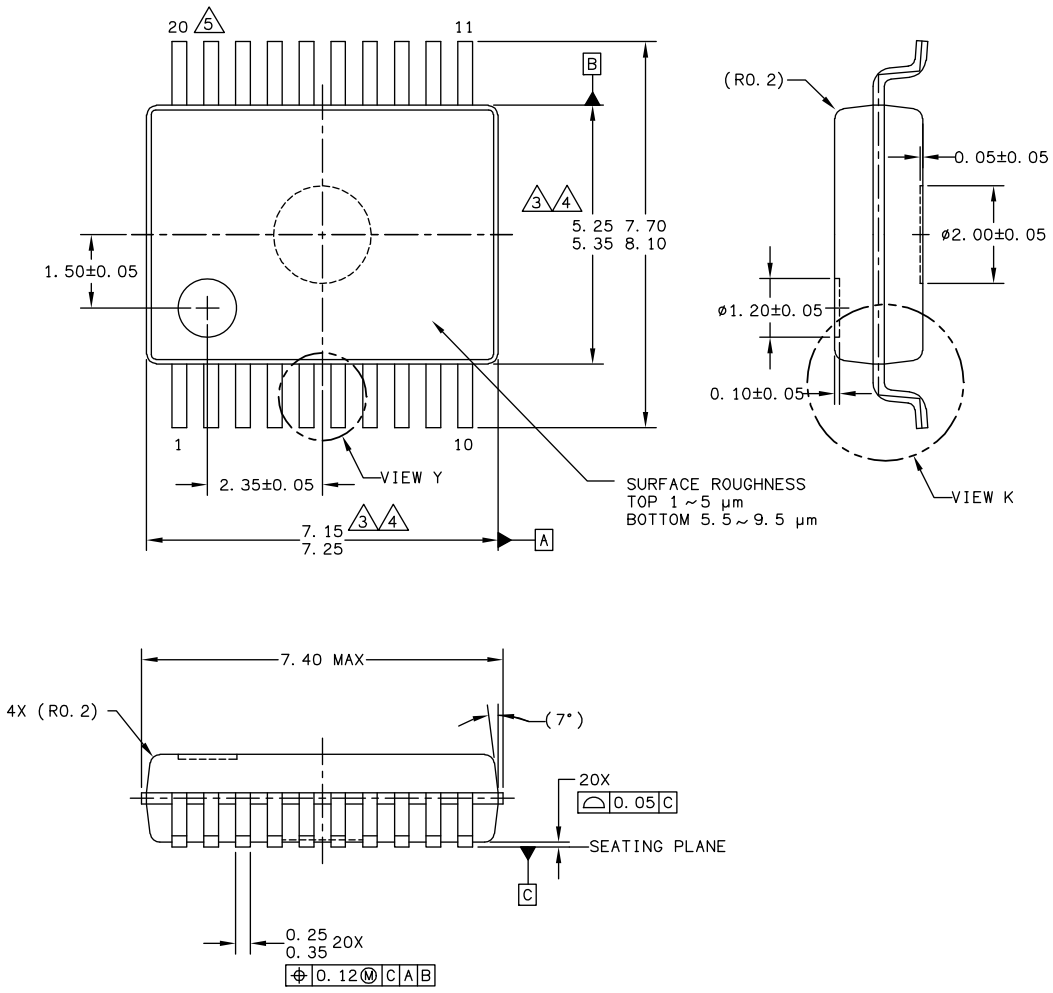
When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground pins to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distances.

## *PACKAGE DIMENSIONS*

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

**Table 6.**

| Package | Suffix | Package Outline Drawing Number |
|---|---|---|
| 20-PIN VMFP | EV | 98ASA10616D |

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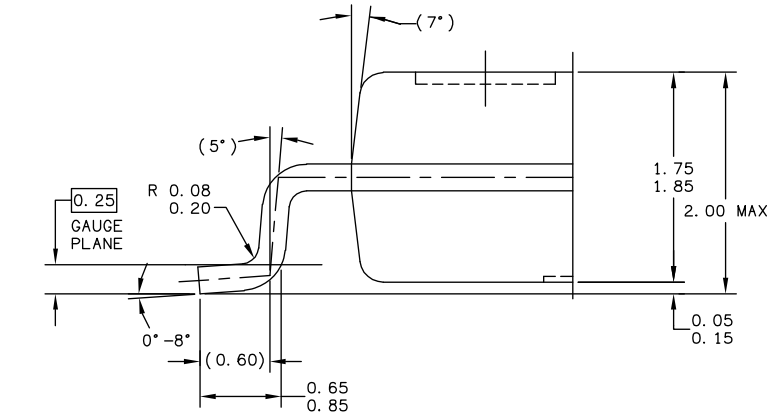
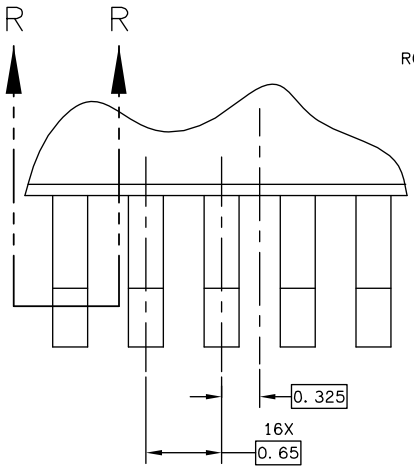
|---|---|---|
| TITLE: EIAJ VMFP 20LD, 0. 65 PITCH | DOCUMENT NO: 98ASA10616D | REV: B |
| | CASE NUMBER: 1569–02 | 01 DEC 2006 |
| | STANDARD: NON–JEDEC | |

**EV (Pb-FREE) SUFFIX**
20-LEAD VMFP
98ASA10616D
ISSUE B

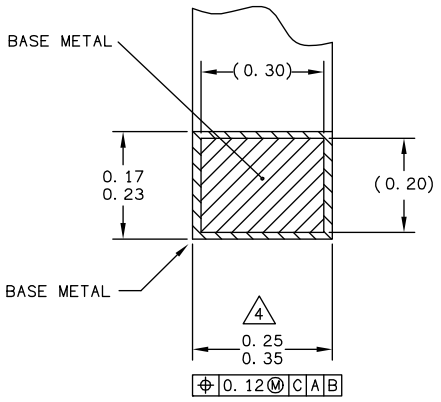
**17529**




VIEW Y

VIEW K
ROTATED 90° CW




SECTION R–R

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| | CASE NUMBER: 1569-02 | 01 DEC 2006 |
| | STANDARD: NON-JEDEC | |

**EV (Pb-FREE) SUFFIX**
20-LEAD VMFP
98ASA10616D
ISSUE B

**17529**

NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.

2 ALL DIMENSIONS ARE IN MILLIMETERS.

3 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.10 ANY SIDE.
DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE.

4 DIMENSIONS ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY
EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS, AND INTERLEAD FLASH,
BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

5 TERMINAL NUMBER ARE SHOWN FOR REFERENCE ONLY.



| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|

| TITLE: EIAJ VMFP 20LD, 0.65 PITCH | DOCUMENT NO: 98ASA10616D | REV: B |
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ISSUE B

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# REVISION HISTORY

| Revision | Date | Description of Changes |
|---|---|---|
| 2.0 | 9/2005 | • Implemented Revision History page<br>• Converted to Freescale format |
| | 12/2013 | • No technical changes<br>• Revised back page<br>• Updated document properties |

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Document Number: MPC17529
Rev 2.0
12/2013