

IR2104/IR21044

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 5V Schmitt-triggered input logic
- Cross-conduction prevention logic
- Internally set deadtime
- High side output in phase with input
- Shut down input turns off both channels
- Matched propagation delay for both channels

Product Summary

V _{OFFSET}	600V max.
I _{O+/-}	130 mA / 270 mA
V _{OUT}	10 - 20V
t _{on/off} (typ.)	680 & 150 ns
Deadtime (typ.)	520 ns

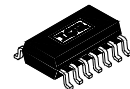
Description

The IR2104/IR21044 are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

Packages



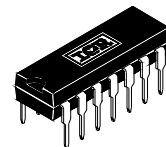
8 Lead SOIC
IR2104S



14 Lead SOIC
IR21044S

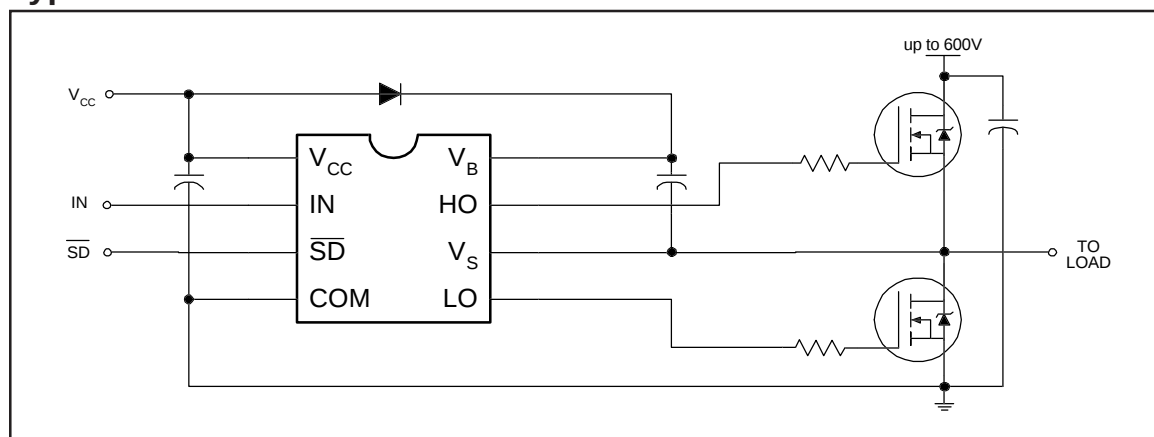


8 Lead PDIP
IR2104



14 Lead PDIP
IR21044

Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _B	High side floating absolute voltage	-0.3	625	V	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3		
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (IN & $\overline{\text{SD}}$)	-0.3	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
R _{thJA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	0	V_{CC}	
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	820	ns	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	150	220		$V_S = 600V$
t_{sd}	Shutdown propagation delay	—	160	220		
t_r	Turn-on rise time	—	100	170		
t_f	Turn-off fall time	—	50	90		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		
MT	Delay matching, HS & LS turn-on/off	—	—	60		

Static Electrical Characteristics

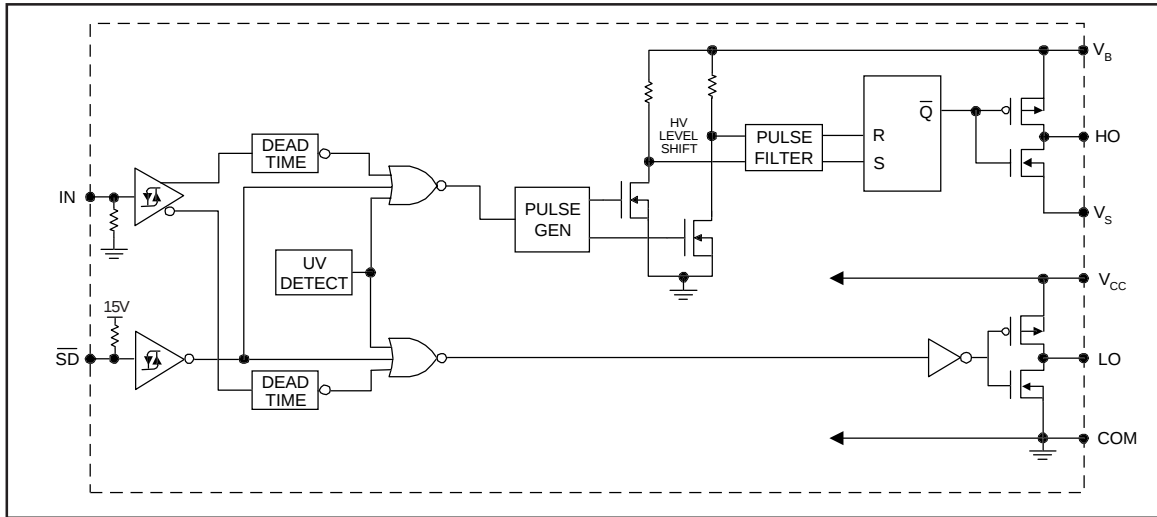
V_{BIAS} (V_{CC} , V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" (HO) & Logic "0" (LO) input voltage	3	—	—	V	$V_{CC} = 10V$ to 20V
V_{IL}	Logic "0" (HO) & Logic "1" (LO) input voltage	—	—	0.8		$V_{CC} = 10V$ to 20V
$V_{SD,TH+}$	SD input positive going threshold	3	—	—		$V_{CC} = 10V$ to 20V
$V_{SD,TH-}$	SD input negative going threshold	—	—	0.8		$V_{CC} = 10V$ to 20V
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
V_{OL}	Low level output voltage, V_O	—	—	100		$I_O = 0A$
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		$V_{IN} = 0V$ or 5V
I_{IN+}	Logic "1" input bias current	—	3	10		$V_{IN} = 5V$
I_{IN-}	Logic "0" input bias current	—	—	1		$V_{IN} = 0V$
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
I_{O+}	Output high short circuit pulsed current	130	210	—	mA	$V_O = 0V$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	270	360	—		$V_O = 15V$ $PW \leq 10 \mu s$

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Functional Block Diagram



Lead Definitions

Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO
$\overline{SD}$	Logic input for shutdown
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

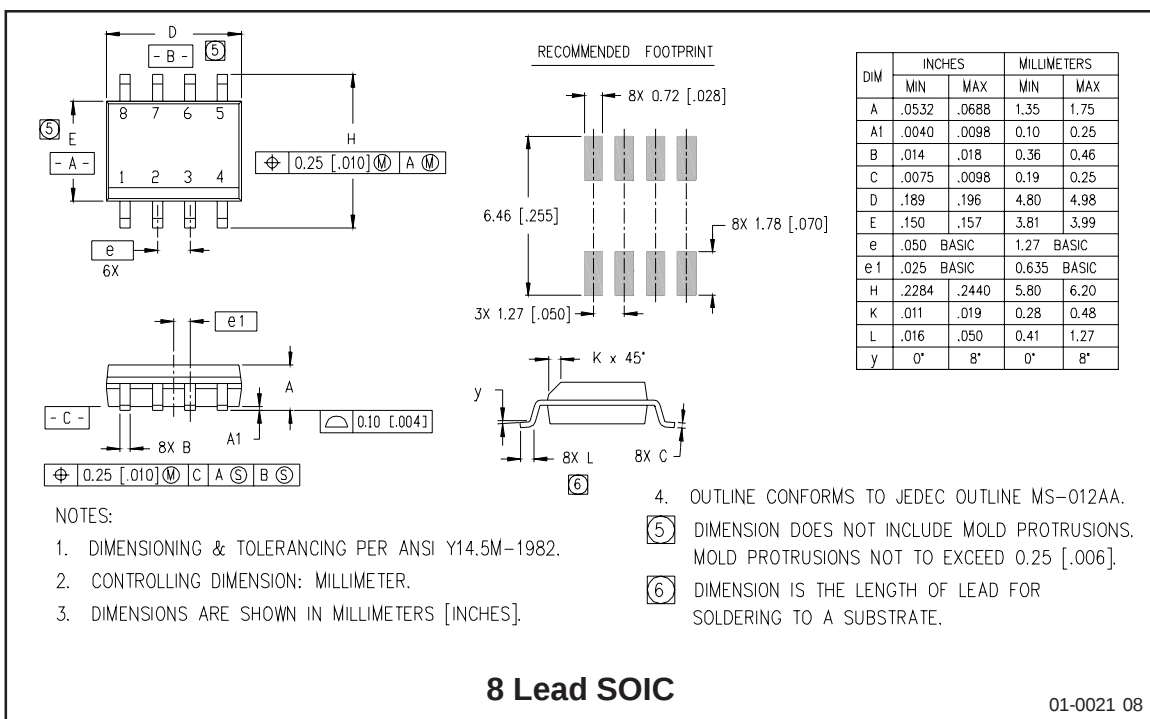
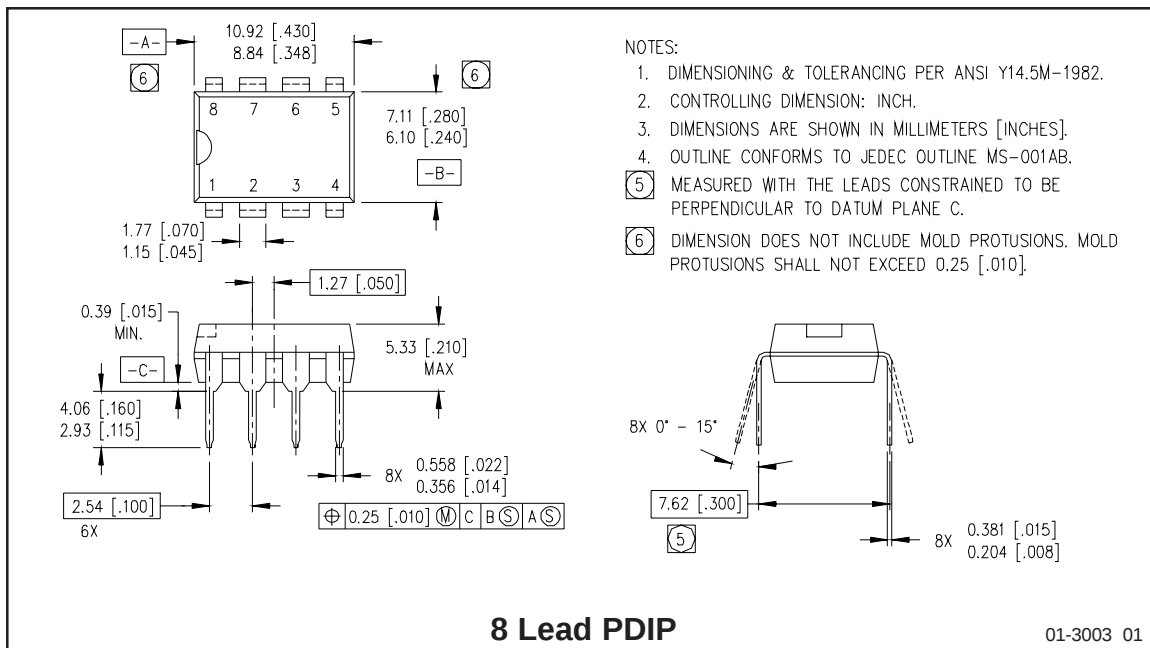
Lead Assignments

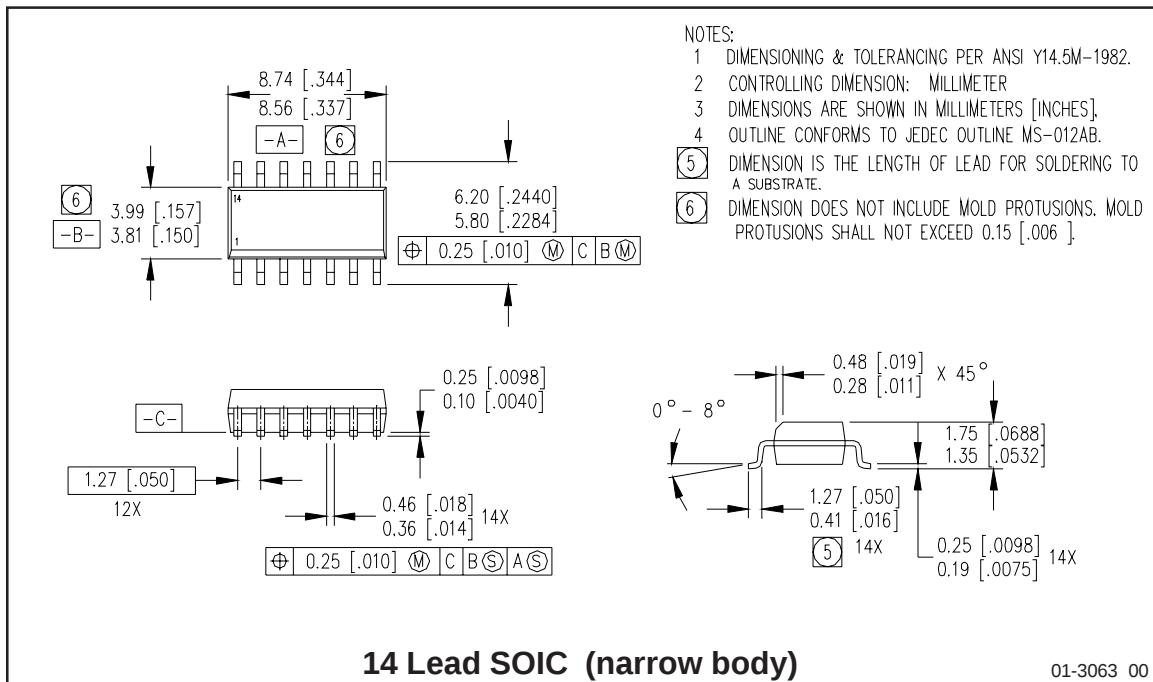
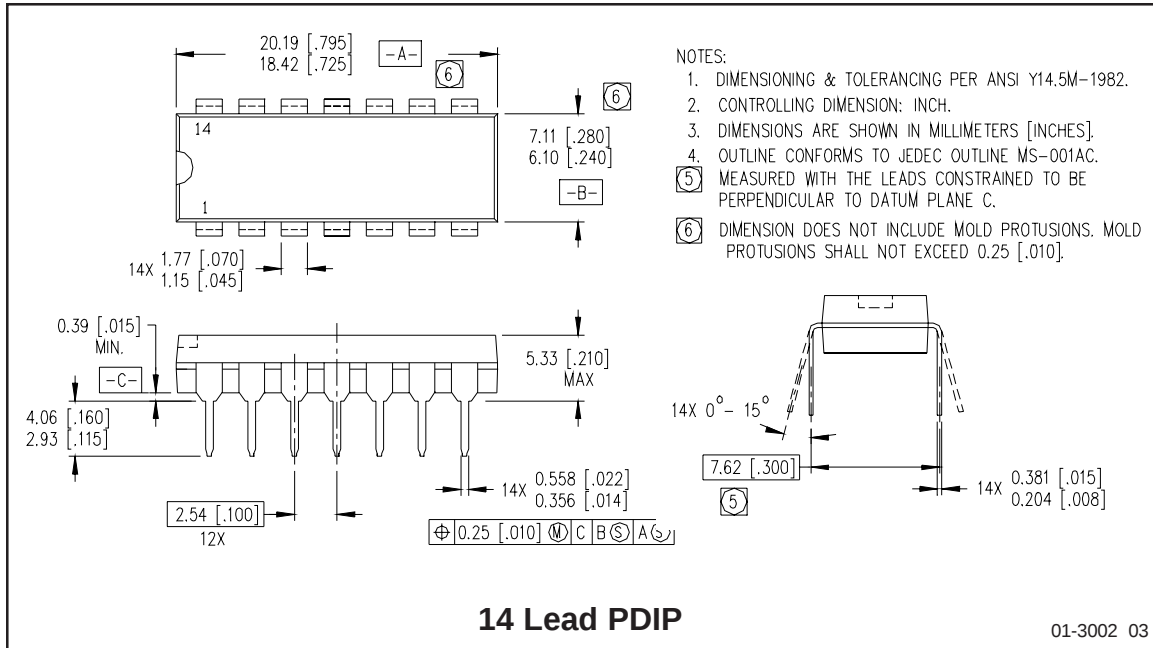
Pinout diagram for IR2104 (8 Lead PDIP): - Pin 1: V_{CC} - Pin 2: IN - Pin 3: $\overline{SD}$ - Pin 4: COM - Pin 5: LO - Pin 6: V_S - Pin 7: HO - Pin 8: V_B 8 Lead PDIP IR2104	Pinout diagram for IR2104S (8 Lead SOIC): - Pin 1: V_{CC} - Pin 2: IN - Pin 3: $\overline{SD}$ - Pin 4: COM - Pin 5: LO - Pin 6: V_S - Pin 7: HO - Pin 8: V_B 8 Lead SOIC IR2104S
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Pinout diagram for IR21044 (14 Lead PDIP): - Pin 1: V_{CC} - Pin 2: IN - Pin 3: $\overline{SD}$ - Pin 4: COM - Pin 5: LO - Pin 6: V_S - Pin 7: HO - Pin 8: V_B - Pin 9: V_S - Pin 10: V_B - Pin 11: HO - Pin 12: V_B - Pin 13: V_{CC} - Pin 14: V_B 14 Lead PDIP IR21044	Pinout diagram for IR21044S (14 Lead SOIC): - Pin 1: V_{CC} - Pin 2: IN - Pin 3: $\overline{SD}$ - Pin 4: COM - Pin 5: LO - Pin 6: V_S - Pin 7: HO - Pin 8: V_B - Pin 9: V_S - Pin 10: V_B - Pin 11: HO - Pin 12: V_B - Pin 13: V_{CC} - Pin 14: V_B 14 Lead SOIC IR21044S
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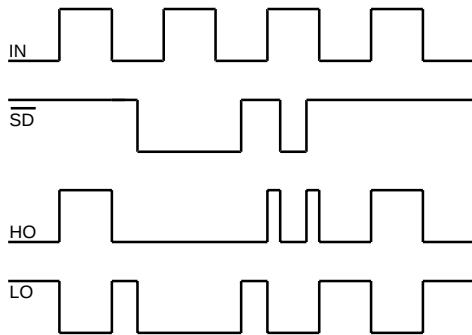


Figure 1. Input/Output Timing Diagram

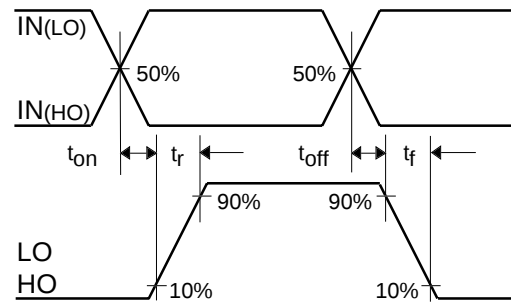


Figure 2. Switching Time Waveform Definitions

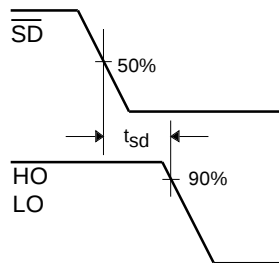


Figure 3. Shutdown Waveform Definitions

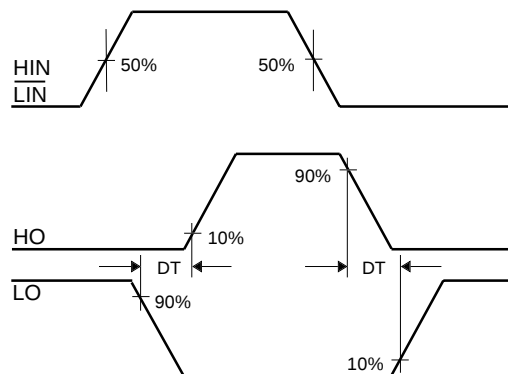


Figure 4. Deadtime Waveform Definitions

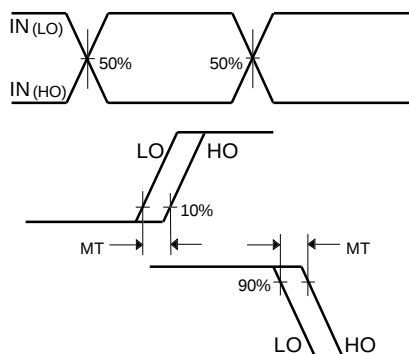


Figure 5. Delay Matching Waveform Definitions

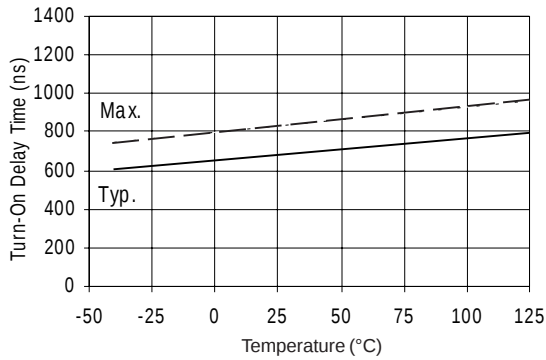


Figure 6A. Turn-On Time vs Voltage

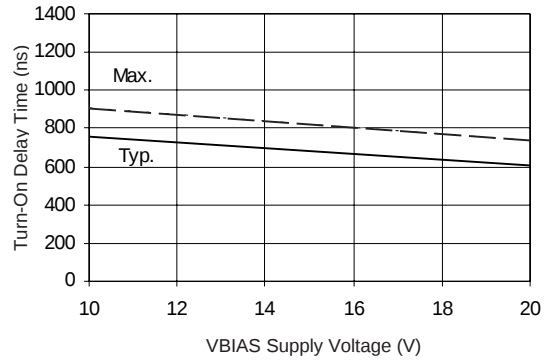


Figure 6B. Turn-On Time vs Voltage

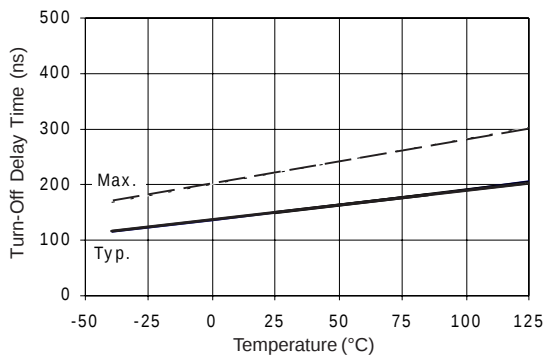


Figure 7A. Turn-Off Time vs Temperature

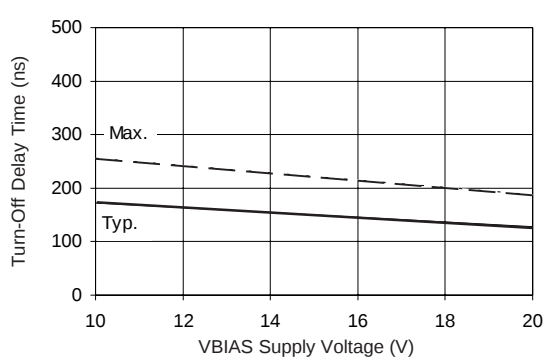


Figure 7B. Turn-Off Time vs Voltage

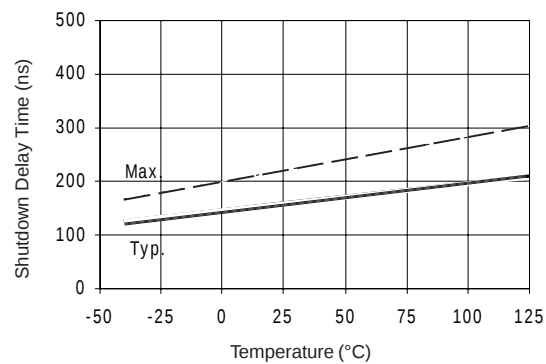


Figure 8A. Shutdown Time vs Temperature

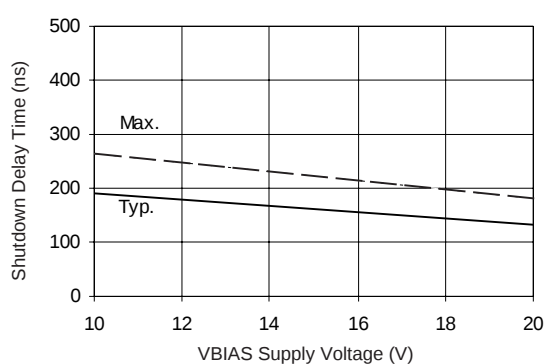


Figure 8B. Shutdown Time vs Voltage

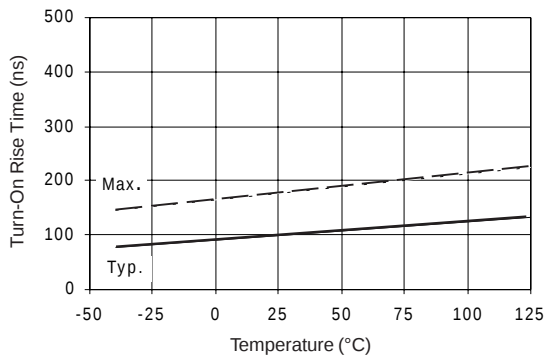


Figure 9A. Turn-On Rise Time vs Temperature

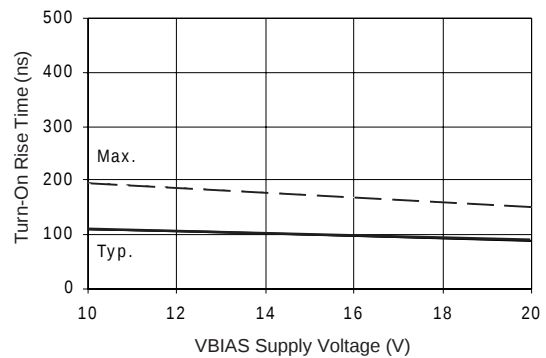


Figure 9B. Turn-On Rise Time vs Voltage

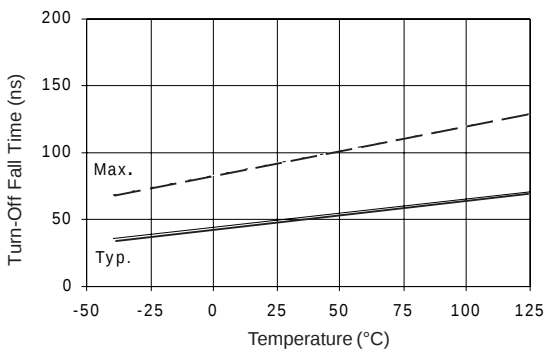


Figure 10A. Turn-Off Fall Time vs Temperature

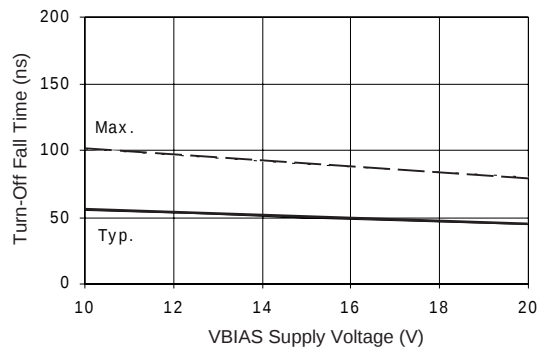


Figure 10B. Turn-Off Fall Time vs Voltage

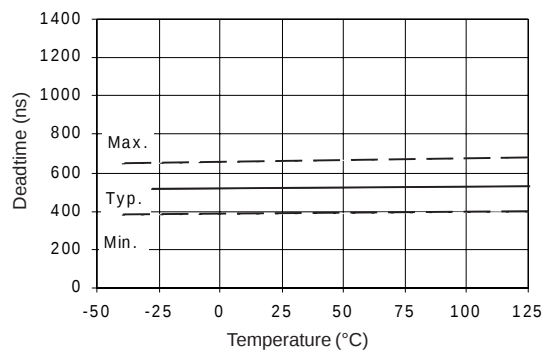


Figure 11A. Deadtime vs Temperature

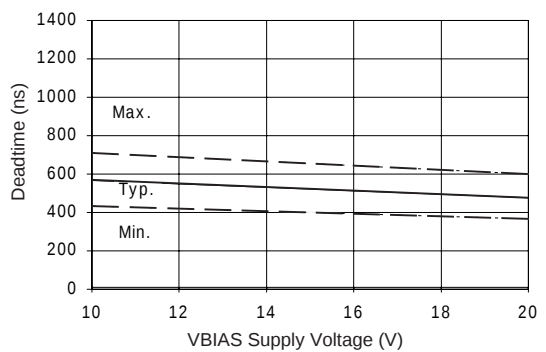


Figure 11B. Deadtime vs Voltage

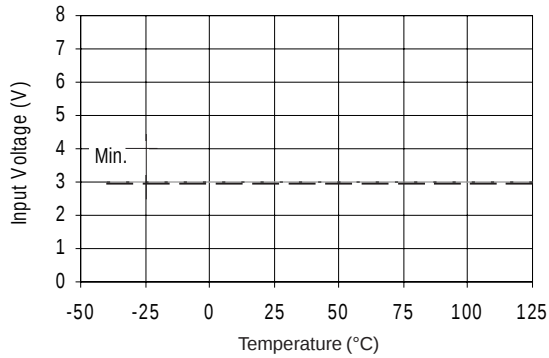


Figure 12A. Logic "1" (HO) & Logic "0" (LO) & Inactive SD Input Voltage vs Temperature

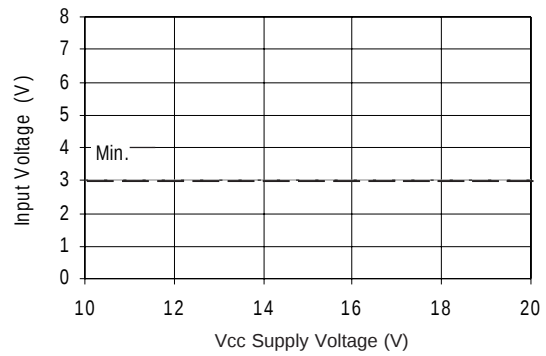


Figure 12B. Logic "1" (HO) & Logic "0" (LO) & Inactive SD Input Voltage vs Voltage

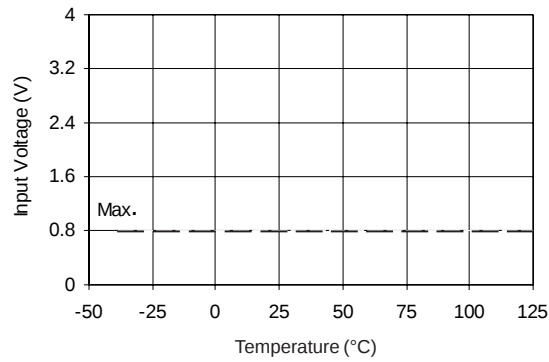


Figure 13A. Logic "0" (HO) & Logic "1" (LO) & Active SD Input Voltage vs Temperature

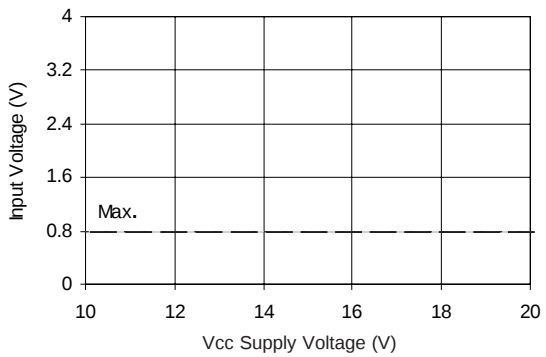


Figure 13B. Logic "0" (HO) & Logic "1" (LO) & Active SD Input Voltage vs Voltage

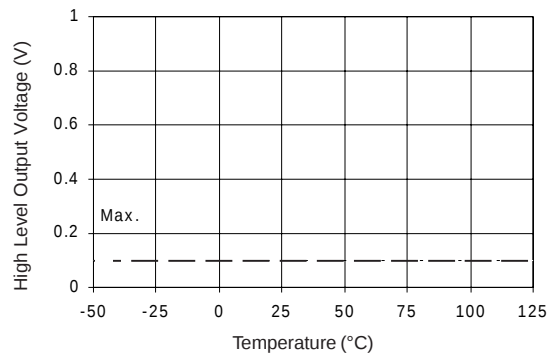


Figure 14A. High Level Output vs Temperature

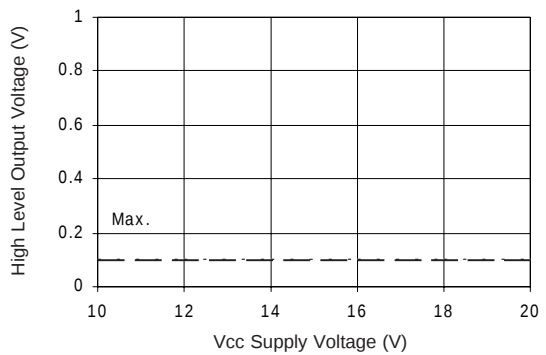


Figure 14B. High Level Output vs Voltage

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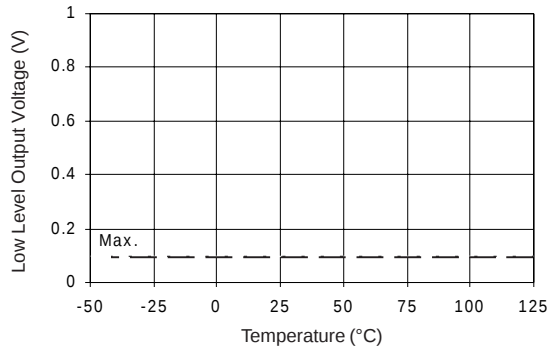


Figure 15A. Low Level Output vs Temperature

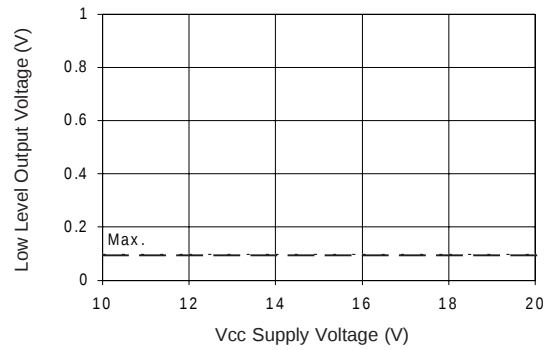


Figure 15B. Low level Output vs Voltage

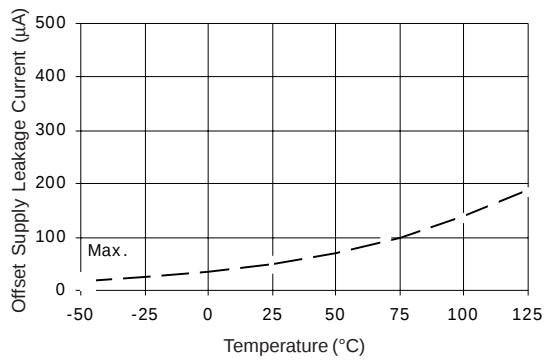


Figure 16A. Offset Supply Current vs Temperature

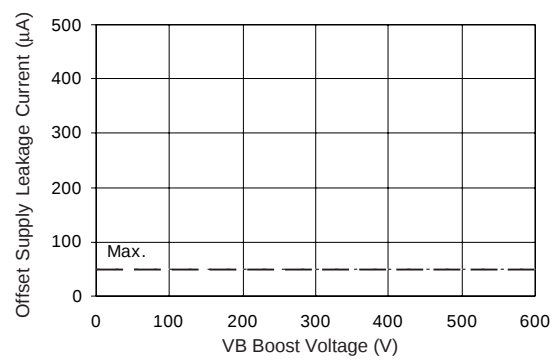


Figure 16B. Offset Supply Current vs Voltage

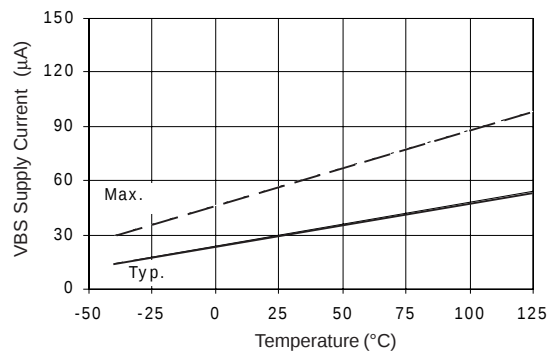


Figure 17A. VBS Supply Current vs Temperature

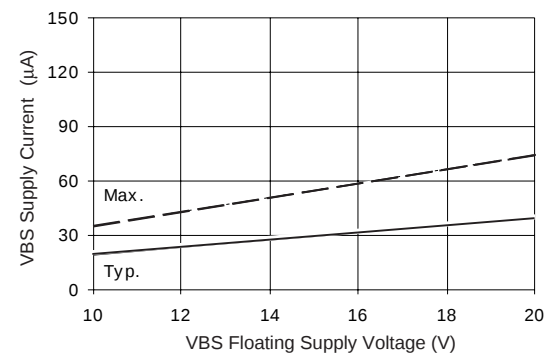


Figure 17B. VBS Supply Current vs Voltage

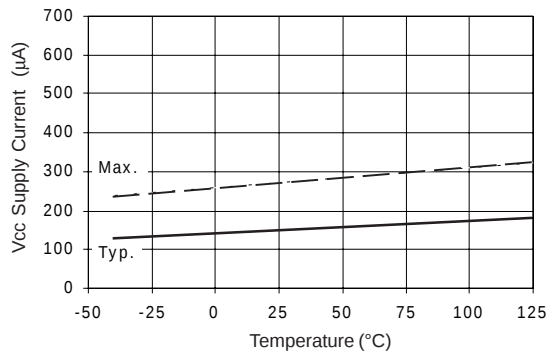


Figure 18A. Vcc Supply Current vs Temperature

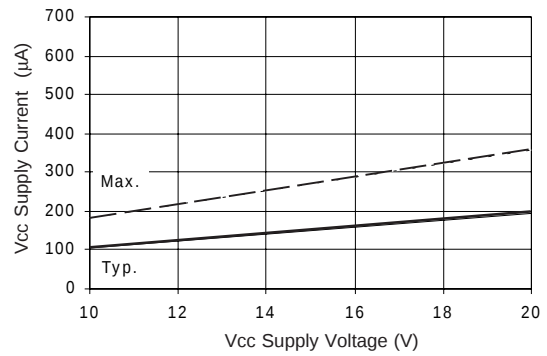


Figure 18B. Vcc Supply Current vs Voltage

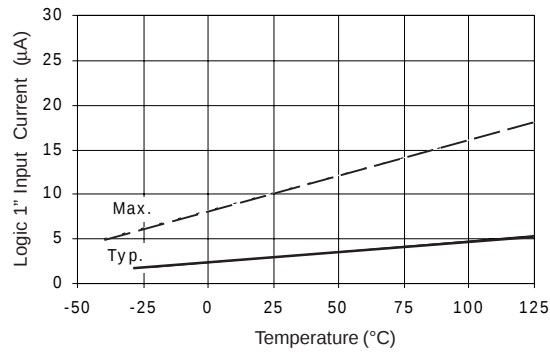


Figure 19A. Logic "1" Input Current vs Temperature

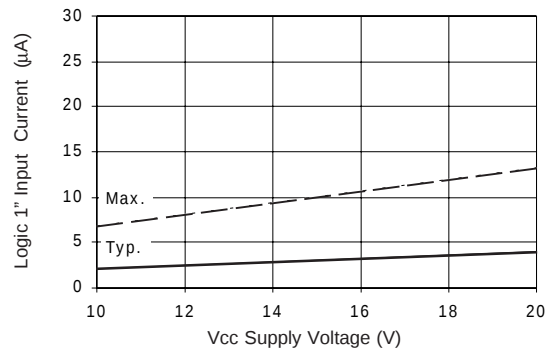


Figure 19B. Logic "1" Input Current vs Voltage

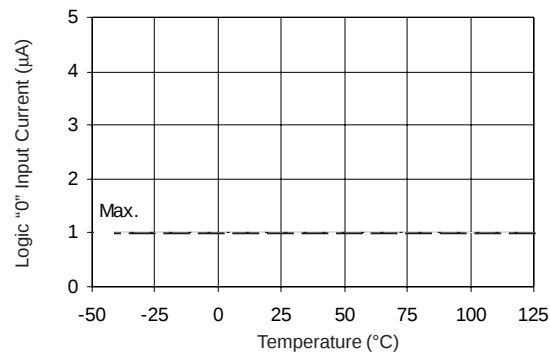


Figure 20A. Logic "0" Input Current vs Temperature

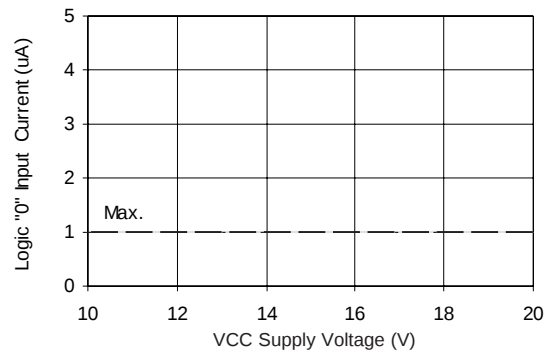


Figure 20B. Logic "0" Input Current vs Voltage

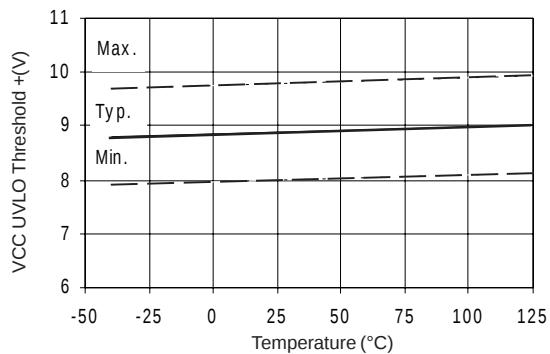


Figure 21A. Vcc Undervoltage Threshold(+) vs Temperature

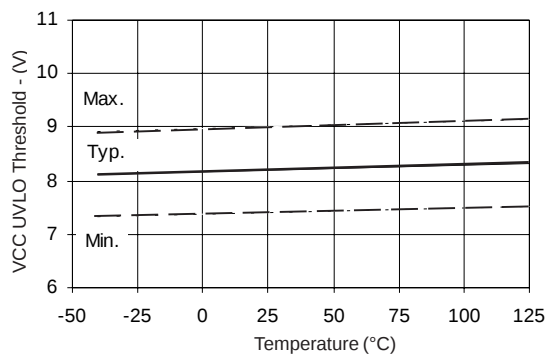


Figure 21B. Vcc Undervoltage Threshold(-) vs Temperature

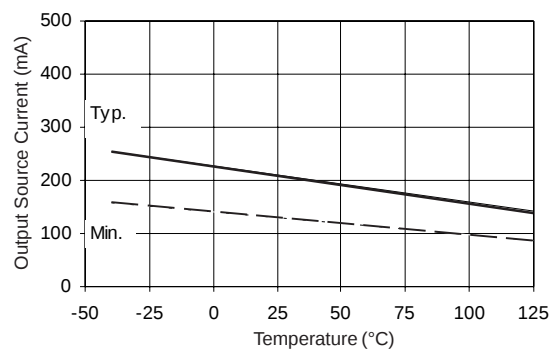


Figure 22A. Output Source Current vs Temperature

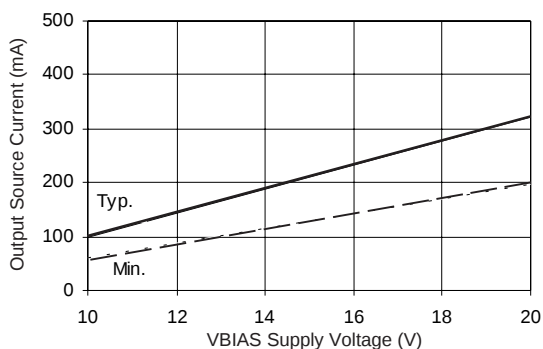


Figure 22B. Output Source Current vs Voltage

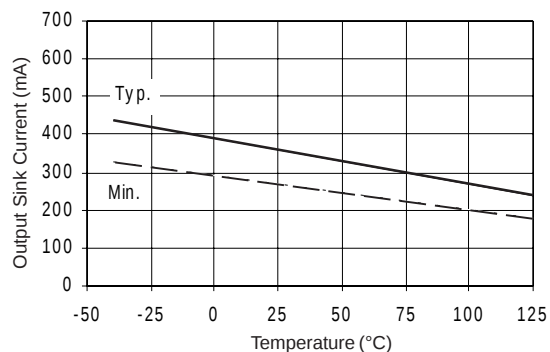


Figure 23A. Output Sink Current vs Temperature

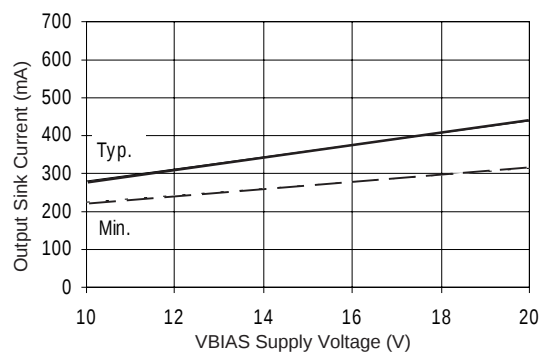


Figure 23B. Output Sink Current vs Voltage

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IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171 Tel: 81 3 3983 0086

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