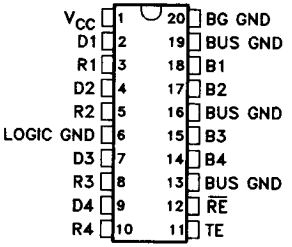
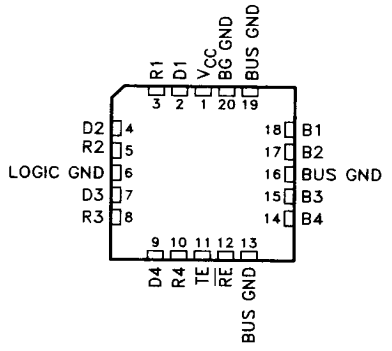
TI0267—D3077, JANUARY 1988—REVISED SEPTEMBER 1989

- **High Speed Quad Transceiver**
- **Fully Compatible with IEEE Standard 896.1-1987 Futurebus Requirements**
- **Drives Load Impedances as Low as 10 Ω**
- **High-Speed Advanced Low-Power Schottky Circuits**
- **Low Power Dissipation . . . 81 mW Max per Channel**
- **High-Impedance P-N-P Inputs**
- **BTL™ Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Low Bus-Port Capacitance**
- **Power-Up/Power-Down Protection (Glitch-Free)**
- **Open-Collector Driver Outputs Allows Wired-OR Connections**
- **Multiple Bus Channel Ground Returns to Reduce Channel Noise Interference**
- **Designed to Be a Faster, Lower Power Functional Equivalent of National DS3893**

N PACKAGE
(TOP VIEW)



FN CHIP CARRIER PACKAGE
(TOP VIEW)



description

The SN75ALS053 is a four-channel, monolithic, high-speed, advanced low-power Schottky device designed for two-way data communication in a densely populated backplane. The SN75ALS053 has independent driver input (Dn) and receiver output (Rn) pins and separate driver and receiver disables. This transceiver is designed for use in high-speed bus systems and is similar to the SN75ALS057 transceiver except that the trapezoidal feature has been eliminated to speed up the propagation delays.

These transceivers feature open-collector driver outputs, each with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pullup on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs are capable of driving an equivalent dc load of as low as 10 Ω.

The receivers have a precision threshold set by an internal bandgap reference to give accurate input thresholds over V_{CC} and temperature variations.

These transceivers are compatible with Backplane Transceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

The SN75ALS053 is characterized for operation from 0°C to 70°C.

BTL is a trademark of National Semiconductor Corporation.

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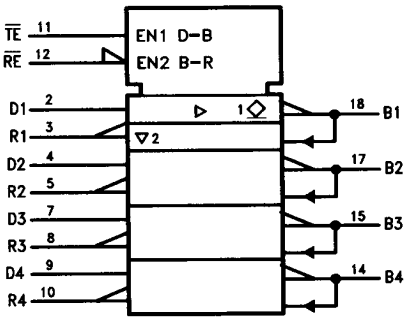
FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS		CHANNELS	
TE	$\overline{RE}$	D → B	B → R
L	L	D	R
L	H	D	D
H	L	T	R
H	H	T	D

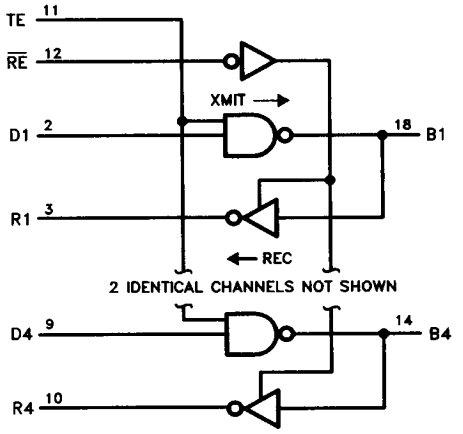
H = high level, L = low level, R = receive, T = transmit, D = disable
Direction of data transmission is from Dn to Bn, direction of data reception is from Bn to Rn.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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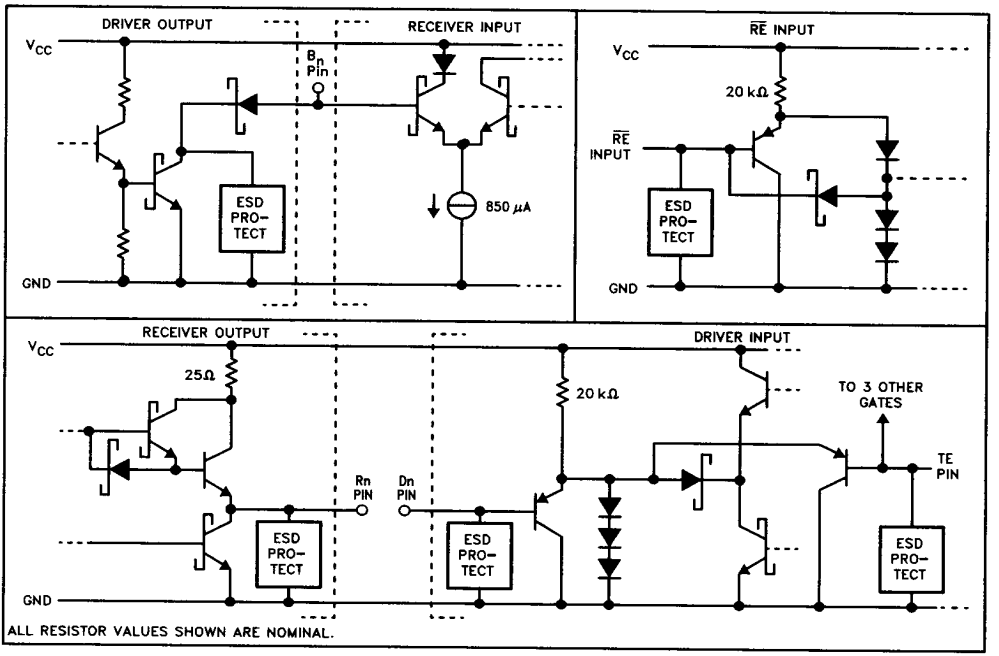
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6 V
Control input voltage	5.5 V
Driver input voltage	5.5 V
Driver output voltage	2.5 V
Receiver input voltage	2.5 V
Receiver output voltage	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6mm (1/16 in.) from case for 10 seconds: N package	260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
FN	1400 mW	11.2 mW/°C	896 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level driver and control input voltage	2			V
V_{IL}	Low-level driver and control input voltage			0.8	V
	Bus termination voltage	1.9		2.1	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, DE, or $\overline{RE}$		$I_I = -18$ mA			−1.5	V
V_T	Receiver input threshold at Bn			1.426		1.674	V
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, $\overline{RE}$ at 0.8 V, $I_{OH} = -1$ mA	2.5			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, $\overline{RE}$ at 0.8 V, $I_{OL} = 20$ mA			0.5	V
		Bn	Dn at 2.4 V, TE at 2.4 V, $V_L = 2$ V, $R_L = 10\ \Omega$, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	Dn, TE or $\overline{RE}$	$V_I = V_{CC}$			40	μA
		Bn	$V_I = 2$ V, $V_{CC} = 0$ or 5.25 V, Dn at 0.8 V, TE at 0.8 V,			100	
I_{IL}	Low-level input current at Dn, TE or $\overline{RE}$		$V_I = 0.4$ V			−400	μA
I_{OS}	Short-circuit output current at Rn		Rn at 0 V, Bn at 1.2 V, $\overline{RE}$ at 0.8 V	−70		−200	mA
I_{CC}	Supply curent					65	mA
$C_{o(B)}$	Driver output capacitance		$V_{CC} = 5$ V, $T_A = 25°C$		6.5		pF

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Dn	Bn	TE at 3 V, V_L = 2 V, See Figure 2	2	7	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	7	
t_{PLH}	Propagation delay time, low-to-high-level output	Dn	Bn	Dn at 3 V, V_L = 2 V, See Figure 2	2	7	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	7	
t_{TLH}	Transition time, low-to-high-level output	Dn	Bn	TE at 3 V, V_L = 2 V, See Figure 2	0.5	5	ns
t_{THL}	Transition time, high-to-low-level output				0.5	5	
	Skew between driver channels†	Dn	Bn	TE at 3 V, V_L = 2 V		1	ns

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.3 V, TE at 0.3 V, See Figure 3	2	8	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	8	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, TE at 0.3 V, V_L = 5 V, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		6	ns
t_{PZL}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, TE at 0.3 V, V_L = 5 V, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		12	ns
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 1 V, TE at 0.3 V, V_L = 0, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		6	ns
t_{PZH}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 1 V, TE at 0.3 V, V_L = 0, C_L = 5 pF, R_{L1} = 500 Ω, See Figure 4		12	ns
	Skew between receiver channels†	Bn	Rn	$\overline{RE}$ at 0.3 V, TE at 0.3 V		1	ns

† Skew is the difference between the propagation delay time (t_{PLH} or t_{PHL}) of one receiver channel and that same propagation delay time of any other receiver channel. It applies for both t_{PLH} and t_{PHL}.

PARAMETER MEASUREMENT INFORMATION

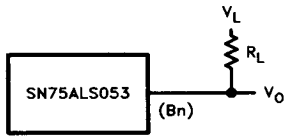
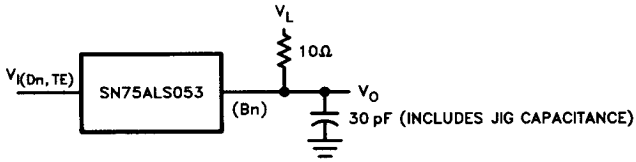
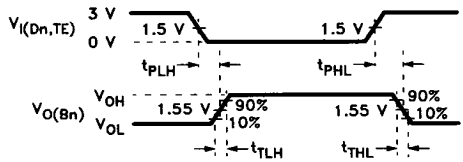


FIGURE 1. DRIVER LOW-LEVEL-OUTPUT-VOLTAGE TEST CIRCUIT



TEST CIRCUIT

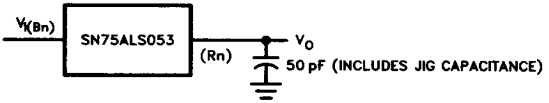


VOLTAGE WAVEFORMS

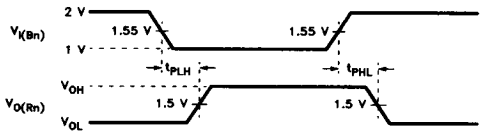
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



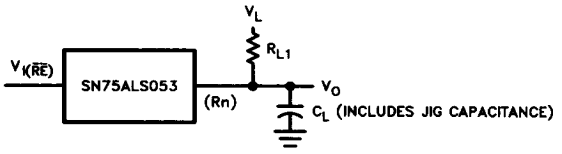
TEST CIRCUIT



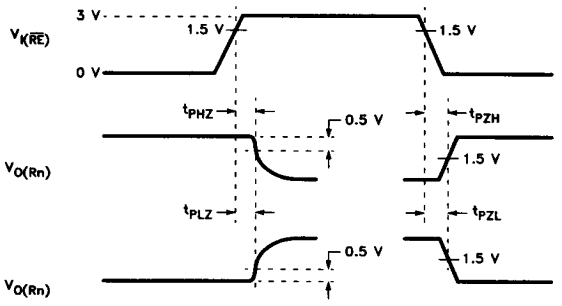
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%

FIGURE 3. RECEIVER PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 4. PROPAGATION DELAY FROM $\overline{RE}$ TO Rn